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Temperature-Dependent Evaluation of Commercial 1.2 kV, 40 mΩ 4H-SiC MOSFETs: A Comparative Study between Planar, One-Side Shielded Trench, and Double Trench Gate Structures

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Abstract. This research investigates the static and dynamic characteristics of 4H-Silicon Carbide (SiC) MOSFETs with different gate structures: planar (Device A), one-side shielded trench (Device B), and double trench (Device C). We analyze threshold voltage, on-state resistance, transconductance, gate-to-source capacitances, and reverse transfer/miller capacitances with gate bias. Additionally, non-linear charges, including input charge, miller plateau, and total gate charge, are examined. Switching losses are assessed over a temperature range of 25° C to 125° C. Our findings reveal distinct performance differences, offering valuable insights for optimizing SiC MOSFETs in electric vehicle applications.

Introduction

The rapid growth of the Electric Vehicle (EV) industry has brought forth a notable surge in the utilization of 4H-Silicon Carbide (SiC) devices, owing to their superior efficiency and enhanced power density in comparison to traditional Silicon (Si) based power electronic devices [1]. In this context, trench SiC MOSFETs have emerged as a pivotal development aimed at curtailing conduction losses in power applications, exhibiting substantially superior performance when contrasted with planar SiC MOSFETs [2]. However, despite the extensive body of research devoted to planar gate SiC MOSFETs, a discernible knowledge gap persists, particularly concerning the intricate nuances of the static and dynamic performance of trench SiC MOSFETs, with a specialized focus on the underlying device physics that contribute to conduction and switching losses. This research aims to bridge this knowledge chasm by undertaking a comprehensive characterization of the static and dynamic performance of commercially available discrete 1200 V, 40 mΩ planar (Device A), one-side shielded trench (Device B), and double trench (Device C) gate structures under varying temperature conditions. The scope of the study encompasses a meticulous array of static and dynamic tests, systematically exploring the impact of gate structure on current conduction in pulse switching mode. Moreover, a thorough analysis of the reverse recovery and switching characteristics will be conducted to glean deeper insights into the intricate functioning of these SiC devices. The outcomes of this research endeavor are anticipated to elucidate potential devices with significantly reduced switching losses, thus offering invaluable insights for EV manufacturers contemplating the adoption of planar or trench SiC MOSFETs in the realm of automotive applications. It is worth emphasizing that this study augments the existing literature by delving deeply into the device physics that underpin conduction and switching losses in trench SiC MOSFETs, with the potential to pave the way for tangible advancements in SiC device development and their subsequent integration into EV applications. Consequently, the findings of this study are poised to have far-reaching implications for the burgeoning EV industry and the broader domain of power electronics.

Results and Discussion

The aim of this study was to investigate the static and dynamic characteristics of three commercially available 1.2 kV 4H-SiC MOSFETs with different gate structures (Fig. 1a, 1b, 1c) in TO-247 casings. The devices were characterized using the B1505A for I-V and C-V characteristics and Keysight PD1500A dynamic power device analyzer by performing double pulse tests (DPT) over a range of device case temperatures [3].

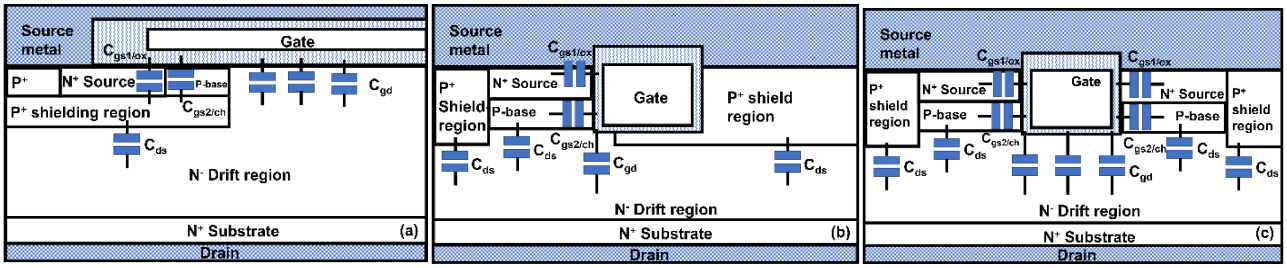

Fig. 1. Cross-sectional view of vertical power 4H-SiC MOSFET test structures: (a) Device A, (b) Device B, and (c) Device C (inset: non-linear parasitic capacitances between S, G, and D terminals).

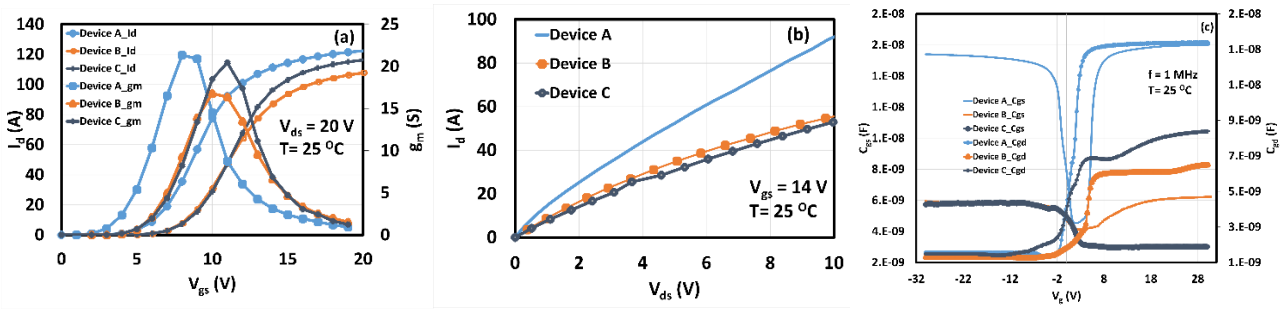

Fig. 2. Measured (a) transfer, (b) output characteristics and (b) non-linear C-V characteristics between each terminal for three gate structures of 1.2 kV 4H-SiC MOSFET.

To determine the threshold voltage (V_{TH}), on-state resistance (R_{ON}), and transconductance (g_m) of each gate structure, we measured the transfer (Fig. 2a) and output (Fig. 2b) characteristics of the three devices. We found that Device A had a lower V_{TH} (2.5 V) due to lower p-doping with a constant current method of 10 mA and resulting in increased g_m compared to the other devices. Device A also exhibited faster transient behavior in switching environments may be due to decreased channel lengths and depths compared to Device B (V_{TH}: 5.5 V) and Device C (V_{TH}: 5.7 V). Additionally, Device A had increased drain currents, likely due to an increased number of gate structures and W/L ratio. R_{ON} is measured from I_{DS}-V_{DS} plot at V_{GS} = 14 V, I_D = 20 A and increased R_{ON} of trench and double trench can be attributed to smaller area compared to planar device. We investigated the non-linear capacitance (Fig. 2c) between the source (S), gate (G), and drain (D) terminals, such as gate-to-source capacitances (C_{gs}) and reverse transfer/miller capacitances (C_{gd}) with gate bias. Device C C_{gd} showed multiple humps due to variation in semiconductor capacitance with interface trapped charge (D_{it}). Device C also exhibited lower C_{gs}, indicating tight control over gate-to-source overlap as minority carriers do not build up from the source with positive bias in the p-base region. We measured non-linear charges, including input charge (Q_{gs}), Miller plateau (Q_{gd}), and total gate charge (Q_g), which matched the non-linear capacitances and impacted the drain voltage and current switching transitions (Fig. 3). Although Device C exhibited lower changes in gate charge with case temperature, the amount of gate charge was higher compared to Device A and Device B due to increased implanted p-base doping for Q_{gs} and trapped charges near the interface states towards the gate bottom for Q_{gd}. Furthermore, the switching loss characteristics of the devices were evaluated at temperatures ranging from 25°C to 125°C using the DPT platform. Switching losses were assessed using a clamped

inductive load of 1 mH with test conditions of V_{dd} = 800 V and I_d = 30 A for the three devices along with a gate drive resistance of 10 Ω [4].

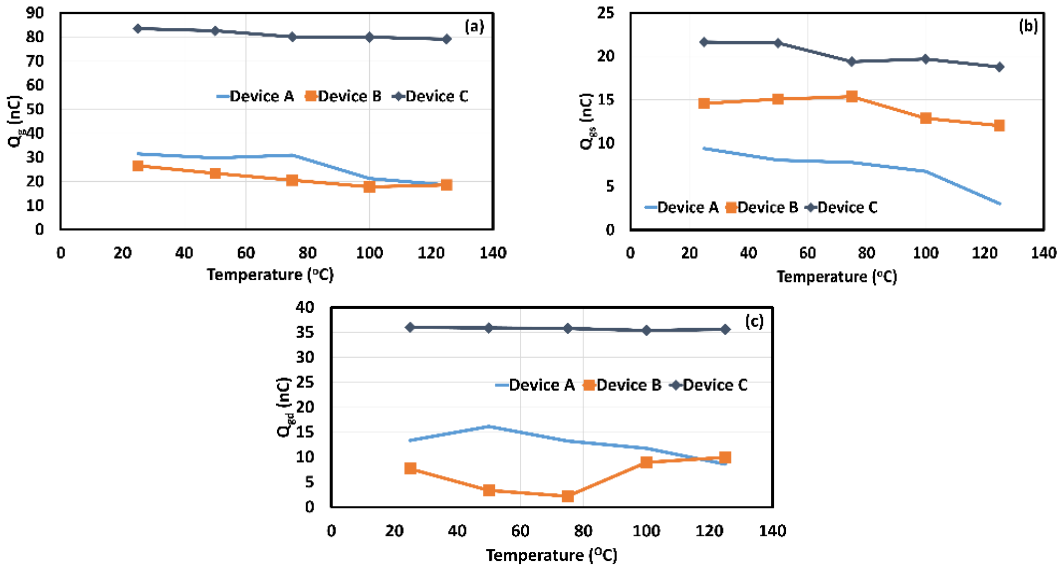

Fig. 3. Measured (a) gate charge, (b) gate-to-source, (c) gate-to-drain charge of each gate structure with the temperature ranging from 25^{O} C to 125^{O} C.

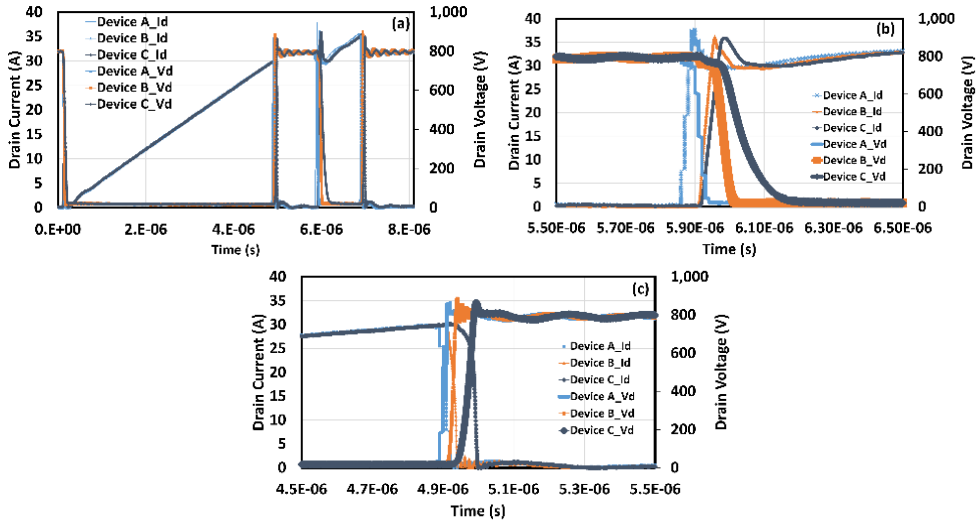

Fig. 4. Measured (a) double pulse test characteristics with (b) turn-on and (c) turn-off switching waveforms of three gate structure of 1.2 kV SiC MOSFET with the clamped inductive load at 25^{O} C.

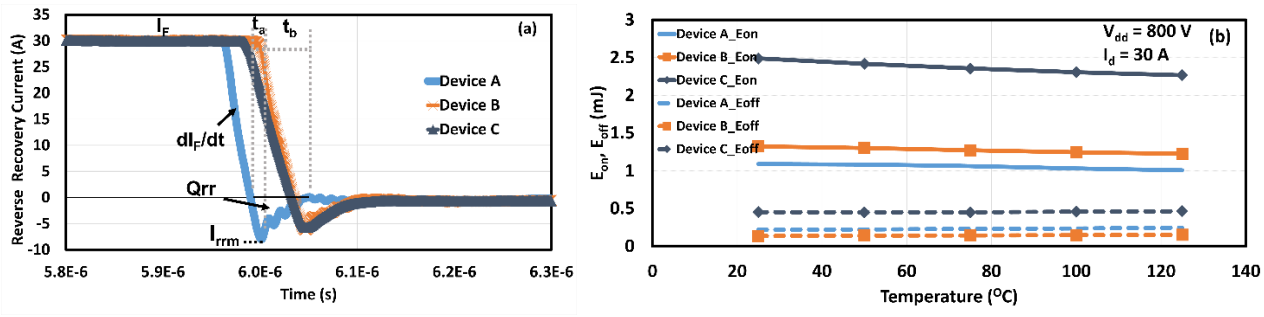

Fig. 5. Measured (a) reverse recovery characteristics and (b) turn-on and turn-off switching losses of three gate structures including reverse recovery loss while varying the case temperature from 25^{O} C to 125^{O} C.

The initial pulse in double pulse waveforms were used to set up the drain current of 30 A (Fig. 4a) to evaluate the turn-on (Fig. 4b), and turn-off (Fig. 4c) characteristics. Switching waveforms were used to estimate the switching losses with overlapping area of drain voltages and currents during turn-on and turn-off. Device C exhibited increased switching losses with reduced slope of switching transitions, probably due to the trapping of charge carriers with increased interface trap density in the channel and at SiC/SiO_2 interface around the trench gate corner. The reverse recovery characteristics (Fig. 5a) demonstrated the influence of the gate structure on the p-body area (channel length and depth) and doping profile, as well as on the minority carrier injection mechanism of the parasitic P-N body diode [5]. The switching transition losses of the three devices, including reverse recovery, showed that Device C exhibited increased switching losses at all temperatures (Fig. 5b). Table 1 lists summarize all the reverse recovery parameters, including peak reverse recovery current (I_{rrm}), reverse recovery energy (E_{rr}), reverse recovery charge (Q_{rr}), reverse recovery time ($t_{rr} = t_a + t_b$), and forward current to peak reverse current transition rate (dI_F/dt). Device C exhibited lowest I_{rrm} of 5.7 A among three devices with a reduced switching transition rate of 590 A/µs. Lower reverse recovery characteristics can be attributed to reduced effective p-base area with the increased shielding from double trenches towards the p-base and trench bottom. These findings contribute to understanding the potential of 1.2 kV 4H-SiC MOSFETs with different gate structures and can be valuable for optimizing device performance in various applications. This underscores the impact of gate structure on the switching loss characteristics of the devices. A comprehensive discussion of the implications of the above findings and the advantages of planar and trench SiC MOSFETs in power applications for the next generation of electric vehicles are explored in this work.

Table 1. Temperature dependent reverse recovery characteristics of three devices

T (^{O}C)	Type	I_{rrm} (A)	E_{rr} (µJ)	Q_{rr} (nC)	t_{rr} (ns)	t_a (ns)	t_b (ns)	dI_F/dt (A/µs)
25	Device A	7.95	39.63	192	49.86	11.22	38.64	969
	Device B	6.12	40.93	191	68.6	12.11	56.49	706
	Device C	5.71	22.39	206	69.87	14.38	55.48	590
50	Device A	7.84	40.99	196	50.65	11.17	39.47	972
	Device B	6.48	45.08	214	68.35	12.67	55.67	703
	Device C	5.73	20.23	194	67.02	14.75	52.26	590
75	Device A	7.86	45.9	208	53.14	11.25	41.88	972
	Device B	7.12	51.08	261	66.42	14.01	52.4	702
	Device C	5.69	22.42	198	71.45	14.4	57.05	590
100	Device A	8.00	53.85	234	58.39	11.37	47.01	972
	Device B	8.05	58.9	320	66.73	17.48	49.24	695
	Device C	5.78	27.86	219	78.29	14.64	63.65	590
125	Device A	8.21	64.66	269	61.38	11.9	49.48	972
	Device B	9.19	69.04	387	68.58	19.21	49.36	693
	Device C	5.75	31.98	230	83.92	14.38	69.54	593

Summary

In summary, this study presents a comprehensive analysis of 4H-Silicon Carbide (SiC) MOSFETs with distinct gate structures. Through an examination of key parameters, non-linear charges, and switching losses across temperature ranges, we have identified performance variations. These findings offer critical insights for optimizing SiC MOSFETs, particularly in electric vehicle applications, where efficiency and temperature stability are vital. Our research contributes to the advancement of power electronics, emphasizing the importance of tailored SiC MOSFET designs for enhanced performance and energy efficiency.

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