# Excellent Avalanche Capability in SiC Power Device with Positively Beveled Mesa Termination

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**Keywords:** power device, silicon carbide, avalanche capability, beveled mesa termination.

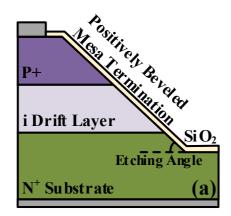
**Abstract.** In this work, 4H-SiC p-i-n diodes with excellent single-pulse avalanche energy density (EAS) with positively beveled mesa termination have been demonstrated. The fabrication of this junction termination extension (JTE) obviates ion implantation and requires only etching process. With its uniform electric field and temperature distribution, the fabricated 4H-SiC p-i-n diodes show breakdown voltage (BV) of 886V (98.4% of the parallel-plane limit) and the inductive avalanche energy density of ~10.4J/cm²@1mH. Meanwhile, ruggedness of the avalanche breakdown has also been evidently promoted. The results confirm that this structure exhibits great capability potential in power applications.

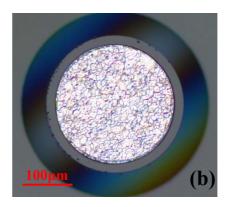
#### Introduction

As silicon-based power devices are approaching their theoretical limits, research concern is now focused on the development of alternative materials [1]. SiC material, with its superior properties of high breakdown field and high thermal conductivity, is a prominent material for power device. And the SiC power device has been widely used in many applications [2]-[5].

For the high-power device, avalanche shock is one of the most extreme operational conditions, which may arise when devices work under highspeed switching [6]-[7]. Therefore, this phenomenon imposes high requirements on the termination of the device. Considering design, process convenience and area economy, JTE termination is one of the most widely used termination technologies for SiC-based power devices. But there are still some problems with JTE terminals, such as charge sensitivity and the concentration of electric field at the edge. Among them, orthogonal positive-bevel-edge termination technique has been proposed to produce symmetric blocking structures in SiC [8] due to its significant savings in chip area, superior terminal efficiency and the uniform electric field distribution. Recent years, Kai-Wen Nie., et al., verify the highly enhanced inductive current sustaining capability and avalanche ruggedness during unclamped inductive switch (UIS) tests in GaN PiN power diodes with this termination [9]. However, there has been no report of the avalanche capability associated with SiC power devices using beveled mesa termination technology. Thus, the avalanche capability of such devices is yet to be demonstrated and explored.

In this article, the 4H-SiC p-i-n diodes with positively beveled mesa termination were fabricated. First, the process and fundamental properties of this device were demonstrated. Then, the single-pulse avalanche energy capability of this device was verified in UIS tests. The effects of the terminal design on the avalanche current capability are discussed with simulation study. Finally, a comparison of avalanche capability with reported power devices is performed, and the results show that SiC devices with this structure have greater advantages in power electronics system applications.





**Fig. 1.** (a) the schematic cross section of the fabricated 4H-SiC p-i-n diode with positively beveled mesa termination. and (b) The optical microscope view of a fabricated 4H-SiC p-i-n diode.

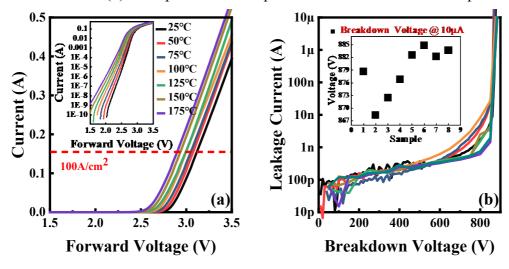


Fig. 2. (a) The forward characteristics at different temperature and (b) the reverse breakdown characteristics of this device.

## **Device Fabrication and Basic Characteristics**

Fig. 1(a) shows the schematic cross section of our fabricated 4H-SiC p-i-n diode fabricated on a 6μm 4H-SiC drift layer, which was continuously grown on a heavily nitrogen-doped *N*+ type 4H-SiC substrate by chemical vapor deposition. High surface injected *p*<sup>+</sup> region to ensure formation of anode ohmic contact. After the implantation, 1650 °C high-temperature post annealing process with 100-nm C film protective capping layer is conducted to activate impurities and remove implantation damage. The mesa structure was fabricated by our proposed improved Bosch etching process [11] using a low-damage inductive coupled plasma (ICP) etching system. With the optimal etching process, positively beveled mesa termination with smooth sidewall was fabricated as shown in Fig. 1(b). A SiO<sub>2</sub> passivation layer was formed by the plasma-enhanced chemical vapor deposition (PECVD). Then, the anode and cathode were formed by sputtering Ni/Ti/Al and Ni/Ti/Ag, respectively. Finally, followed with annealing process in a N<sub>2</sub> atmosphere at 1000°C for 3 mins to form the ohmic contact.

On-wafer forward I-V measurement are performed using an Agilent B1505A analyzer. Fig. 2(a) illustrates the temperature dependence of forward I-V curve of the fabricated device with an active anode area of  $0.16 \text{mm}^2$ . A forward voltage drop is 3.4 V corresponding to a current density of  $200 \text{A/cm}^2$  and a differential on-resistance of  $2.28 \ m\Omega \cdot cm^2$  at room temperature. The turn-on voltage and forward voltage drop at  $100 \text{A/cm}^2$  of SiC p-i-n rectifier are 2.75 and 3.15 V at room temperature. Due to the SiC band gap narrowing with temperature results in the increase of carrier

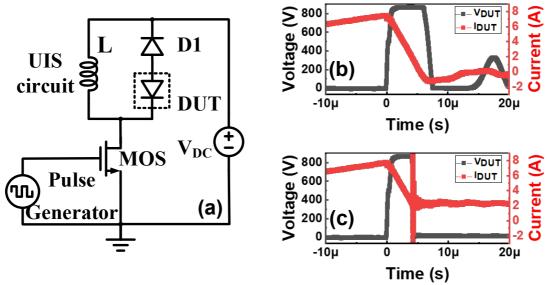


Fig. 3. (a) The basic UIS tests circuit, where L the load inductor, D1 is the Schottky diode to prevent the error turning-on of DUT. (b) The typical voltage and current waveform and (c) the failure voltage and current waveform captured from DUT during the UIS test.

<b>Table I.</b> The com	parison	of avalance	he performan	ices in UIS	tests with	different	power rectifiers

Power diode	Drift layer thickness (µm)	Breakdown Voltage(V)	Peak current (A)	EAS(J/cm <sup>2</sup> )
GaN PiN [10]	>6	1200	7.86	1.5@1mH
GaN PiN [9]	2.5	714	5.68	5.5@1mH
SiC MPS [13]	>6	~2100	10.2	5.9@1mH
SiC MPS [14]	>6	1650	9.1	6.8@3mH
SiC JBS [15]	>6	1600	5.4	6.8@3mH
SiC PiN(this work)	6	961	7.7	10.4@1mH
	6	864		12.6@3mH

lifetime with temperature [12]. The maximum change of forward voltage drop is less than 0.2V at 25°C to 175°C indicates the fabricated devices have good robustness against high temperatures.

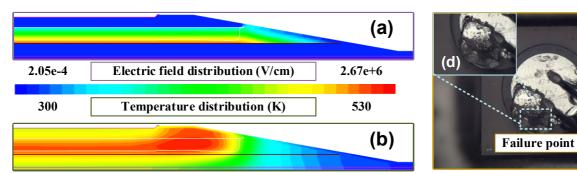
Fig. 2(b) shows the typical breakdown voltage curves of eight devices. It can be seen that the leakage current is less than 10nA at 800V. The inset of Fig. 2(b) shows the breakdown voltage of device at  $10\mu A$ , and it is found that the maximum breakdown voltage is 886V, which is close to 98.4% of the ideal parallel-plane breakdown voltage. These results confirm the stability and high efficiency of the fabricated device terminal.

### **Experimental Results and Discussion**

To evaluate the avalanche capability of the device, the device was validated using the UIS system. Fig. 3(a) shows the basic UIS tests circuit. With a commercial SiC MOSFET (BV<sub>mos</sub>>BV<sub>DUT</sub>) switched from on to off state, energy discharging from the inductor (L) would generate an intense current through the DUT. Fig. 3(b) present the typical voltage and current waveforms captured from single-pulse UIS tests, representing an avalanche breakdown event in the SiC p-i-n diode. With a load inductor of 1mH, and change the MOSFET on-state time, the transient signal exhibits peak voltage of 867V and peak current of 7.7A. As the peak current increases, the DUT has shorted out and becomes a criterion for device failure [13], is shown in Fig. 3(c). Therefore, the EAS can be calculated by the following equation:

$$EAS = \int_0^{tava} V_d(t) J_d(t) dt \tag{1}$$

where  $V_d$  is the diode avalanche voltage,  $J_d$  is the diode avalanche current density, and tava is the avalanche duration.



**Fig. 4**. (a) The distribution of the electric field and (b) the temperature in device during the UIS test. (c) The position of the failure point when the device damaged. (d) Topography near the failure point.

According to the equation, a high single-pulse avalanche energy density of 10.4J/cm<sup>2</sup> was realized given the diodes area of 0.16mm<sup>2</sup>. Table I summarizes the representative parameters of some reported diodes [9], [10], [13], [14], [15]. It is evident that with positively beveled mesa termination structure the EAS are significantly increased. To our knowledge, this is the excellent EAS data for 4H-SiC power rectifiers, even better than other materials.

To further discuss the reasons for the advantaged by this structure, the simulations of 2D-electric field and temperature distributions of the fabricated diodes when the avalanche process occurs are shown in Fig. 4(a) and 4(b). The electric field of the device is uniformly distributed in the body which effectively prevents the concentration of the electric field at the edge of the device. Meanwhile, heat is also uniformly distributed in the body, this prevents the device from burning out due to localized overheating. Fig. 4(c) and 4(d) are microscopic image of the failure device. Compared with the simulation results, it can be found that the failure of the device occurs at the boundary of the active region and the oxide layer. This provides favorable evidence for the designers to design more efficient avalanche protection power devices.

Combined experimental and simulated failure analysis, considering the simple fabrication process, this structure reported here showed great potential in achieving high-performance SiC power rectifier for high-avalanche-capability SiC power applications.

# **Summary**

In this article, high-performance 4H-SiC p-i-n diodes with positively beveled mesa termination have been demonstrated. With the help of experiments and technology computer-aided design simulations, the UIS behaviors of this device are discussed in detail, which intends to help engineers improve the device designing. Due to the uniform voltage and temperature distributions of this structure, the device presents excellent breakdown characteristic and single-pulse avalanche energy capability. Thus, this structure has great potential for SiC power rectifiers, especially for high-avalanche-capability power applications.

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