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Comparison of Si CMOS and SiC CMOS Operational Amplifiers

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Abstract. In this study, we numerically compare the characteristics of Si and SiC CMOS operational amplifiers (OpAmp) using LTspice. According to prior researches, we set the device parameters for Si and SiC MOSFETs. The OpAmp consists of three stages: the input stage, the gain stage, and the output stage. We established three criteria for the OpAmp's operation: (1) a unity gain frequency of 1MHz, (2) an open-loop gain of at least 75dB, and (3) a phase margin of more than 60° when a load capacitance is 300pF. To achieve a unity gain frequency of 1MHz, we adjusted the values of the resistor and capacitor used for phase compensation. The supply voltage was set to be ±5V for the Si OpAmp and ±15V for the SiC one. Our numerical analysis of the frequency response shows that the Si OpAmp met all three criteria. In contrast, the SiC OpAmp, when faced with a load capacitor of 300pF, had a phase margin of 43.4°, falling below the 60° mark. For the SiC OpAmp, the frequency response declined rapidly when the supply voltage dropped to 10V or below.

Introduction

Silicon carbide (SiC) integrated circuits (ICs) are highly capable of withstanding harsh environments owing to their superior tolerance for heat and radiation. There are studies on SiC ICs based on BJTs [1], JFETs [2] and MOSFETs [3]. Among them, SiC CMOS ICs are quite attractive since silicon (Si) CMOS ICs are dominant in the field of both analog and digital circuits. Thus, it is interesting to clarify how much properties of SiC CMOS ICs can be obtained by using currently available SiC n-type and p-type MOSFETs although their channel mobilities are much lower than those of Si MOSFETs.

In this study, we utilized LTspice to numerically assess the features of Si and SiC CMOS operational amplifiers (OpAmp). We determined the device parameters for Si and SiC MOSFETs based on previous studies. The OpAmp is structured in three phases: input, gain, and output. We outlined three performance metrics for the OpAmp: (1) a 1MHz unity gain frequency, (2) a minimum open-loop gain of 75dB, and (3) a phase margin exceeding 60° when subjected to a 300pF load capacitance. To realize the 1MHz unity gain frequency, we tweaked the resistor and capacitor values meant for phase compensation. We designated a supply voltage of ±5V for the Si OpAmp and ±15V for its SiC counterpart. Our data analysis on the frequency response indicated that the Si OpAmp satisfied all three set metrics. On the other hand, the SiC OpAmp, when loaded with a 300pF capacitor, registered a phase margin of 43.4°, which is below the set 60° standard. Notably, the frequency response for the SiC OpAmp deteriorated significantly when its supply voltage reduced to 10V or less.

Si MOSFET vs. SiC MOSFET

The transconductance of MOSFET at the saturation region is given by

$$g_m = \mu C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_T) \tag{1}$$

where μ is the channel mobility, C_{ox} the gate capacitance, W the gate width, L the gate length, V_{GS} the gate-source voltage, and V_T the threshold voltage, respectively. Table 1 shows the main device parameters of Si and SiC MOSFETs according to Ref. [4] and [3]. Note that the channel mobilities of n- and p-type SiC MOSFETs are an order of magnitude smaller than those of Si counterparts. Additionally, SiC MOSFETs, which have an oxide film thickness twice that of Si MOSFETs, possess

Table 1: Main MOSFET parameters

Parameters	Symbol	[Unit]	Si NMOS	Si PMOS	SiC NMOS	SiC PMOS
Threshold voltage	V_T	[V]	0.8	-0.85	5.6	-9.5
Channel mobility	μ	[cm^2/Vs]	500	180	18.5	3.6
Oxide thickness	t_{ox}	[nm]	27	27	52	52

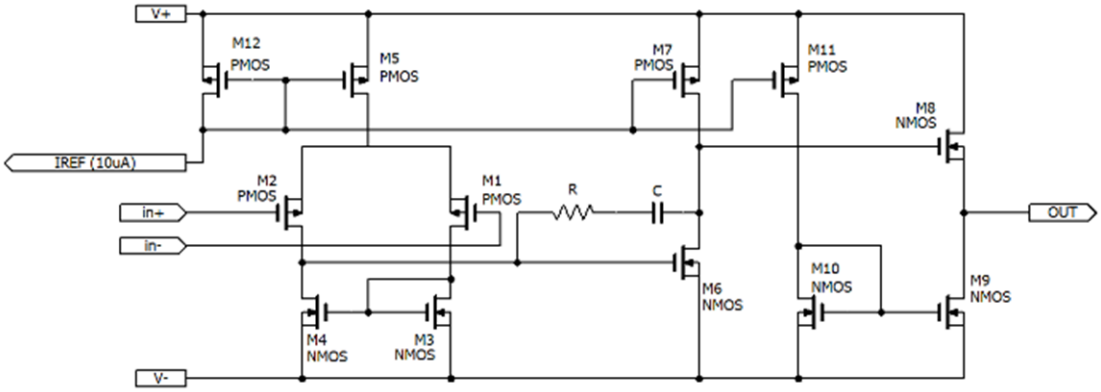

Fig. 1: Internal circuit of an OpAmp. The OpAmp consists of a PMOS input differential amplifier, a NMOS source-grounded gain stage, and a NMOS source follower output buffer.

a larger gate threshold voltage. This contributes to the need for higher supply voltages in SiC integrated circuits. We use NMOS4 and PMOS4 models for LTspice simulation.

Operational Amplifier

Figure 1 shows the internal circuit of an operational amplifier (OpAmp) [4]. The OpAmp consists of a PMOS input differential amplifier, a NMOS source-grounded gain stage, and a NMOS source follower output buffer. The characteristics are tuned by changing the reference current value (I_{REF}) and the constants of the phase compensation circuit C and R. We set the following design criteria [4]: (1) the open-loop gain is larger than 75dB, (2) the unity gain frequency is about 1MHz, and (3) the phase margin, the difference between the phase shift value and $-180°$ at the unity gain frequency, is larger than 60° when a 300pF load capacitance was connected. Table 2 shows the MOSFET size parameters for Si and SiC OpAmps. In SiC MOSFETs, increasing the W/L ratio and, in some cases, increasing the number of used elements (M) help suppress the decrease in transconductance caused by the lower mobility. In order to obtain the 1MHz unity gain frequency, the resistance and capacitance for phase compensation are set to be $R = 2$ kΩ and $C = 15$ pF for Si OpAmp while they are $R = 10$ kΩ and $C = 1.0$ pF for SiC one. The supply voltage is ± 5V for Si OpAmp and ± 15V for SiC one.

Frequency Response

We numerically compare the characteristics of Si and SiC CMOS OpAmps using LTspice. The frequency response of OpAmp is evaluated in the circuit with a 1kΩ load resistor and a load capacitor, whose capacitance is 0, 50, 100, or 300pF (Fig. 2). Figure 3 shows the Bode plot for Si CMOS OpAmp with different load capacitances (green: 0pF, blue: 50pF, red: 100pF, light blue: 300pF). The open-loop gain is 96.6dB and the unity gain frequency is independent on the load capacitance. The phase margin decreases as the load capacitance increases. Still, it is larger than 60° when a 300pF load capacitance is connected. We summarize output characteristics in Table 3.

Table 2: MOSFET size parameters of Si and SiC OpAmps

FET No.	Type	Si		SiC		Comments
		W/L	Multiplier M	W/L	M	
M1	p	$20\mu/5.0\mu$	4	$20\mu/2.5\mu$	5	V_{in}^-
M2	p	$20\mu/5.0\mu$	4	$20\mu/2.5\mu$	5	V_{in}^+
M3	n	$20\mu/2.5\mu$	2	$20\mu/2.5\mu$	2	
M4	n	$20\mu/2.5\mu$	2	$20\mu/2.5\mu$	2	
M5	p	$12\mu/2.5\mu$	6	$20\mu/2.0\mu$	12	30μA
M6	n	$32\mu/2.0\mu$	14	$32\mu/2.0\mu$	14	gain stage
M7	p	$12\mu/2.5\mu$	42	$20\mu/2.0\mu$	84	210μA
M8	n	$32\mu/2.1\mu$	40	$64\mu/2.0\mu$	65	buffer
M9	n	$12\mu/2.5\mu$	54	$12\mu/2.5\mu$	54	700μA
M10	n	$12\mu/2.5\mu$	6	$12\mu/2.5\mu$	4	50μA
M11	p	$12\mu/2.5\mu$	10	$20\mu/2.0\mu$	20	50μA
M12	p	$12\mu/2.5\mu$	2	$20\mu/2.0\mu$	4	10μA (I_{REF})

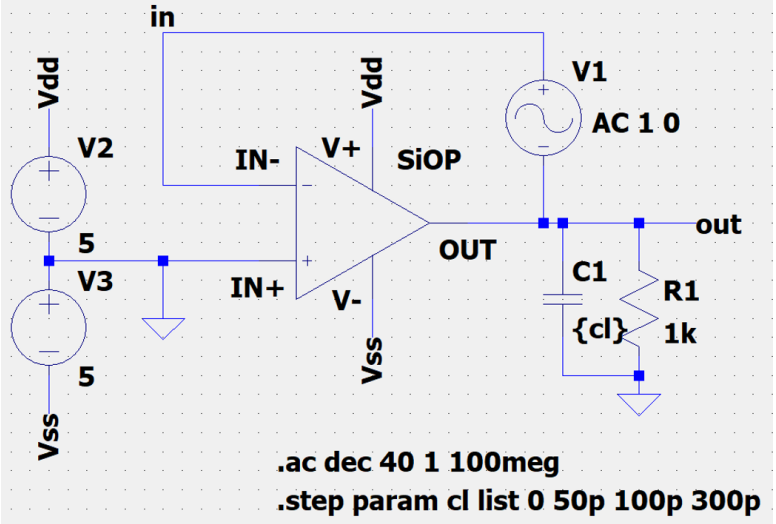

Fig. 2: OpAmp evaluation circuit with a 1kΩ load resistor and a load capacitor, whose capacitance is 0, 50, 100, or 300pF.

Figure 4 shows the Bode plot for SiC CMOS OpAmp with different load capacitances. The open-loop gain is 93.6dB. The unity gain frequency reduces to 0.86MHz when a load capacitance is 300pF. The phase margin decreases as the load capacitance increases, and it is smaller than 60° when a 300pF load capacitance is connected. Results are summarized in Table 4. Next we investigate the effect of supply voltages. Figure 5 shows the Bode plot for SiC CMOS OpAmp with different supply voltages (green: ±7.5V, blue: ±10V, red: ±12.5V, light blue: ±15V). The load capacitance is 0pF. The frequency response of gain and phase shift are nearly the same for the supply voltage is ±12.5V and ±15V. On the other hand, the criteria for the unity gain frequency 1MHz is no longer satisfied when the supply voltage is less than ±10V. It is thought that the problem arises when one of the MOSFETs in the circuit deviates from the saturation region.

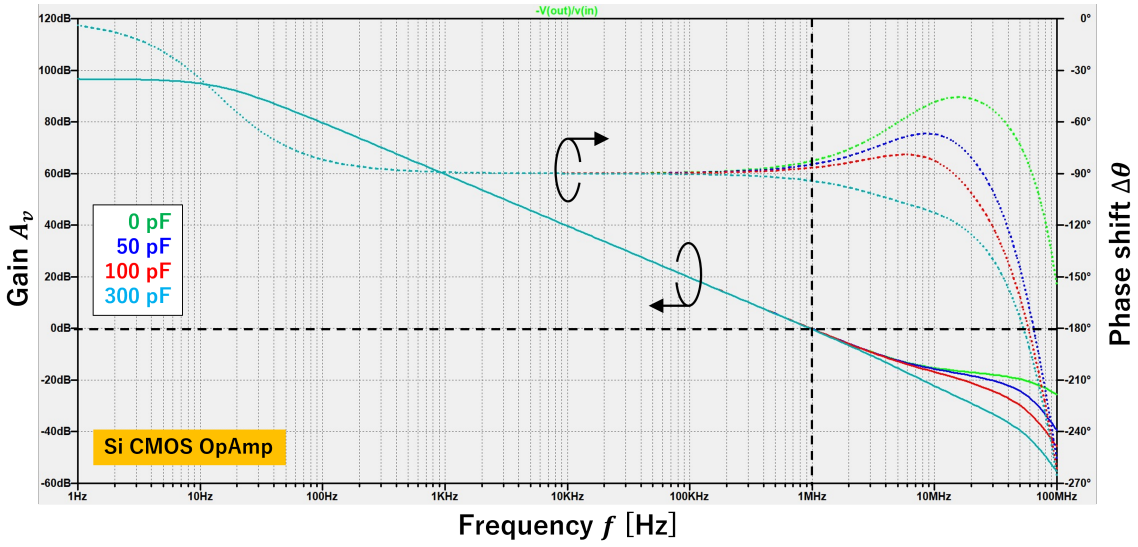

Fig. 3: Bode plot for Si CMOS OpAmp with different load capacitances (green: 0pF, blue: 50pF, red: 100pF, light blue: 300pF). Solid and dotted lines are corresponding to the gain (left axis) and phase shift (right axis), respectively. The supply voltage is ±5V.

Table 3: Output characteristics for Si CMOS OpAmp

Load capacitance [pF]	Open-loop gain [dB]	Unity gain frequency [MHz]	Phase margin [degree]
0	96.6	0.98	97.2
50	96.6	0.98	95.2
100	96.6	0.98	93.3
300	96.6	0.96	85.9

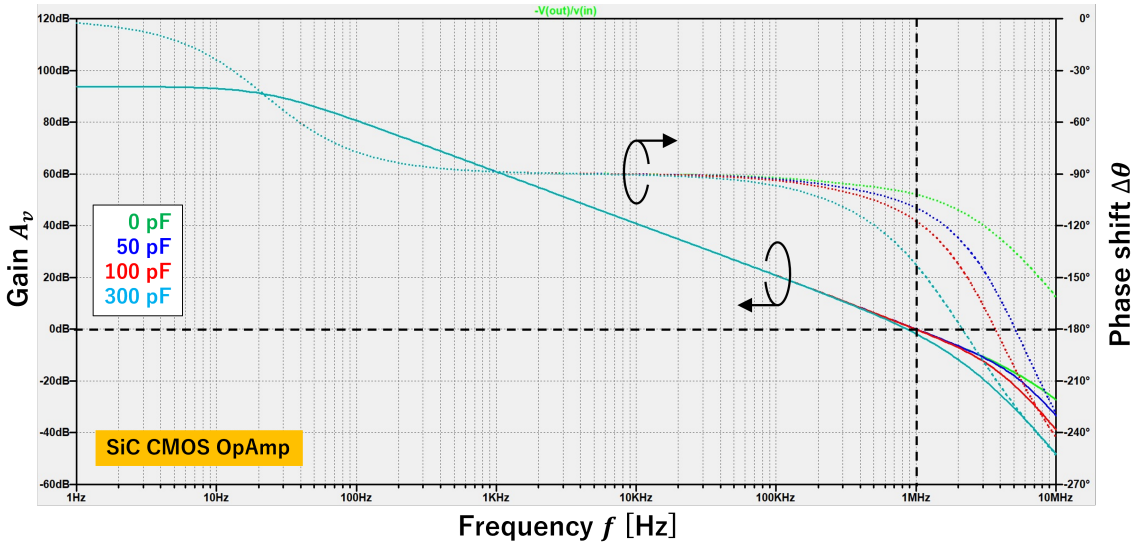

Fig. 4: Bode plot for SiC CMOS OpAmp with different load capacitances (green: 0pF, blue: 50pF, red: 100pF, light blue: 300pF). Solid and dotted lines are corresponding to the gain (left axis) and phase shift (right axis), respectively. The supply voltage is ±15V.

Table 4: Output characteristics for SiC CMOS OpAmp

Load capacitance [pF]	Open-loop gain [dB]	Unity gain frequency [MHz]	Phase margin [degree]
0	93.6	1.0	78.1
50	93.6	1.0	70.4
100	93.6	0.99	63.0
300	93.6	0.86	43.4

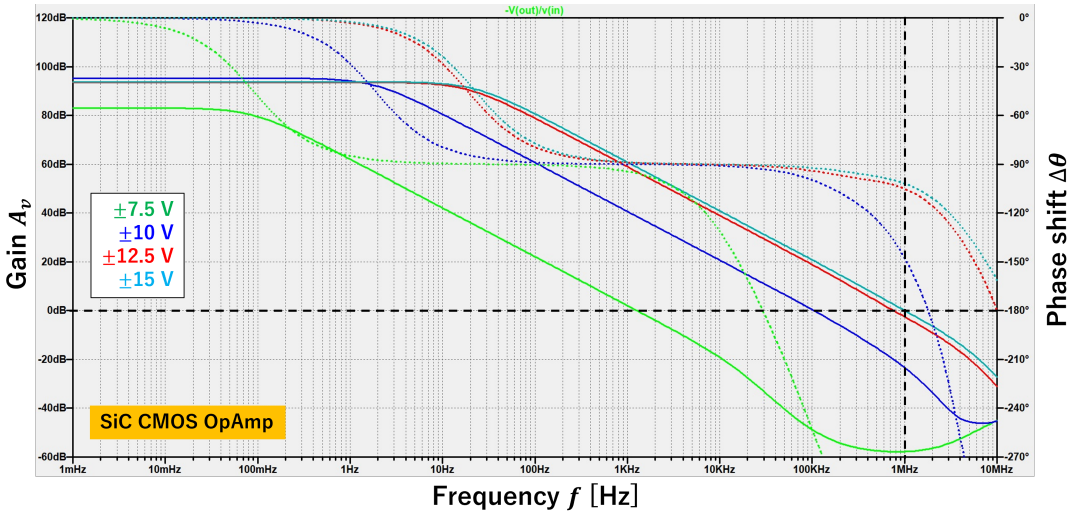

Fig. 5: Bode plot for SiC CMOS OpAmp without a load capacitor at different supply voltages (green: ±7.5V, blue: ±10V, red: ±12.5V, light blue: ±15V). Solid and dotted lines are corresponding to the gain (left axis) and phase shift (right axis), respectively.

Summary

In this study, we numerically compare the characteristics of Si and SiC CMOS operational amplifiers (OpAmp) using LTspice. According to prior researches, we set the device parameters for Si and SiC MOSFETs. The OpAmp consists of three stages: the input stage, the gain stage, and the output stage. We established three criteria for the OpAmp's operation: (1) a unity gain frequency of 1MHz, (2) an open-loop gain of at least 75dB, and (3) a phase margin of more than 60° when a load capacitance is 300pF. To achieve a unity gain frequency of 1MHz, we adjusted the values of the resistor and capacitor used for phase compensation. The supply voltage was set to be ±5V for the Si OpAmp and ±15V for the SiC one. Our numerical analysis of the frequency response shows that the Si OpAmp met all three criteria. In contrast, the SiC OpAmp, when faced with a load capacitor of 300pF, had a phase margin of 43.4°, falling below the 60° mark. For the SiC OpAmp, the frequency response declined rapidly when the supply voltage dropped to 10V or below.

References

[1] M. Shakir *et al.*: Electronics vol. 8 (2019), p. 496.

[2] M. Krasowski and P. Neudeck: NASA/TM-20210000735 (2021), p. 1.

[3] T. Liu *et al.*: IEEE J. Ele. Dev. Soc. vol 10 (2022), p. 129.

[4] H. Yoshida: *Practical design of CMOS analog IC* (CQ Publishing, Japan, 2010) (in Japanese).