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Comparative Performance Evaluation of High-Voltage Bidirectional, Conventional and Superjunction Planar DMOSFETs in 4H-SiC

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Abstract. We quantitively compare the static and dynamic performance for high-voltage SiC bidirectional (BD) conventional and superjunction (SJ) DMOSFETs by using 3D TCAD simulations. We extract the specific on-resistance ($R_{ON,sp}$) and the total specific switching charge ($Q_{T,sp}$), which is a sum of the specific gate charge ($Q_{G,sp}$) and drain charge ($Q_{DS,sp}$) to quantify both the static and switching characteristics respectively. We also develop a new Figure-of-Merit (FoM), which is the product of $R_{ON,sp}$. $Q_{T,sp}$, to evaluate the overall performance. We show that the high-voltage 4H-SiC BD SJ DMOSFET has the best FoM with substantial (>58%) improvement, compared to the BD conventional DMOSFETs, which increases with increasing breakdown voltage.

Introduction

4H-SiC is superior to silicon in power devices due to its better electrical and material properties, such as x10 higher critical field, enabling high-voltage devices with a significant (~1000 times) reduction in on-state resistance. Also, superjunction (SJ) devices offer a better trade-off between specific on-resistance and breakdown voltage ($R_{ON,sp} \propto BV$) compared to conventional devices ($R_{ON,sp} \propto BV^{2.5}$). Bidirectional (BD) or AC switches are beneficial in many power applications, such as, PV systems [1], and matrix converters [2], reducing system complexity, size, and cost. In this paper, we comparatively evaluated the performance of high-voltage 4H-SiC BD conventional and SJ DMOSFETs.

BD power MOSFETs or AC power transistor switches can be physically realized using several ways [3]. One way is to connect two power MOSFETs in either common-drain or common-source configuration. Common-source configuration has an advantage over common-drain in having the same gate driver for both MOSFETs, but it adds packaging challenges. Here, we adopt the common-drain configuration as it is more physically feasible, yet it introduces some circuit complexity, where the gates must have their own gate driver because they are referenced to their corresponding source terminal as depicted in Fig. 1a [4].

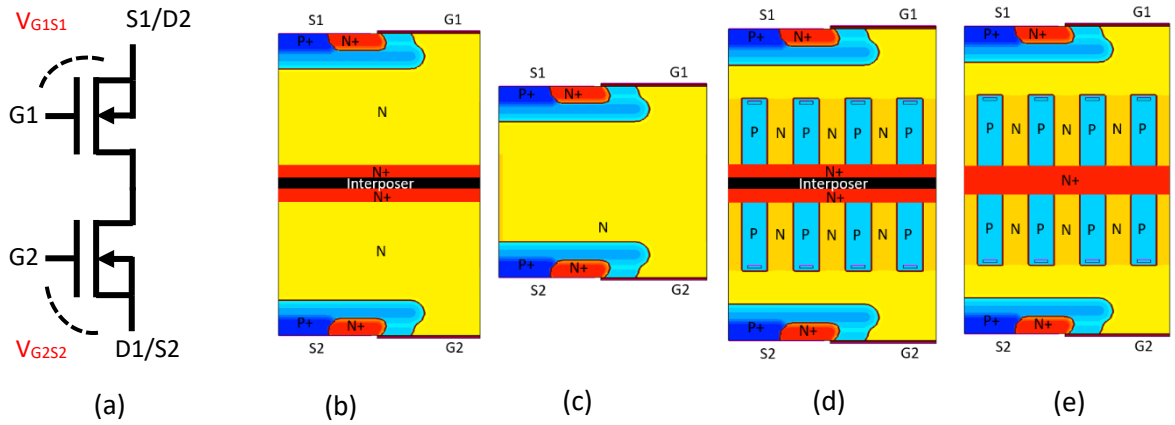

Fig. 1. (a) Circuit schematic of a bidirectional (BD) MOSFET switch. Half-cell schematic cross-sections for BD DMOSFETs with different configurations: (b) hybrid conventional, (c) monolithic (shared-drift-region) conventional, and (d) hybrid superjunction (SJ), and (e) monolithic (non-shared-drift-region) SJ DMOSFETs.

Simulation Design

In this paper, we simulated BD conventional and SJ 4H-SiC DMOSFETs using a 3-dimensional TCAD device simulator (Sentaurus). As depicted in Fig. 1b and 1d, the hybrid BD DMOSFETs have an interposer layer between two MOSFETs that are connected drain-to-drain. In this configuration and during the off state, the MOSFET whose V_{DS} is lower, blocks the voltage. For the monolithic configuration, the monolithic conventional MOSFET has only one drift region that blocks the voltage at both directions (sharing drift region) because it acts as open based PNP. However, the monolithic SJ conventional MOSFETs has two drift regions and cannot block the voltage using only one drift region (non-sharing drift region) because the P-pillars are connected to the P-body and without the N+ field-stopping layer the current will flow in the off state. Accordingly, we explore the hybrid configuration (Fig. 2d) for 1.2 to 10kV BD SJ DMOSFETs comparing it schematically with monolithic and hybrid conventional DMOSFETs as shown in Fig. 1.

The BD conventional DMOSFETs structural parameters are calculated from the parallel-plane design [5], while the BD superjunction DMOSFETs is designed from the critical breakdown field estimation [6] by using the pillar performance limit [7].

Results

The specific on-resistance ($R_{ON,sp}$) was extracted numerically using Sentaurus TCAD assuming the baseline structure cell pitch of 6 μm, quantifying the static performance for all MOSFETs at all BV ratings. Compared to the hybrid BD conventional DMOSFET, the hybrid BD SJ DMOSFET exhibits a 33% (up to 98% at 10kV) reduction in $R_{ON,sp}$, but to the monolithic conventional DMOSFET, it has a 15% (up to 96% at 10kV) better $R_{ON,sp}$. At lower BV ratings, the channel resistance dominates that is why the percentage is small compared to high BV ratings where the drift region resistance dominates which has a better trade-off ($R_{ON,sp} \propto BV$ instead of $R_{ON,sp} \propto BV^{2.5}$) between $R_{ON,sp}$ and BV as depicted in Fig. 2.

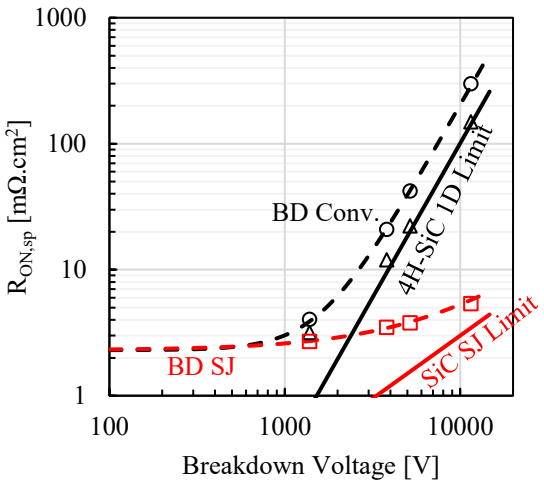

Fig. 2. $R_{ON,sp}$ and BV trade-off for monolithic BD conv. (Triangle), Hybrid-BD conv. (Circle) and Hybrid-BD SJ DMOSFETs (Square)

For the dynamic performance, the specific gate charge $Q_{G,sp}$ and the specific drain-to-source charge $Q_{DS,sp}$ are extracted numerically from the simulation using a resistive load circuit. $Q_{G,sp}$ has been calculated by integrating the gate current i_G over turn-on (or turn-off), while $Q_{DS,sp}$ has been calculated by integrating drain current I_{DS} over turn-on and turn-off times. It was found that hybrid BD SJ DMOSFET has 10% and 73% reduction in $Q_{G,sp}$ and $Q_{DS,sp}$ respectively compared to its conventional counterparts as illustrated in Fig. 3. The substantial reduction in $Q_{DS,sp}$ in the SJ DMOSFET is due to the abrupt change in the drift depletion capacitance with increasing drain bias from rapid initial lateral depletion of the pillars.

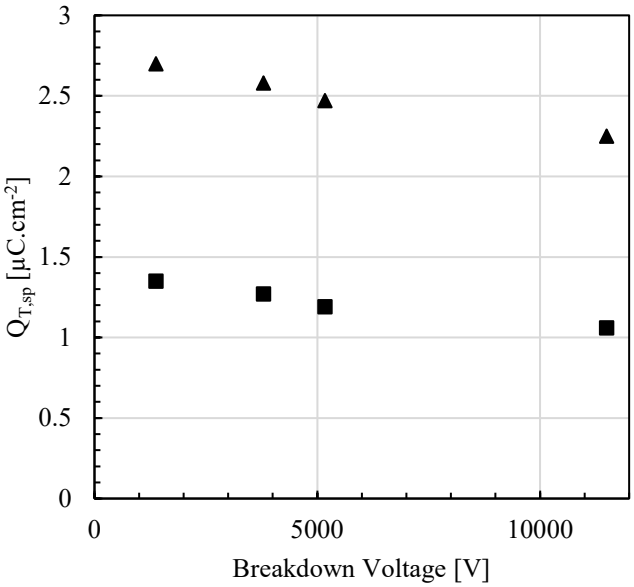

Fig. 3. $Q_{T,sp}$ for monolithic BD conv. (Triangle), and Hybrid-BD SJ DMOSFETs (Square)

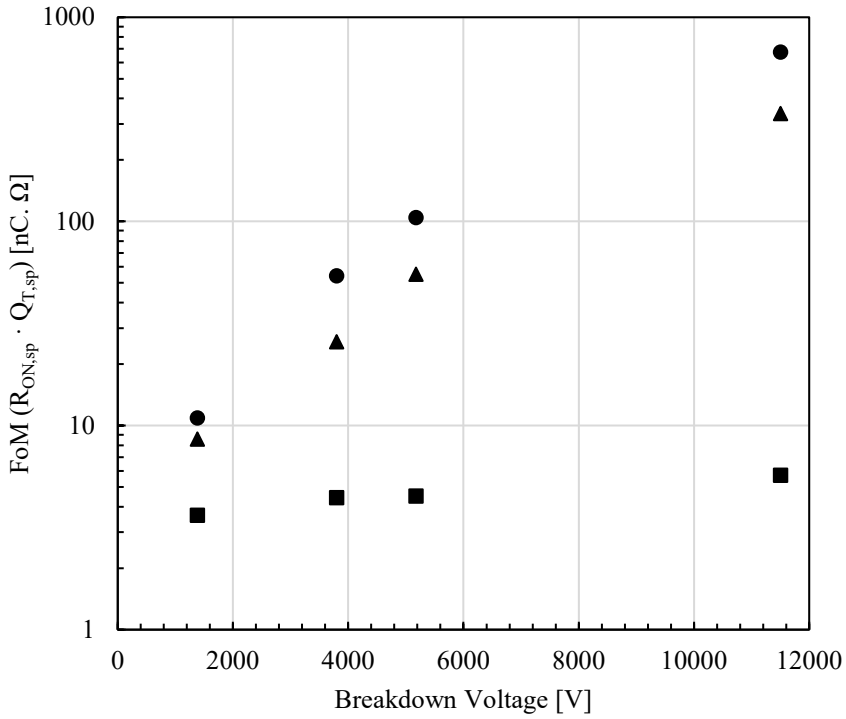

Fig. 4. FoM for monolithic BD conv. (Triangle), Hybrid-BD conv. (Circle) and Hybrid-BD SJ DMOSFETs (Square)

We use the $R_{ON,sp} \cdot Q_{T,sp}$ Figure of Merit (FoM) to evaluate and quantify the static and dynamic performance simultaneously, where $Q_{T,sp}$ is the sum of $Q_{G,sp}$ and $Q_{DS,sp}$ [8]. The hybrid BD SJ DMOSFET shows a substantial (more than 58%) improvement in the FoM compared to its conventional counterparts as shown in Fig. 4.

Conclusion

We simulate high-voltage bidirectional 4H-SiC conventional and superjunction DMOSFETs and compare their static and dynamic characteristics. We focus on hybrid BD SJ and compare it to its conventional counterparts (Hybrid and monolithic). To quantify both static and dynamic parameters, we extract $R_{ON,sp}$ and $Q_{T,sp}$ respectively, $Q_{T,sp}$ is the sum of $Q_{G,sp}$ and $Q_{DS,sp,}$ then by using a new FoM ($R_{ON,sp}$. $Q_{T,sp}$), we evaluate both performance simultaneously. Hybrid-BD SJ DMOSFET exhibits at least 58% reduction in FoM which is deemed to be advantageous in many power electronics systems.

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