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Comparison of the Surge Current Capabilities of SBD-Embedded and Conventional SiC MOSFETs

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Keywords: surge current, SBD embedded MOSFET, BMA cell, repetitive surge stress, SF expansion.

Abstract. We demonstrated that the surge current capability of 3.3 kV Schottky-barrier-diode-embedded (SBD-embedded) SiC MOSFETs is equivalent to that of conventional SiC MOSFETs and three times higher than that of SiC SBDs. Furthermore, we revealed that the bipolar degradation attributed to the repetitive surge stress of high current density was negligible, which can be explained by the small total area of the expanded stacking faults (SFs) caused by the limited total period of conduction of the body diodes.

Introduction

Schottky-barrier-diode-embedded (SBD-embedded) SiC MOSFETs suppress the bipolar degradation caused by the activation of parasitic body diodes (BDs) during the dead-time phases of inverters without external SBDs, which reduces the total device size [1, 2]. A surge current over the rated current flows through diodes in MOSFETs under certain fault events, such as a ground fault and a short-circuit fault; therefore, surge current capability is important for power device reliability. The surge current capability of SBDs is low because conductivity modulation does not occur in SBDs during surges. Recently, a few reports have investigated the surge capabilities of SBD-embedded MOSFETs [3–5], which appear to depend on the device design and structure.

We developed a new structure called a bipolar mode activation (BMA) cell to improve the surge current capability of parallel-connected SBD-embedded SiC MOSFETs. The BMA cells generate uniform I–V characteristics of embedded SBDs and prevent current crowding in parallel-connected chips, which results in surge current capability that is five times higher at a 1% failure rate of the four parallel-connected devices with BMA cells than those without BMA cells [6].

In this study, we focused on the surge current capability of single chips and compared them with SBD-embedded SiC MOSFETs with BMA cells and conventional SiC MOSFETs. Furthermore, we investigated whether surge current stress induces bipolar degradation of SBD-embedded SiC MOSFETs with BMA cells.

Comparison of Surge Current Capabilities

We fabricated 3.3 kV SBD-embedded SiC MOSFETs, conventional SiC MOSFETs, and SiC SBDs and measured their surge current capabilities. The doping density and thickness of the drift layers of the three types of samples are close and designed for 3.3 kV class devices. The chip size is an important factor in discussing the surge current capability because it affects the heat dissipation efficiency during a surge. The active areas of the three samples were all about 0.4 cm^2. Fig. 1 shows a cross-section of the samples used in this study. The BMA cells were formed in less than 1% of the active area of the SBD-embedded MOSFETs.

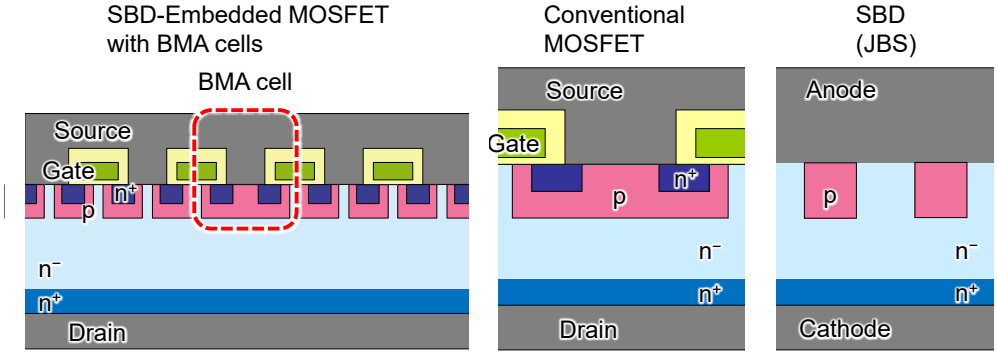

Fig. 1. Cross-sections of measured samples: an SBD-embedded MOSFET with BMA cells, a conventional MOSFET, and an SBD.

Surge Current Tests. We applied the surge current of a half-sine pulse for approximately 10 ms to the samples, which increased the peak value (I_{FSM}) until failure. Fig. 2 shows the source current density (J_S) and source–drain voltage (V_{SD}) waveforms under surge tests immediately before the failure of each sample. In a V_{SD} waveform of SBD-embedded MOSFET, there is a snapback point at ~0.8 ms. Only unipolar current flows through the SBD region during the first phase before the snapback point, whereas bipolar current leads to remarkable conductivity modulation during the second phase after the point.

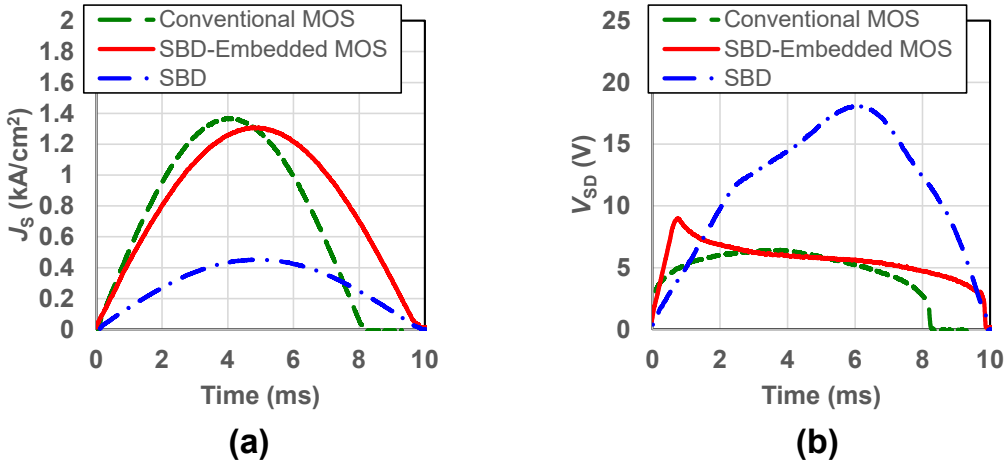

Fig. 2. (a) Source current density (J_S) and (b) source–drain voltage (V_{SD}) waveforms of the three types of samples under surge tests just before the failure of each sample.

Fig. 3 shows the J_S–V_{SD} trajectories derived from Fig. 2. The SBD-embedded and conventional MOSFETs exhibit counterclockwise loops in the J_S–V_{SD} trajectories because of the conductivity modulation caused by the activation of the BDs, where the SBD-embedded MOSFET operates as a unipolar device up to a V_{SD} of approximately 9 V.

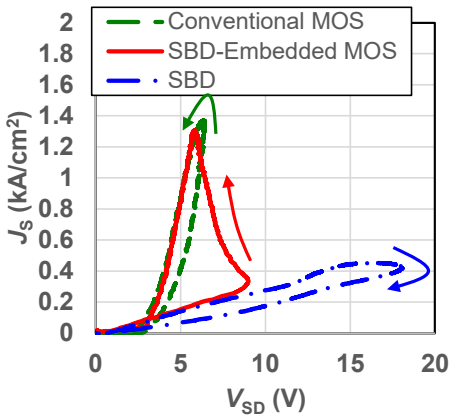

Fig. 3. J_S–V_{SD} trajectories of the three types of samples derived from Fig. 2.

Comparison of Capabilities. Fig. 4 presents Weibull plots of the surge current capabilities for five chips of SBD-embedded MOSFETs, 20 conventional MOSFETs, and 50 SBDs. The surge capabilities of the SBD-embedded MOSFETs are almost equal to those of conventional MOSFETs (~1.3 kA/cm^2), while those of SBDs are much lower (~0.45 kA/cm^2).

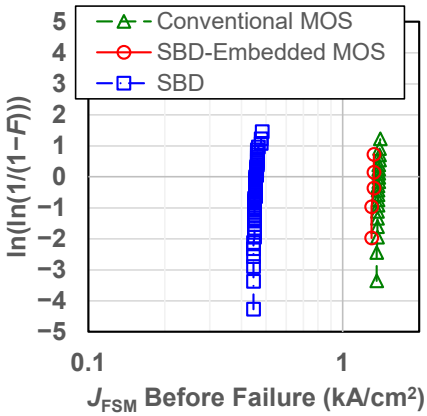

Fig. 4. Weibull plots of the surge current capability for SBD-embedded MOSFETs (circles), conventional MOSFETs (triangles), and SBDs (squares).

Fig. 5 (a) shows the specific resistance (R_{SD}) waveforms of the samples under surge current stress derived from the following equation:

$$R_{SD} = V_{SD} / J_{SD}. \quad (1)$$

While the R_{SD} of an SBD increases to ~35 mΩcm^2 around the current peak and over time owing to the temperature rise, the R_{SD} of an SBD-embedded MOSFET and a conventional MOSFET decrease to ~5 mΩcm^2 because of conductivity modulation, which results in much higher surge capabilities for both MOSFETs, as shown in Fig. 4.

Fig. 5 (b) shows the R_{SD} waveform and the transition of the consumed energy density of the SBD-embedded MOSFETs under surge-current stress. During the first phase before the snapback point, SBD-embedded MOSFETs behave as unipolar devices and exhibit an R_{SD} higher than that of conventional MOSFETs. The first phase, however, is short and the consumed energy density during the phase is low, which results in the similar surge capabilities of both MOSFETs.

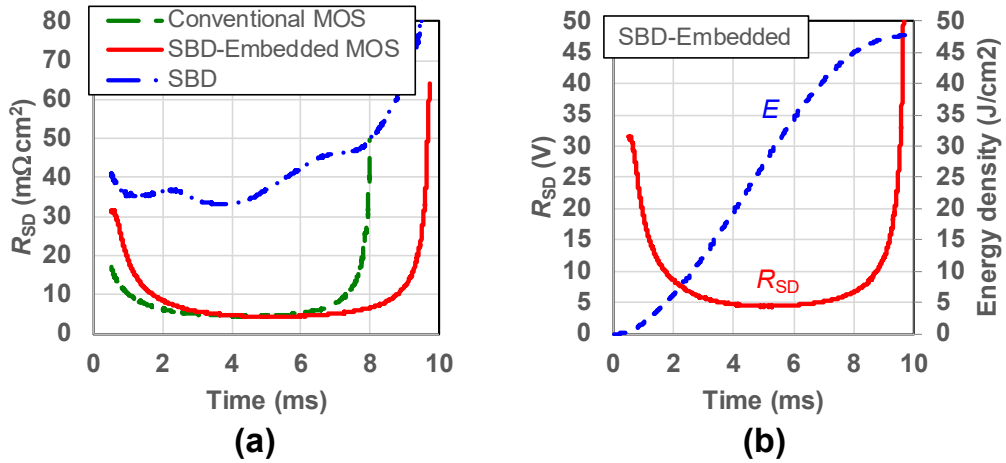

Fig. 5. (a) Specific resistance (R_{SD}) waveforms of SBD-embedded MOSFETs (solid line), conventional MOSFETs (dashed line), and SBDs (dotted-dashed line) under surge current stress. (b) R_{SD} waveform (solid line) and transition of consumed energy density (dashed line) of SBD-embedded MOSFETs.

Increase of ON Resistance by Surge Current Stress

As described in the previous section, the BDs in SBD-embedded MOSFETs are activated for a short time during surge currents owing to the high temperatures and high current densities. We investigated whether the BD activation caused stacking fault (SF) expansion and increased the ON resistance of the device.

Repetitive Surge Tests. We applied 50 surge pulses with a peak current density (J_{FSM}) of ~550 A/cm^2 for 10 ms to 15 chips of SBD-embedded MOSFETs. Fig. 6 shows the cumulative frequency of the ΔR_{ON} ratio, calculated using the following equation:

$$\Delta R_{ON}\text{ ratio} = (R_{ON}^{after} - R_{ON}^{before})/R_{ON}^{before}, \quad (2)$$

where R_{ON}^{before} and R_{ON}^{after} denotes the R_{ON} values of the samples before and after the surge current stress, respectively. In all samples, there was no increase in the R_{ON}; most ΔR_{ON} values arose from measurement errors. The lack of bipolar degradation in SBD-embedded MOSFETs after the surge current activates the BDs can be explained by the small total area of the expanded SFs.

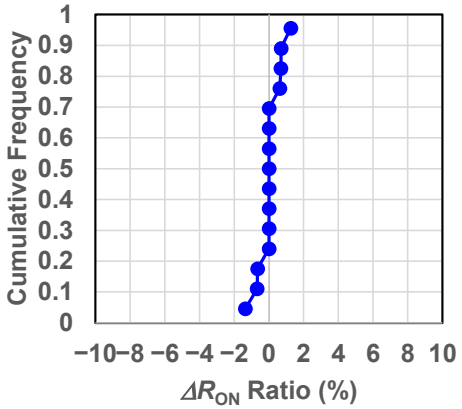

Fig. 6. Cumulative frequency of the ΔR_{ON} ratio of SBD-embedded MOSFETs induced by 50 times pulses with a J_{FSM} of ~550 A/cm^2 and a duration of 10 ms.

Estimation of SF Area Expanded by Repetitive Surge. Fig. 7 (a) shows the expansion velocity of bar-shaped SFs, which is a major cause of an increase in R_{ON} in 1.2 kV PN diodes measured by in situ emission microscopy during bipolar current conduction with 600–1400 A/cm^2 at 70–170°C. The

dashed lines indicate fitting lines with a single equation assuming the expansion velocity follows Arrhenius low. As shown in Fig. 7 (b), our data are consistent with those obtained from 3.3 kV MOSFETs at 150°C [7]. Assuming the temperature of chips during surge events to be 600°C, we estimated the expansion length of an SF after 100 pulses of 1000 A/cm^2 with a duration of 10 ms to be approximately 75 μm.

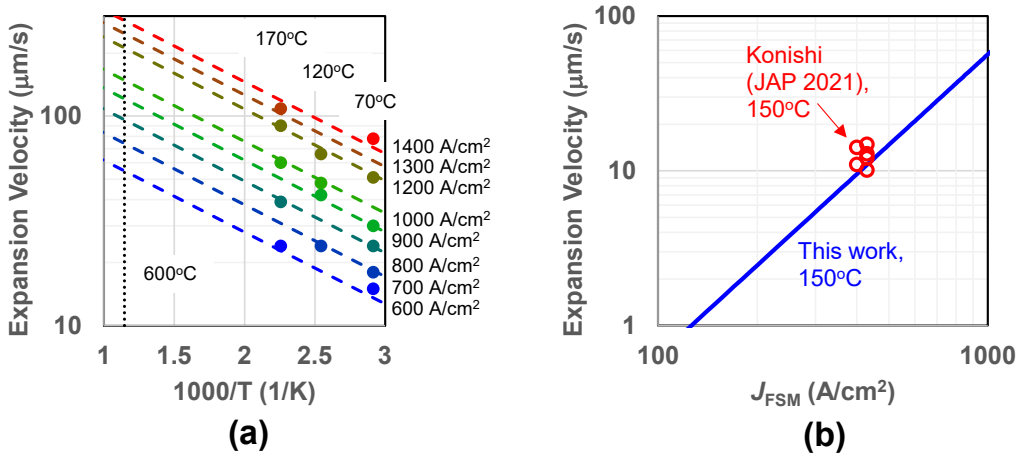

Fig. 7. (a) Expansion velocity of bar-shaped SFs in 1.2 kV PN diodes measured by in situ emission microscopy during bipolar current conduction with 600–1400 A/cm^2 at 70–170°C. (b) Expansion velocity of bar-shaped SFs at 150°C extracted from Fig. 7 (a). Data from 3.3 kV MOSFETs reported by Konishi et al. [6] are also plotted.

Fig. 8 shows that the SF area can be calculated as double the product of the expansion length and SF width of 429 μm in a 30-μm thick epilayer when we approximate the shape of the SFs to be rectangular. ΔR_{ON} ratio can be calculated as the ratio of the total SF area to the active area using the following equation:

$$\Delta R_{ON} \text{ ratio} = A_{SF} / (A_{active} - A_{SF}), \quad (3)$$

where A_{SF} and A_{active} is the expanded SF and active area. We disregarded the effects of the SFs on the carrier lifetime in the drift region because we considered the ON resistance under the unipolar mode. We estimated that approximately 60 SFs per chip would increase R_{ON} by 10%.

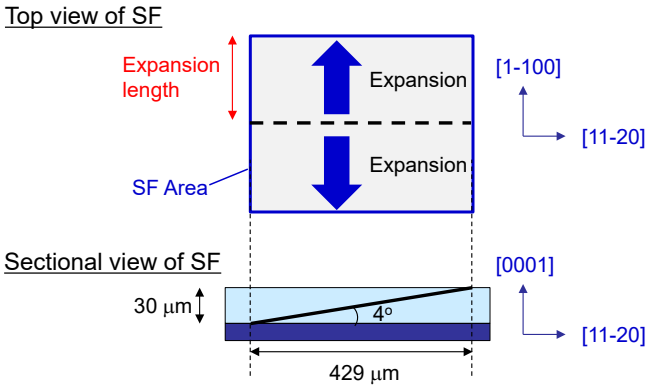

Fig. 8. Schematic of a bar-shaped SF used for the calculation of SF area interrupting current flow. The shape is approximated to be rectangular for simplicity.

Estimation of the Number of SFs in a chip. After applying high current stress to the BDs in 1706 chips of 3.3 kV conventional MOSFETs, we removed the metal layers on the chips with increased R_{ON}, which should include bar-shaped SFs in their active area. Photoluminescence images were obtained from the chips using a 340-nm excitation laser and a 420-nm-band-pass filter, and the

number of bar-shaped SFs in each chip was counted. Fig. 9 (a) shows the relative frequency of the number of SFs per chip for 1706 chips. Fig. 9 (b) shows the cumulative frequency of the number of SFs per chip, where the red circles denote the measured data converted from Fig. 9 (a). The blue line indicates the line fitting the measured data under the assumption of a gamma distribution, which is consistent with actual defect distributions [8]. A chip seldom contains more than 60 SFs.

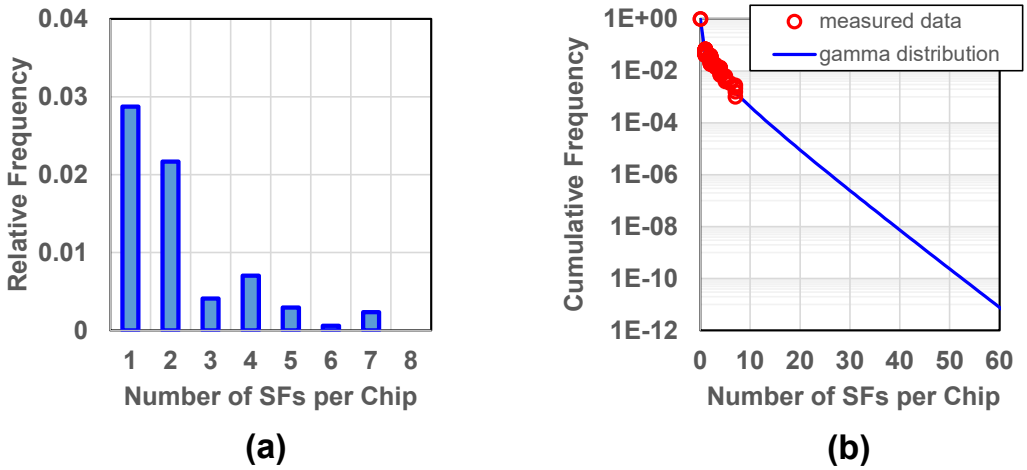

Fig. 9. (a) Relative frequency of the number of SFs per chip in 1706 chips. (b) Cumulative frequency of the number of SFs per chip. Red circles: measured data calculated from Fig. 8. Blue line: Fitting line assuming a gamma distribution.

ΔR_{ON} ratio in SBD-embedded and conventional MOSFETs. We estimated ΔR_{ON} ratios in the SBD-embedded and conventional MOSFETs after repetitive surge stress and normal operation. While SFs expand ~75 μm by repetitive surge stress, as estimated before in both devices, they do not expand during normal operation in SBD-embedded MOSFETs because all freewheeling current flows through their embedded SBDs. In conventional MOSFETs, SFs expand ~3.85 mm during one week of normal operation:10 kHz operation with a dead time of 1 μs under a freewheeling current density of 100 A/cm^2 at 150ºC. From the above expansion lengths of the SFs and the distribution of the number of SFs in a chip (Fig. 9), we estimated the ΔR_{ON} ratio, as shown in Fig. 10, where the ΔR_{ON} ratio reached 20% with a probability of approximately 1% in conventional MOSFETs and 10% with a probability of approximately 10^{-11} in SBD-embedded MOSFETs.

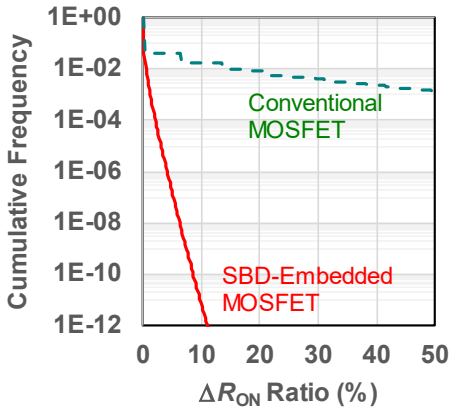

Fig. 10. Cumulative frequency of ΔR_{ON} ratio in SBD-embedded MOSFETs (solid line) and conventional MOSFETs (dashed line) after both repetitive surge stress and one week of normal operation: 10 kHz operation with a dead time of 1 μs under a freewheeling current density of 100 A/cm^2 at 150ºC.

Summary

We compared the surge current capabilities of single chips of 3.3 kV SBD-embedded SiC MOSFETs with BMA cells, conventional MOSFETs, and SBDs with an active area of approximately 0.4 cm^2, thereby revealing that the surge current capability of SBD-embedded SiC MOSFETs is equivalent to that of conventional SiC MOSFETs and three times higher than that of SiC SBDs. Furthermore, we revealed that the bipolar degradation of the samples attributed to the repetitive surge stress of 50 pulses with a J_{FSM} of approximately 550 A/cm^2 and a duration of 10 ms was negligible, which can be explained by the small total area of the expanded SFs caused by the limited total period of BD conduction. We estimated that approximately 60 SFs in a chip would increase R_{ON} by 10% with surge stress and that its probability is extremely low.

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