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Junction-Controlled-Diode-Embedded SiC-MOSFET for Improving Third Quadrant and Turn-On Characteristics

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Abstract. In this paper, we propose a novel 1200V SiC MOSFET featuring the embedded junction-controlled-diode (JCD-MOSFET) and demonstrate its static and dynamic characteristics through TCAD simulations. Without sacrificing blocking and conduction performance, the adoption of JCD can effectively reduce knee voltage to 1.7V based on unipolar carrier conduction mode. Due to the reduced peak reverse recovery current and reverse recovery charge, the JCD-MOSFET achieves 30.8% lower turn-on losses than conventional MOSFET. Meanwhile, the fabrication process for the JCD-MOSFET is the same as conventional MOSFET without an extra mask. This proposed JCD-MOSFET prototype shows great potential in target applications in the near future.

Introduction

SiC MOSFETs characterize both low conduction and switching losses under a wide range of blocking voltages, which are suitable for industrial and automotive applications, e.g., uninterruptible power supply, energy storage systems, and main drive inverters of electric vehicles [1]. The adoption of an internal freewheeling diode, i.e., PN body diode, of SiC MOSFET enables switching operation without external diode chips. However, the operation of PN body diodes has a high knee voltage V_{knee} (~2.7V) with the risk of bipolar degradation. To alleviate these issues, several unipolar diode integration strategies have been proposed, such as Schottky-barrier-diode-embedded and source or gate-controlled channel-diode-embedded SiC MOSFETs [2-4]. Unfortunately, these strategies bring a huge challenge between blocking and conduction capability. Moreover, complicated fabrication processes are also required.

In the paper, we propose a novel 1200V junction-controlled-diode-embedded SiC MOSFET (JCD-MOSFET), offering lowered knee voltage, reduced reverse recovery charge and turn-on losses, as well as compatible fabrication process as conventional planar SiC MOSFET (C-MOSFET).

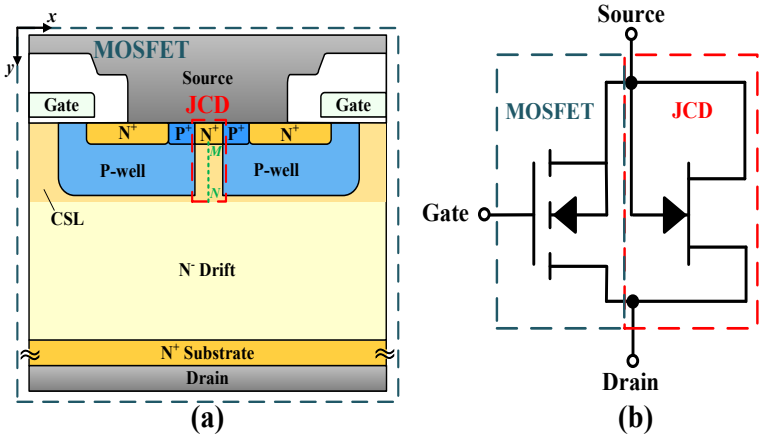

Fig. 1. (a) Cross-section structure and (b) equivalent circuit of the proposed JCD-MOSFET.

Device Structure and Design Concept

The cross-section structure and equivalent circuit of the proposed JCD-MOSFET are shown in Fig.1. Additionally, for comparison, a 1200V/80mΩ C-MOSFET is also characterized, and the physical parameters and device area are the same for C- and JCD-MOSFET [5].

There is a JCD embedded into the adjacent P-well of JCD-MOSFET as shown in the red line of Fig. 1. Due to the current spreading layer (CSL) between the adjacent P-well being fully depleted, the JCD generates a low potential barrier as shown in Fig. 2(a). As V_{DS} reaches -1.7V, electrons can flow from the N^- drift to N^+ source region by overcoming the potential barrier of JCD as shown in Fig. 2(b).

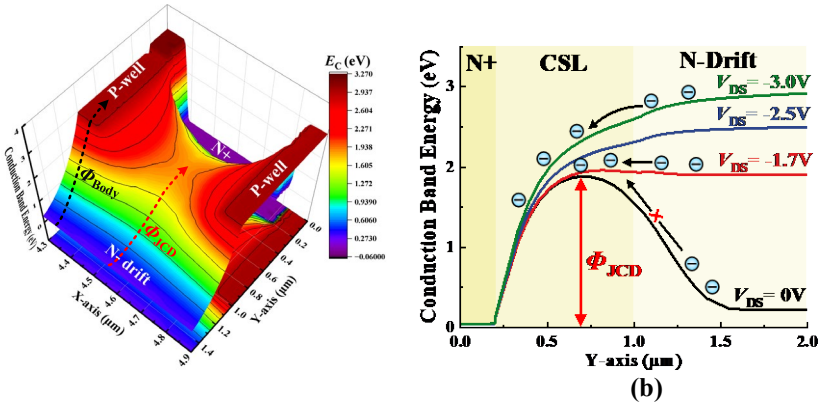

Fig. 2. Three-dimensional conduction band energy E_C distribution of JCD under zero applied bias and (b) E_C distribution along line M-N in Fig. 1 under various V_{DS}.

The JCD can turn on at 1.7V through unipolar conduction as shown in Fig. 3(a), which is much lower than that of PN body diode. Moreover, thanks to reduced holes injected from the body diode as shown in Fig. 3(b), the bipolar conduction mode is significantly suppressed. Furthermore, on one hand, the potential barrier decreases with the wider channel width L_j of JCD, achieving the reduction of V_{knee} as shown in Fig. 4(a). On the other hand, the wider L_j weakens blocking capability because of the premature breakdown of JCD as shown in Fig. 4(b).

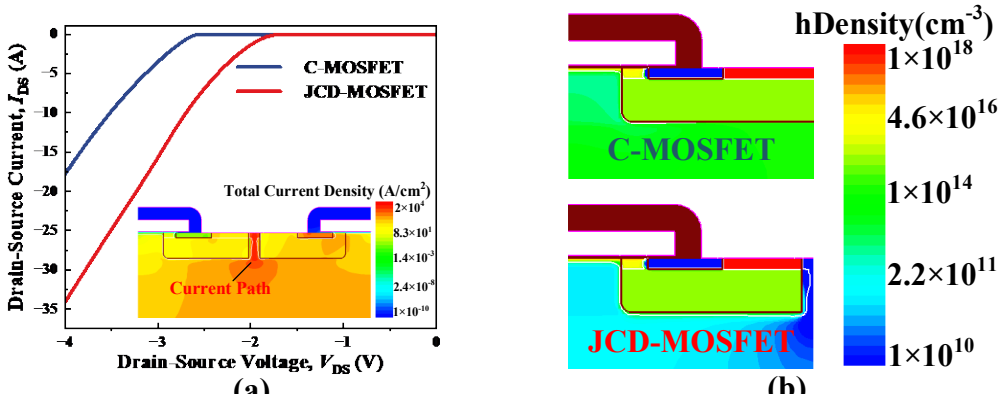

Fig. 3. (a) Third quadrant characteristics and (b) hole density distributions at I_{DS}=-10A for C- and JCD-MOSFET.

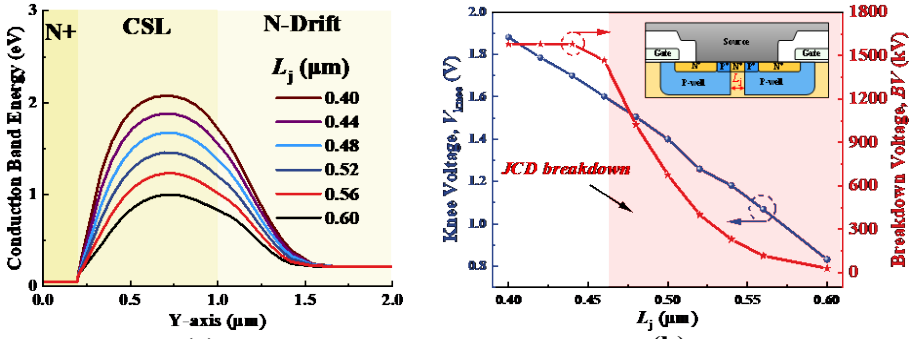

Fig. 4. Influence of L_j on (a) E_C distribution along line M-N in Fig. 1 under zero applied bias, (b) V_{knee}, and BV for JCD-MOSFET.

Results and Discussion

As shown in Fig. 5, the JCD-MOSFET exhibits the same ON-resistance $R_{DS(on)}$ of 80mΩ at V_{GS}=20V and breakdown voltage BV of 1597V at V_{GS}=-5V as C-MOSFET. This is because the JCD is in OFF-state when the JCD-MOSFET operates in the first quadrant.

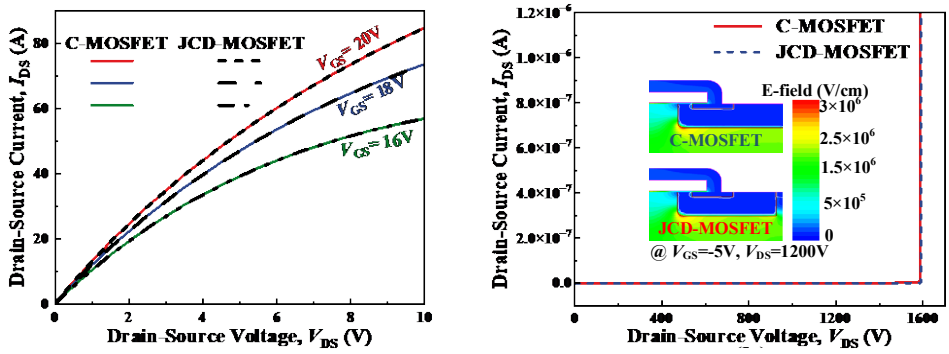

Fig. 5. (a) Output characteristics and (b) breakdown voltage characteristics for C- and JCD-MOSFET.

Moreover, the peak reverse recovery current and reverse recovery charge (Q_{rr}) of JCD-MOSFET are only 22.7A and 117.9nC as shown in Fig. 6, which reduces 36.6% and 43.3% compared with C-MOSFET, respectively. This improvement is thanks to the absence of hole injection when the JCD turns on. The JCD-MOSFET shows the same turn-off characteristic as that of C-MOSFET as shown in Fig. 7(a), whereas the JCD-MOSFET reduces the turn-on losses E_{on} by 30.8% as the C-MOSFET owing to lower reverse recovery charge as shown in Fig. 7(b).

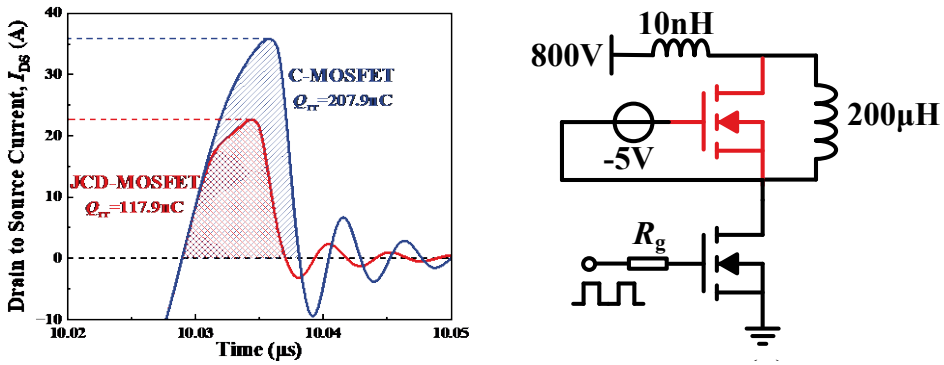

Fig. 6. (a) Reverse recovery characteristics of the diodes in C- and JCD-MOSFET and (b) inductive load double-pulse test circuit.

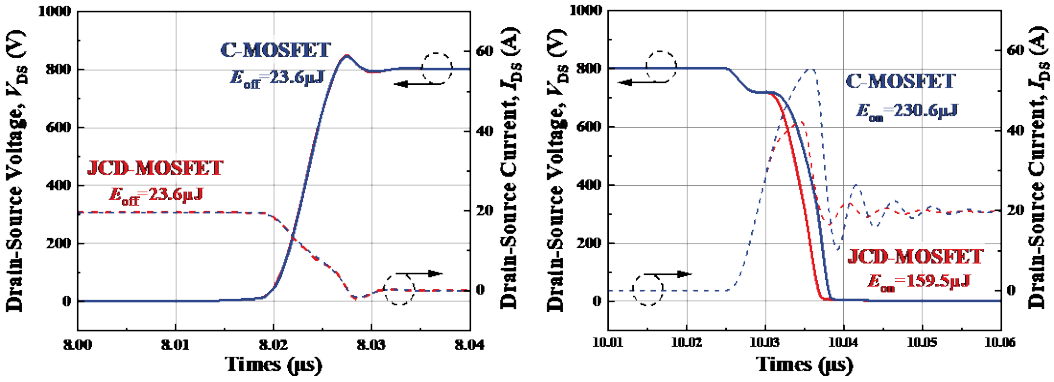

Fig. 7. (a) Turn-off and (b) turn-on waveforms of C- and JCD-MOSFET.

Furthermore, we also provide an available fabrication process flow of the JCD-MOSFET without adding an extra mask as shown in Fig. 8. The electrical performance comparison between C-and JCD-MOSFET is shown in Table I, demonstrating that this work provides a cost-effective design strategy to improve SiC MOSFET performance.

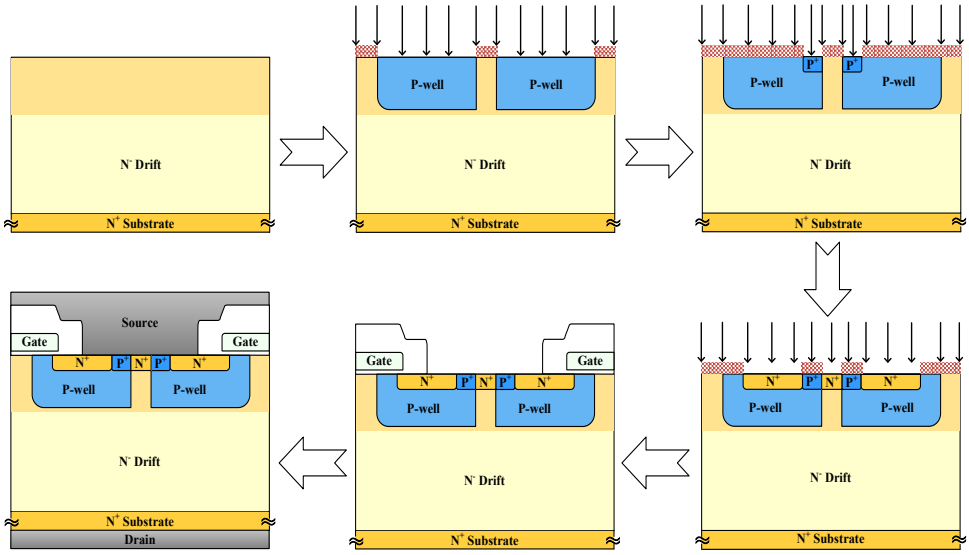

Fig. 8. Available fabrication process of the proposed JCD-MOSFET.

TABLE I
Performance Comparision of SiC C-MOSFET and JCD-MOSFET

	C-MOSFET	JCD-MOSFET	Unit
$R_{DS(on)}$	80	80	mΩ
BV	1597	1597	V
V_{knee}	2.7	1.7	V
Q_{rr}	207.9	117.9	nC
E_{on}	230.6	159.5	μJ
E_{off}	23.6	23.6	μJ

Summary

In this paper, we propose a novel JCD-MOSFET that realizes lowered V_{knee}, reduced Q_{rr} and E_{on}, as well as compatible fabrication process as C-MOSFET simultaneously. The embedded JCD turns on when the V_{DS} reaches -1.7V and achieves unipolar carrier conduction. Compared with C-MOSFET, the peak reverse recovery current and Q_{rr} of JCD-MOSFET are reduced by 36.6% and 43.3%,

respectively. As a result, the JCD-MOSFET shows a 30.8% lower E_{on} than that of C-MOSFET. Meanwhile, an available fabrication process flow of the JCD-MOSFET without adding an extra mask is also proposed.

Acknowledgment

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