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Influence of Channel Length and Gate Oxide Thickness Variations in 3300 V 4H-SiC VDMOSFET

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Abstract. In this work, variations in the channel length and gate oxide thickness are studied for the design optimization of 3300 V 4H-SiC based VDMOSFETs. For this, a batch of 3 wafers was processed and tested for key device characteristics. The results indicate shorter channel length of 0.5 μm leads to an increase in the drain leakage current, thus affecting the breakdown voltage as well. The thinner gate oxide at 50 nm demonstrates better control of threshold voltage with no variations in the gate leakage current distribution as compared to 65 nm.

Introduction

With high critical electrical field and thermal conductivity, the wide bandgap SiC based power devices offer unparalleled advantages in high-voltage, high-power, and high-frequency applications such as solar, railway traction inverters and EV/HEV drives. [1], [2] 3.3 kV rated 4H-SiC based VDMOSFETs offer distinct benefits in size and cost reduction for high frequency and high voltage applications such as traction and solid-state transformers for power networks. [3], [4] For robust and reliable performance at such high voltage, a well optimized device design is required. Previous work to optimize the device design mostly covered lower voltage ranges of 1.2 kV [5], [6], [7], [8] while the same is limited for 3.3 kV range devices [9]. In this work, the effect of channel length (L_{ch}) and gate oxide thickness (T_{ox}) are studied to optimize the device design thus alleviating any detrimental effects due to short channel on the key device metrics.

Fabrication and Measurements

Figure 1(a) shows a cross-sectional view of the 3.3 kV VDMOSFET fabricated on 150 mm, N+ 4H-SiC wafers with epilayer thickness of 30 μm, a fully processed wafer is shown in fig. 1(b). The dimensions of the designed dies investigated in this study are 3.2 x 3.2 mm. The channel length variation from 0.5 to 0.8 μm with a step-size of 0.1 μm was considered along with a split of 50 nm and 65 nm for gate oxide thickness. While two 150 mm wafers were processed with 50 nm gate process, a single wafer was processed for 65 nm gate oxide.

Typical aluminium and nitrogen implants were used for P+/JTE/Pwell and N+/JFET, respectively. These implants were then activated by a high temperature annealing with a carbon cap layer. Gate dielectric was fabricated, including passivation of interface and oxide traps. The front ohmic contacts to N+/P+ were enabled via a self-aligned nickel silicidation. A power metal stack, consisting of Ti/Al/Cu, was then deposited to provide metallization for the source and gate. For the ohmic back contact, the deposited metal was laser annealed to form an ohmic contact followed by a solderable back metal stack. For electrical characterization, Agilent B1505A power device analyzer was used for both wafer-sort and sweep measurements. The gate oxide thickness was also tracked both by inline optical and EOL (End of Line) measurements using process control monitor structures. Other key specs like field effective mobility, gate breakdown voltages, specific contact resistance, sheet resistance for N+, P+, poly layers were also measured using dedicated structures.

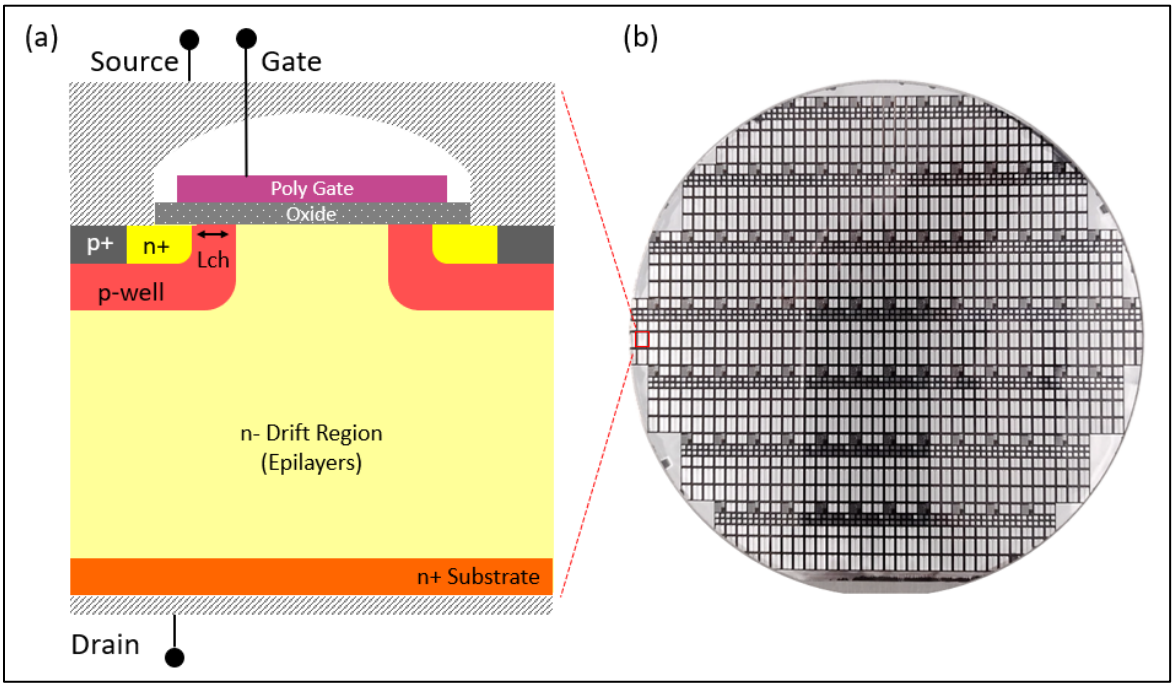

Fig. 1. (a) Cross-sectional view of the 3.3 kV VDMOSFET **(b)** Image of one of the three multi-project 150 mm SiC wafer containing 3.3 kV VDMOSFETs.

Results and Discussion

Figure 2(a) and (b) show variations in the threshold voltage, V_T-µA, defined at a fixed drain current of 1.0 µA, with different L_{ch} and T_{ox} considered in this study. For a fixed gate oxide thickness, lowering of V_T-µA as L_{ch} scaled from 0.8 to 0.5 µm is observed, an indication of a typical short-channel effects behavior. As seen in figure 2(b), a lower aspect ratio (L_{ch} /T_{ox}) results in higher del V_T-µA (del V_T-µA measures the shift in threshold voltage with channel length variation) for the thicker T_{ox} of 65 nm as compared to 50 nm devices. This trend in the threshold voltage variation also agrees with related studies reported in the literature where the critical channel length triggering the SCEs varies from 0.9 to 2.7 µm, depending on the doping concentration in the Pwell region. [10], [11]

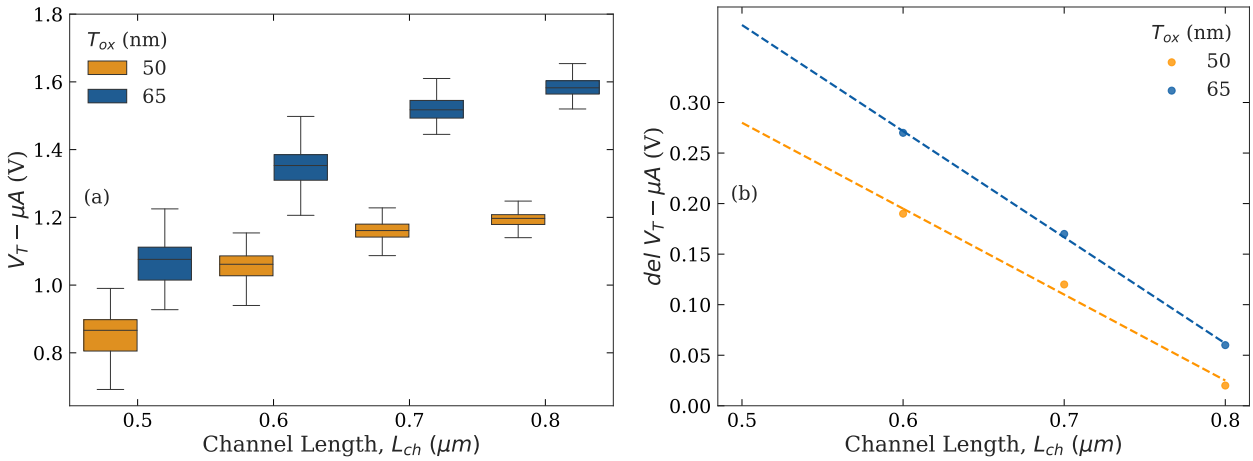

Fig. 2. (a) Box plots of variations in the threshold voltage, V_T-μA, measured at a fixed drain current of 1 µA and **(b)** shift in the threshold voltage, del V_T-µA, for variations in the channel length and gate oxide of 0.5, 0.6, 0.7, and 0.8 µm and 50 nm, 65 nm, respectively.

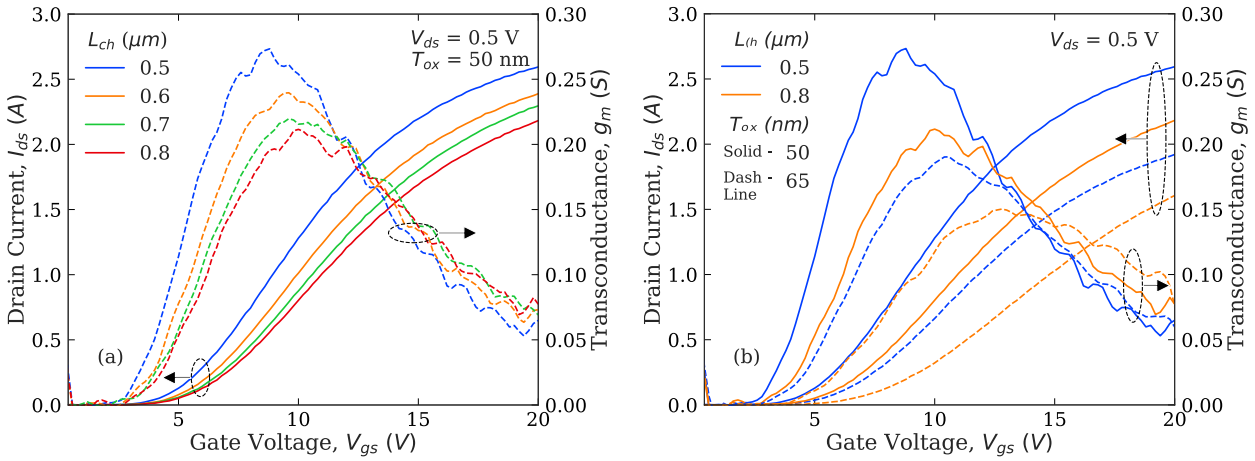

Fig. 3. (a) Transfer characteristics of T_{ox} = 50 nm devices measured at V_{ds}= 0.5 V for different L_{ch}, the secondary y-axis plots the corresponding transconductance curves **(b)** Comparison of transfer characteristics of L_{ch} = 0.5 and 0.8 µm devices for 50 and 65 nm gate oxide thickness, the secondary y-axis plots the corresponding transconductance curves.

Typical transfer curves are plotted in figure 3(a) and 3(b), respectively, for both L_{ch} variation and T_{ox} variations at V_{ds} = 0.5 V. An increment in the peak transconductance (g_m) with both L_{ch} and T_{ox} scaling can be observed indicating a scope of further design optimization depending on application requirements. Figure 4(a) and (b) show the variation in the device leakage current (IDSS) and breakdown voltages (BVDSS), respectively. The 0.5 µm devices shows a significant increase in the leakage current, with over an order of magnitude higher leakage current as compared to other devices. The longer channel length devices (L_{ch} ≥ 0.6 µm) show similar leakage levels with average IDSS around 80 nA. Though, the increase in the leakage current in 0.5 µm devices reduces the BVDSS by 100 V, the other device types record an average BVDSS of 3900 V. This increase in the drain leakage current and subsequent lowering of BVDSS at extreme lower end of L_{ch} scaling can also be attributed to SCEs where the drain voltage starts affecting minimum channel potential, resulting in higher leakage current and lowering breakdown voltages.

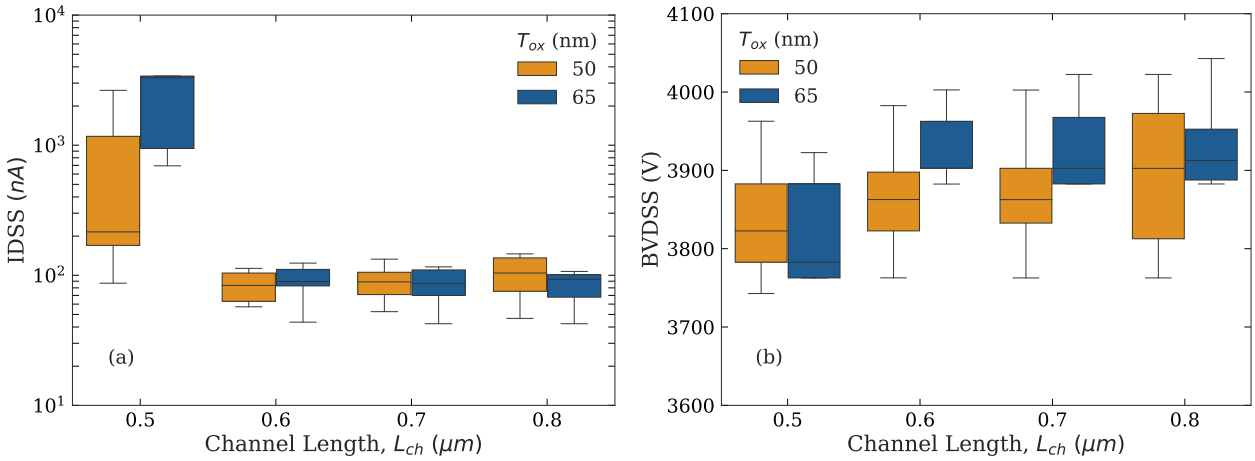

Fig. 4. (a) Device leakage current (IDSS) measured at 3300 V plotted in base Log_{10} scale and **(b)** Breakdown voltage (BVDSS) for different L_{ch} and T_{ox} devices.

Though other device metrics like V_T-mA (threshold voltage measured at 10 mA drain current) showed typical variations with L_{ch} and T_{ox}, the gate-leakage current (IGSS) did not show any significant variation in 50 and 65 nm devices. This indicates a further scope of scaling down the gate oxide thickness thus enabling shorter channel length and tighter design pitch. However, any significant increase in IGSS and related gate oxide reliability issues in thinner gate oxide and a good trade-off between Rdson and L_{ch} will ultimately define the lower and upper limits for scaling T_{ox} and L_{ch}, respectively.

Summary

This study demonstrates the limits of channel length scaling due to detrimental effects like device leakage and the benefits of thinner gate-oxide in limiting the short channel effects below 0.7 μm where the key device characteristics like IDSS and BVDSS starts getting affected adversely. A further scope of scaling down the gate oxide thickness thus enabling shorter channel length and tighter pitch can be explored further. However, any significant increase in IGSS and related gate oxide reliability issues in thinner gate oxide and a good trade-off between on resistance and L_{ch} will ultimately define the lower and upper limits for scaling T_{ox} and L_{ch}, respectively.

Acknowledgement

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