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Investigation of the Short-Circuit Withstand Time and On-Resistance Trade-Off of 1.2 kV 4H-SiC Power MOSFETs

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Keywords: 4H-SiC MOSFET, Trade-Off of Power MOSFET, Short Circuit Withstand Time.

Abstract. The short-circuit withstand time and on-resistance trade-off is investigated in 4H-SiC Power MOSFETs. We compare the static and short circuit withstand time results along with JFET width dependency and PWELL doping variation of MOSFET. We present that smaller Rds,on by wider JFET width and lighter doped PWELL results in worse short circuit withstand time.

Introduction

SiC Power MOSFETs allow high power, high voltage and high temperature operation due to very attractive properties of 4H-SiC, such as high critical electric field, low leakage current, and high thermal conductivity due to the wide bandgap nature of the material [1]. Recent SiC power MOSFET technology development has focused on minimizing of on-resistance (Rds,on) of the devices for reduction of conduction losses and improved energy efficiency. However, reductions in Rds,on of SiC MOSFET results in higher power density and increased electric field in the structure, which causes trade-offs with other performance parameters, such avalanche voltage (BVDSS) and short circuit withstand time (SCWT) [2, 3]. The most approach for improving SCWT is to reduce MOSFET output current. The various methods of improving SCWT have been investigated along focusing MOSFET and JFET parameter [4,5]. These results are appearing strong relationship with Rds,on. We have investigated the trade-off relationship for the BVDSS capability, parasitic capacitances, and SCWT based on design and process parameters and the results are reported in this paper.

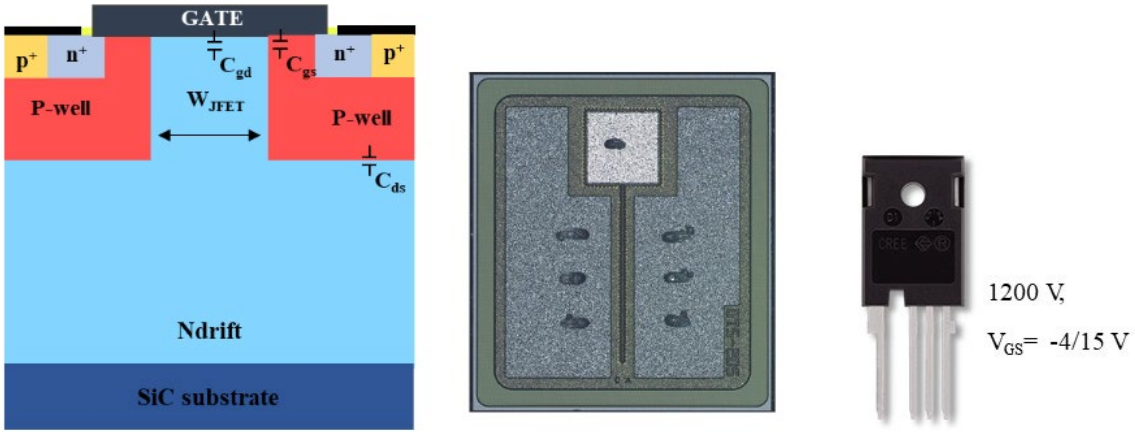

Fig. 1. The cross-sectional view and chip of 1.2 kV SiC Power MOSFETs.

Table 1. Design and process variations for the experiment

	Description
Design	▪ JFET width variation (ΔW_{JFET}) - 0 (reference), +80 nm, -120 nm, -200 nm
Process	▪ P-well doping concentration - Reference doped P-well - Heavier doped P-well (200 % of reference)

1.2kV 4H SiC MOSFET structure and Experiment

Figure 1 shows a simplified cross-sectional view of the 1.2 kV SiC Power MOSFET. JFET gap (W_{JFET}) was varied from -200 nm to 80 nm from the reference W_{JFET} value, with a fixed cell pitch, to study the impact of JFET width on performance parameters, which includes Rds,on, SCWT, and parasitic capacitances. Doping concentration in the P-well was also varied in this experiment. A summary of design and process variations are shown in Table 1.

Electrical Results

Figure 2 shows the Rds,on values (Vgs=15V) at 25 ºC (a) and 175 ºC (b) as a function of JFET gap (ΔWJFET) and P-well doping concentration. Rds,on increases monotonically with decreasing JFET gap. Heavier P-well doping concentration also resulted in higher Rds,on, as well. This is because of the increase in JFET resistance due to narrower JFET gap and the more positive threshold voltage caused by the increased P-well doping concentration. However, BVDSS was improved at narrower JFET gaps and heavier doped P-well because of reduced electric-field distribution near P-well to JFET gap. Values of normalized parasitic capacitances (Ciss, Coss, and Crss) measured from devices with varying JFET gaps and P-well doping concentrations are provided in Figure 3. Devices with heavier doped P-wells showed larger Ciss and Coss than those with lighter doped P-wells. Crss showed the opposite trend from Ciss and Coss, with heavier P-well doping leading to lower Crss. Devices with narrower JFET gap showed the same trend as the devices with higher P-well doping concentration on the capacitances. Figure 4 shows C-V plots for Ciss, Coss and Crss for the devices with two different P-well doping concentrations.

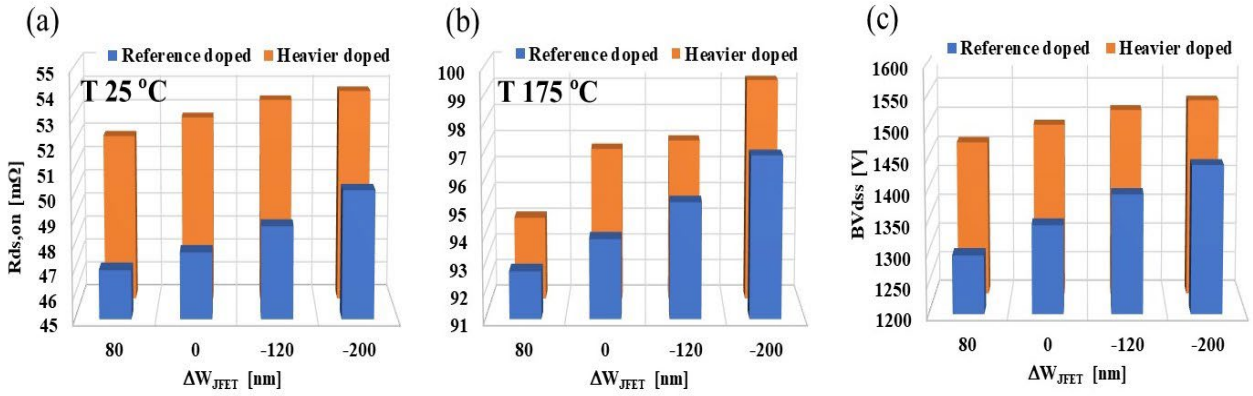

Fig. 2. Static characteristic for JFET width and comparison with P-well doping amounts (a) the on-resistance at 25 ºC vs ΔW_{JFET}, (b) the on-resistance at 175 ºC vs ΔW_{JFET}, (c) BVdss at 25 ºC vs ΔW_{JFET}

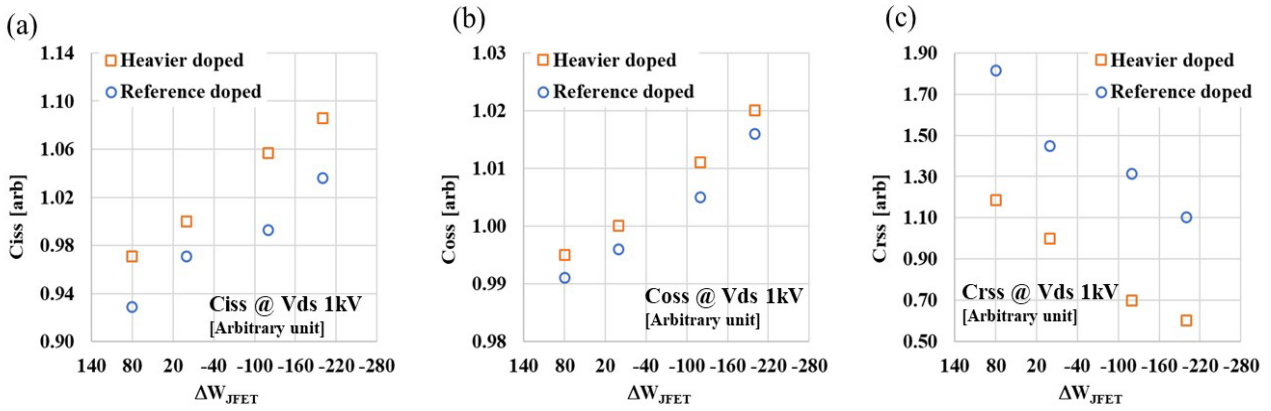

Fig. 3. Normalized Ciss, Coss, and Crss characteristic. (a) Ciss (input capacitance) vs ΔW_{JFET} (b) Coss (out capacitance) vs ΔW_{JFET} (c) Crss (Reverse transfer capacitance) vs ΔW_{JFET}. The measurements were done at a VDS of 1000V.

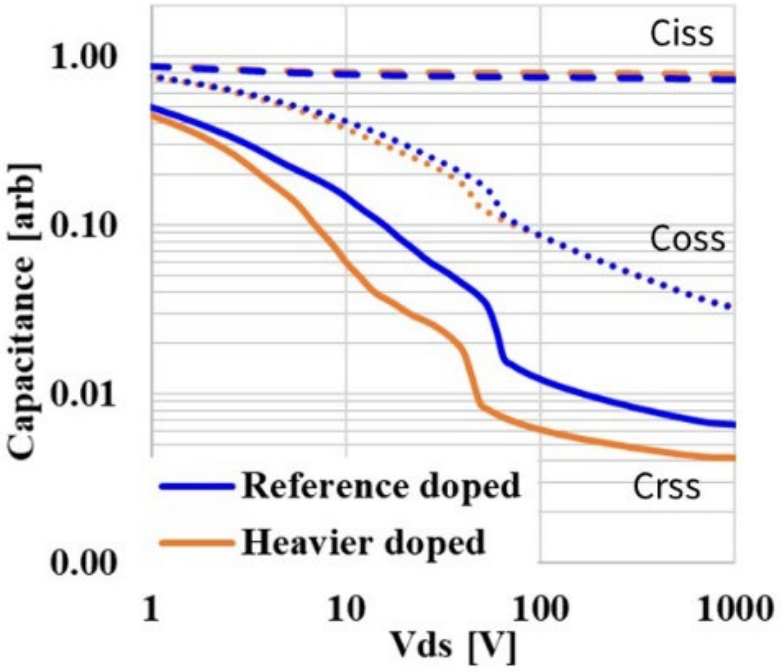

Fig. 4. C-V characteristic (Ciss, Coss, Crss) of SiC MOSFETs with two P-well doping concentrations. The reference JFET gap was used.

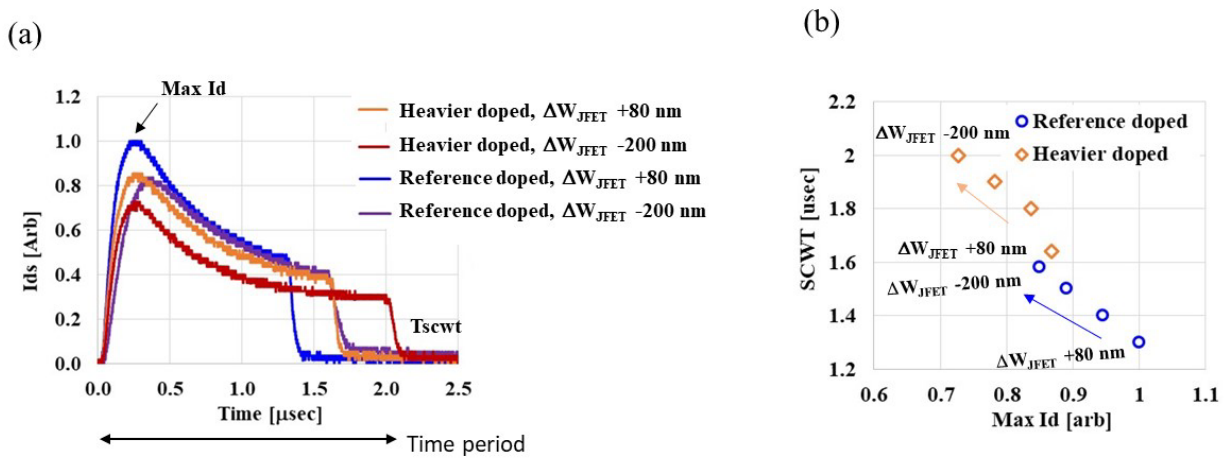

Fig. 5. (a) Short circuit withstand time (SCWT) waveform comparison (b) SCWT as a function of max drain current.

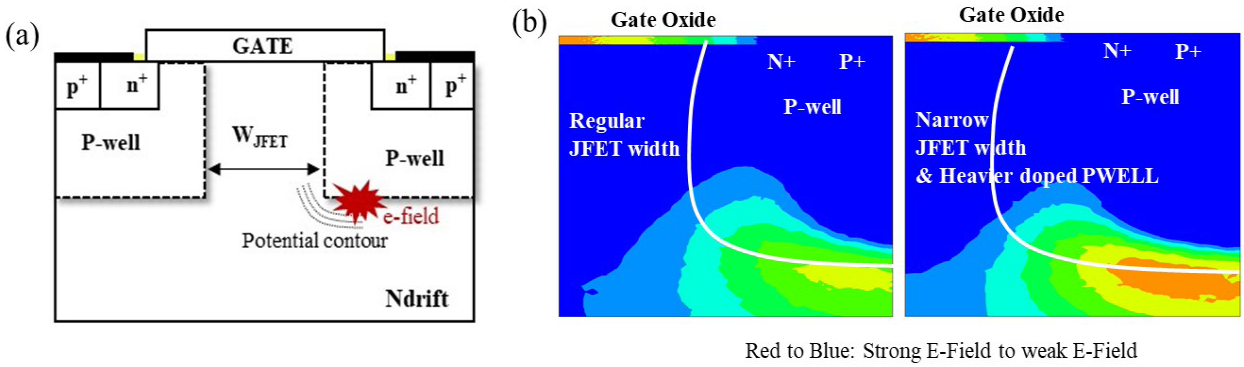

Fig. 6. (a) The describing sketch for electric field distribution at the high electric field of the structure (b) TCAD simulation e-field contour comparison at Vgs=0V.

Figure 5(a) shows short-circuit current wave form comparison at a VDS of 800 V. The junction temperature at the beginning of the waveform was 25°C for all devices. Devices with heavier doped P-well showed smaller peak drain current. With the reduced peak drain current during short circuit events, SCWT also improved with higher P-well doping, as shown in Figure 4(b). These results indicate that smaller JFET width results in higher JFET resistance, which reduces the amount of drain current at MOSFET saturation, which improves the SCWT. Smaller JFET width also reduces electric field in the gate oxide due to self-shielding, which can improve both BVDSS and SCWT, as shown in Figure 6. High doping concentrations in the P-well also reduce the current density in the saturation region of the MOSFET.

Conclusion

In this paper, we presented the short-circuit withstand time and on-resistance trade-off relationship in 4H-SiC Power MOSFETs. We compared Rds,on, Capacitance, and breakdown voltage of SiC MOSFET as a function of JFET width variation and PWELL doping concentrations. Narrower JFET width and heavier PWELL concentrations lead the drain current reduction at MOSFET saturation due to higher JFET resistance, which results in breakdown voltage and the short circuit withstand time improvement under Rds,on trade-off. For design optimization of 4H-SiC power MOSFETs, these trade-off relationships should be considered as well as Rds,on for optimum performance of the power system.

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