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Power Cycling Performance of 3.3 kV SiC-MOSFETs and the Impact of the Thermo-Mechanical Stress on Humidity Induced Degradation

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Abstract. Recently, silicon carbide (SiC) power modules of the 3.3 kV voltage class became available and are a promising candidate to replace silicon power modules in traction applications. However, the more than three times higher Young's Modulus compared to silicon leads to a reduced lifetime under thermo-mechanical stress. This could pose a significant obstacle in their implementation, since traction applications are particularly demanding in their mission profiles with respect to load cycling, but also to environmental conditions. Thus, the thermo-mechanical stress is not just limiting the lifetime itself, but might also promote the humidity induced degradation due to delamination or micro-cracks. In this work, multiple power cycling tests at different temperature swings on 3.3 kV SiC MOSFET chips in a power module were performed, to assess their ruggedness under thermo-mechanical stress. Before or afterwards, these modules were tested under standard HV-H³TRB conditions to verify the interaction between thermo-mechanical and humidity stress on the robustness of the modules.

Design of Experiment and Devices Under Test (DUT)

The low availability and high cost of 3.3 kV SiC-MOSFET modules prohibited an experiment on full modules. Instead engineering samples were used, which had been manufactured on the same processing line as the standard traction devices with traction rated packaging materials (fig. 1). The silicone gel (Si-gel) potted modules are used to assess the reliability of the devices in terms of thermo-mechanical and electro-chemical stress with respect to an application relevant packaging. These packages were already used for different investigations [1,2] with a focus on humidity induced degradation. In [2], a comparison between Si-IGBTs and SiC-MOSFETs in these packages is shown with a clear difference in the performance under HV-H³TRB conditions (**H**igh **V**oltage, **H**igh **H**umidity, **H**igh **T**emperature, **R**everse **B**ias) at 90% of the nominal voltage. But, it is questionable if the chips are just too robust or if the test is not triggering the relevant failure mechanisms. From this point of view, multiple options for accelerating the test are feasible:

- Harsher constant climate [1]
- Cycled climate, condensation [3,4]
- Cycled voltage [4,5]
- Multi-stress testing [5,6]

All of the said options will change the acceleration factor compared to the standard testing at 85°C and 85% relative humidity (rel. h.). But, the acceleration due to the modifications is unclear and so are the triggered failure mechanisms. For SiC-devices, the multi-stress testing with a combination of power cycling testing (PCT) and HV-H³TRB was already part in a number of publications [6,7] and is therefore one of the modifications with an existing data base. Overall, this experiment is performed to find a crosslink between these two different lifetime-limiting stress factors. Delamination effects and microcracks of the insulation materials might influence the humidity performance, while the humidity related degradation, corrosion, oxidation of the interconnect metals or the housing material can change the thermo-mechanical behaviour.

Fig. 1. Image of a device under test. The DUTs feature an AlN substrate, a copper baseplate and were produced by Mitsubishi Electric Corp. as engineering samples. They are fabricated with traction rated materials and produced on the same line as the standard modules. The footprint of the package is 125 mm by 60 mm. The module is populated with 3.3k V SiC MOSFET chips with a nominal R_{DSon} of 40 mΩ.

Test Conditions and Procedure

Multi-stress testing is a way to close the gap between highly accelerated and application relevant testing. The combination of thermo-mechanical and electro-chemical stress was already part of previous works, but the results were not fully conclusive. A test campaign was carried out on a baseplate-less package type with SiC-MOSFETs in [6], where no influence of this multi-stress testing could be found. In contrast, the investigations in [7] show a significant influence of HV-H³TRB pre-conditioning on the power cycling performance. In this case, moulded discrete devices were used and especially pre-conditioning without bias voltage tend to reduce the lifetime in a PCT with a clear tendency to bond wire fatigue. Overall, all these previous investigations were executed on different package types (baseplate-less and discrete) with 1200 V MOSFETs and mixed results. Therefore, it is worthwhile to perform another campaign on that topic with 3.3 kV SiC-MOSFETs and traction rated interconnections.

HV-H³TRB Testing. Testing high power modules under accelerated humid conditions is well documented for Si-devices and more and more data has been gathered with SiC-devices in recent years. The results on Si-IGBTs showed a clear, measurable degradation behaviour and reproducible failure mechanisms [9,10], which can be solved by robust chip designs [9]. SiC-MOSFETs tend to show a significant difference in their degradation and failure pattern. First of all, well designed SiC-MOSFETs show a much higher life time in the HV-H³TRB test [2,11,12] and the test time can exceed 10 times the standard of 1000 h. Overall, the standard conditions of 85 °C and 85% rel.h. are not sufficient anymore to accelerate the aging process and obtain failures within a reasonable time frame. Nevertheless, these conditions are the industry standard and provide a benchmark for any kind of advanced testing, in particular, to extend the data base with respect to the investigations in [2,12]. As shown in [13], the bias voltage significantly increases the acceleration in humidity testing and can be used to stress the devices even further. Due to the high testing time, already reported in the past [12], an increase to 90 % V_{nom} (2.97 kV) can shorten the time to failure as shown in [1,13], but this is not proven yet for SiC-MOSFETs [2]. The overall procedure of humidity testing is well documented [2,9,10,13] and a combination of leakage monitoring throughout the testing and intermediate blocking curve measurements after defined time steps is utilised.

Table 1. Test splits with their corresponding conditions and further usage for multi-stress testing after pre-conditioning

Split	Test Conditions	Pre-con. samples	Pre-con status
HV-H³TRB SiC	**85 °C / 85 % rel.h. / 65% & 90% V_{nom}**	**6 / 14**	**1000h-4100h**
HV-H³TRB Si	**85 °C / 85 % rel.h. / 65% & 90% V_{nom}**	**6 / 6**	**600h-4100h**
PCT-SiC	**ΔT_{vj} = 50-100 K**	**8 / 10**	**EoL**
PCT-Si	**ΔT_{vj} = 70 K**	**4 / 8**	**> 235 kc**

The protection of the device in case of a failure event or a leakage current rise is a critical moment in the test and to avoid excessive damage, a highly sensitive monitoring system is used. A fast turn off procedure is assured with a transimpedance amplifier current measurement and an IGBT-half-bridge.

Power Cycling Testing. The situation of PCT for Si-devices is well documented and widely accepted in terms of degradation mechanisms [15] and modelling [16,17]. For SiC-devices, the database is not as solid and still subject to research. The overall lifetime of SiC-devices is shorter in PCT compared

to their silicon counterparts [8] in the same package. This is due to the higher Young's Modulus [15] and the resulting higher thermo-mechanical stress on the interconnections. In [8], 1.2 kV SiC-MOSFETs were compared to their Si-IGBT counterparts in identical packages (baseplate-less, DBC-substrate, Si-gel insulation), resulting in an up to five times higher lifetime for the IGBTs. This gap can be closed by improved packaging methods such as sintering and bond buffers [18], which will lead to even higher costs for the final product. While the failure mechanisms (die attach degradation and bond-wire lift-off) for both semiconductor types are the same, the modelling of the failure for Si-devices is not fully applicable for SiC-devices. For Si-IGBTs, the CIPS 08 model [16] is commonly used to model the failure times with respect to the temperature swing (ΔT_{vj}). While testing, the virtual junction temperature (after pre-test calibration) as well as $V_{DS,on}$ are monitored. The gate voltage (V_{GS}, V_{GE}) was set to +15 V / -12 V to ensure a fully closed channel in the SiC-MOSFETs. The failure criteria in the PCT are slightly different for SiC- and Si-devices and therefore, a distinction is mandatory. Both device types will use the 15 % increase in R_{th} as a failure criterion for solder degradation, but for bond-wire lift-off the standard criterion for Si-devices can be misleading. SiC-MOSFETs tend to show a drift in the threshold gate voltage (V_{th}) over time, and this can result in a change in $V_{DS,on}$ without any corresponding degradation in the thermal or electrical path. To avoid such issues, the use of a fixed threshold in $V_{DS,on}/V_{CE,on}$ is not recommended but the detection of a steep increase of the forward voltage is used to detect any bond-wire failure. To verify the existing database, the Si-IGBTs are used as a reference for the modelling. The verification of the package and the general degradation behaviour, the SiC-MOSFETs are stressed at different temperature swings, which should reproduce the results from [17].

Multi-Stress Testing. Both reliability tests were carried out independently from each other and the pre-conditioned devices were afterwards used vice versa. Due to the inconclusive database of previous publications [6,7], a high impact of the pre-conditioning is desirable and therefore, an end of life (EoL) preconditioning was aimed for. This kind of pre-conditioning is critical and excessive damage (gate rupture, cell short, edge termination breakdown, etc.) of the devices needs to be avoided. While the EoL in PCT is easily achieved in short periods of time, this is not true for the humidity testing. As shown in [2] with the same devices, the lifetime in the HV-H³TRB test is much higher for SiC-MOSFETs compared to their silicon counterparts and an EoL was not reached in an acceptable time frame. The overview of the different test splits is shown in tab. 1 with the corresponding pre-conditioning states. It is expected from the results in [2], that the IGBTs will deliver a convincing result in an exactable time frame in both tests. As stated before, the EoL-testing is critical for the subsequent test procedure and therefore, the number of samples after the PCT reduced to 4 Si-IGBTs and 8 SiC-MOSFETs due to failures in the other devices. The pre-conditioning in the HV-H³TRB test did not cause any critical failures and 6 SiC-MOSFETs were removed from the test already after 1000 h and 4500 h to continue with the PCT.

Table 2. Results of the PCT of the Si-IGBTs for ΔT_{vj} = 70 K

DUT	Load Current [A]	$\Delta T_{vj,init}$ [K]	Cycles to Failure [kc]	Failure Mode
Si-70K-01	**107.5**	**69.3**	**225.0**	**BW**
Si-70K-02	**107.5**	**68.5**	**235.0**	**BW**
Si-70K-03	**107.5**	**75.0**	**202.3**	**BW**
Si-70K-04	**107.5**	**70.1**	**170.0**	**BW**

Results of the Power Cycling Test

The reference test was performed on Si-IGBTs at ΔT_{vj} = 70 K and was interrupted after half of the population failed in PCT (4 samples). These modules tend to fail with excessive damage in the PCT and therefore, failed devices were not usable for any further investigations. Nevertheless, the results of the reference test are shown in tab. 2 with the last device failing at 235 kc (kilo-cycles) and this leads to a pre-conditioning state of the Si-IGBTs of > 235 kc. The situation for the SiC-MOSFETs is slightly different due to the variation in temperature swings and the results are shown in fig. 2.

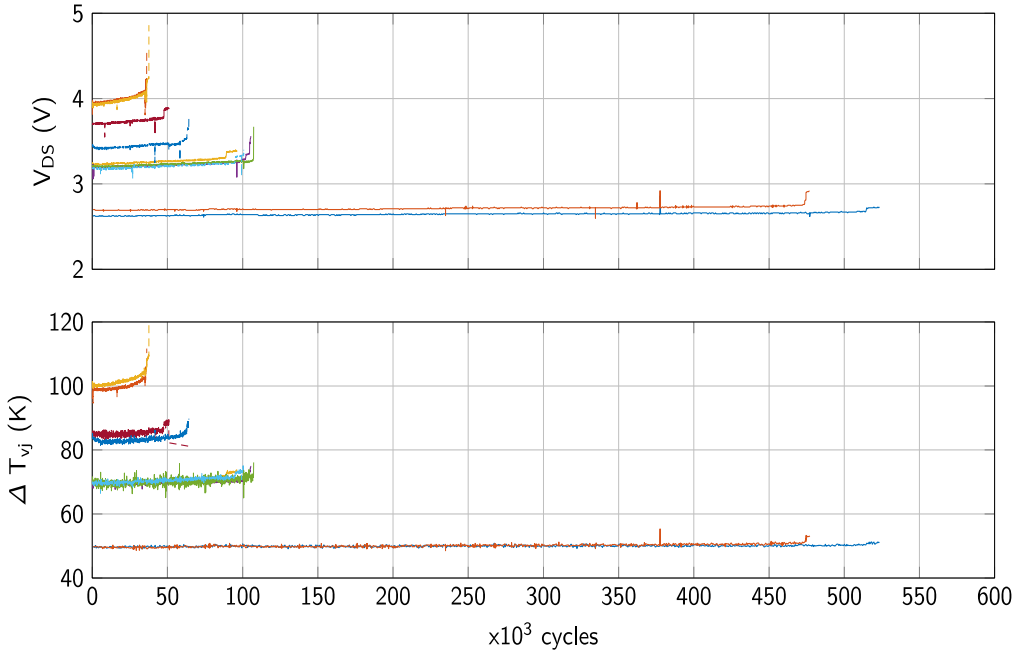

Fig. 2. V_{DS} and ΔT_{vj} during the PCTs for all SiC-DUTs. The DUTs, which were tested at higher temperature swings exhibit a higher V_{DS} due to the higher load current. All DUTs exhibit a step increase in V_{DS}, indicating bond wire failure.

The failure mode is consistent for all devices (IGBT and MOSFET) and it is found to be bond-wire lift-off (increase in $V_{DS,on}$ / $V_{CE,on}$). Overall, the lifetime changes dramatically if lower temperature swings (50 K) are applied, which fits to previous publications [17]. Furthermore, the lifetime of the SiC-MOSFETs is lower by about a factor of two, which is a smaller deviation compared to results from low voltage devices [8]. To verify the procedure as well as the devices, the results were fitted with respect to the simplified CIPS'08 [16] model in fig. 3. The Si-IGBT's lifetime can be fitted with the model and show an acceptable result with an adjustment of parameter K'. The same model cannot fit all the SiC-MOSFET results (fig. 3). For ΔT_{vj} = 50 K & ΔT_{vj} = 70 K, a modelling approach with just an adjustment of K' is possible but, the lifetime at ΔT_{vj} > 70 K is underestimated that way. If the complete model is fitted to $\Delta T_{vj} \geq$ 70 K, it underestimates the lifetime at ΔT_{vj} = 50 K, but can model the higher ΔT_{vj}., though with a very low β_1 value (slope). Possible remedies for that issue were discussed in publications like [17] and are not part of this work.

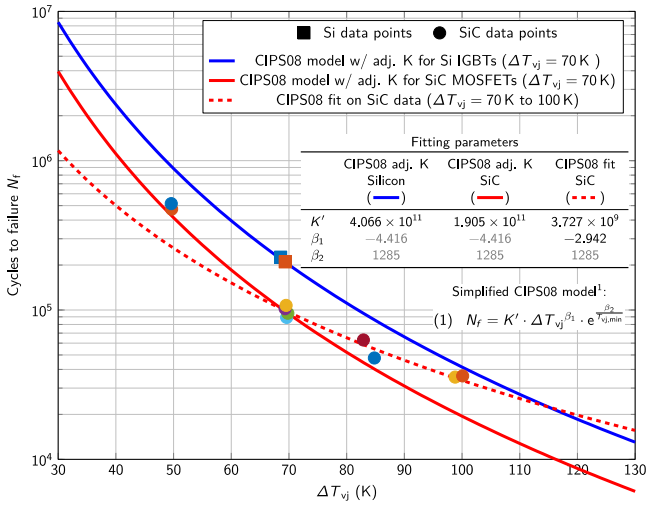

Fig. 3. Test results and corresponding lifetime plots for all DUTs. The lifetime curves were obtained by the original parameters and an adjusted K' factor to meet the data points at ΔT_{vj} = 70 K, indicated by solid lines, as well as a parameter fit on the test data for the SiC MOSFETs for ΔT_{vj} between 70 K and 100 K to the simplified CIPS08 model (inset equation 1), indicated by the red dashed line.

Discussion. The Si-IGBTs yield about the expected results. This confirms the validity of the experiment and also the correct failure mechanism. The results of the SiC-MOSFETs are in good agreement with previous test campaigns, but with a lower difference between Si- and SiC-devices compared to low voltage devices [12]. Applying a lower temperature swing results in a deviation from the model, which was previously reported and shows the correct failure pattern for these devices. The fitted model approach in fig. 3 (red dashed line) for $\Delta T_{vj} \geq 70$ K, allows a normalisation procedure to fit all values on one temperature swing and compare it to the other pre-conditioned devices. 8 out of 10 SiC-MOSFETs were able to perform in the HV-H³TRB test for further testing after EoL was reached.

Results of the HV-H³TRB Test

As stated before, the results of the accelerated humidity testing under high voltage bias is the continuation of the results from [2], with more devices added to test for the PCT pre-conditioning. Within the accumulated test time of more than 6,000 h, the EoL of the SiC-MOSFETs was not reached and not even degradation was observed. While the Si-IGBTs reproduced their expected lifetime from previous investigations [9,10,13], the SiC-MOSFETs show a highly extended lifetime, which is in good agreement with results on low voltage devices [12]. To compare different groups in the HV-H³TRB, the graph in fig. 4 (right) was found to be useful. At every intermediate measurement, the blocking curve of each device is taken at room temperature (fig. 4 (left)) to monitor the degradation in addition to the online leakage monitoring. The measurement is stopped after reaching the avalanche inception voltage (steep rise of the leakage current) to avoid damage.

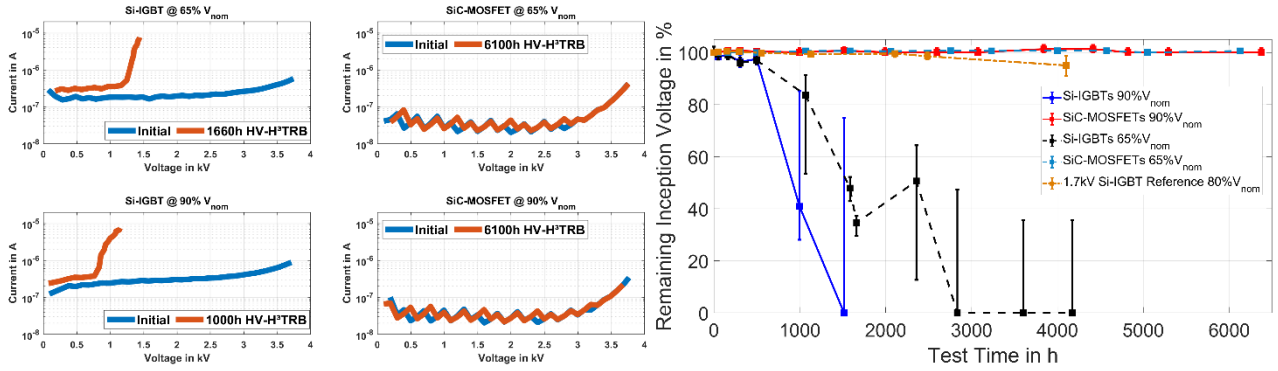

Fig. 4. Blocking curves with different test time after drying at room temperature (left picture), normalised remaining inception voltage over testing time for Si-IGBTs and SiC-MOSFETs at different voltage biases (right picture)

This resulting voltage level is used in the graph in fig. 4 (right) to illustrate the median of the inception voltage with the corresponding 25 % and 75 % quartiles of the test group. With increasing test time, the voltage level decreases and acts as a measure of the degradation over time. The voltage acceleration for the Si-IGBTs between 65 % and 90 % V_{nom} is around a factor of 1.7, which is in good agreement with previous investigations [13]. In fig 4 (right), a 1.7 kV Si-IGBT reference (85 °C / 85 % rel.h. / 80 % V_{nom}, [9]) is added to show the outstanding humidity robustness of modern SiC-devices compared to even highly (reliability) optimised Si-IGBTs.
The last IGBT was excluded from the test after 4,100 h of accumulated test time (long-runner [13]) and all the IGBTs could be used for the PCT as pre-conditioned devices. After 2,000 h of accumulated test time, 6 SiC-MOSFETs were added to this test at 90 % V_{nom} to enable the multi-stress testing without stopping the EoL-testing of the first SiC-MOSFET reference samples. 3 of these devices were removed after 1,000 h, and the other 3 after 4,100 h in the humidity chamber.

Table 3. Multi-stress testing splits with test conditions and quantities

Split	Si-IGBTs	SiC-MOSFETs	Test Conditions
HV-H³TRB after PCT	**4**	**8**	**85 °C / 85 % rel.h. / 90% V_{nom}**
PCT after HV-H³TRB	**7**	**7**	**ΔT_{vj} = 70 K**

Discussion. The results of this HV-H³TRB testing reproduce the results from previous investigations with the clear conclusion, that the accelerated test conditions under 85 °C, 85 % rel.h. and high voltage bias close to the nominal voltage are not accelerating the aging of SiC-devices, such that failures occur within a reasonable time frame. As already shown in [2], it is unclear if well designed modern SiC-MOSFETs are too robust or if test conditions are not suitable anymore. Static test conditions are not application relevant and focused on the acceleration of certain mechanisms. For example, the Al-corrosion at the edge termination of the chip, described in [9,10,13], is not of interest for SiC-devices due to the different edge-termination design. Therefore, dynamic test conditions such as the AC-HTC [4] and the dynamic H³TRB [5] (pulsed DC instead of constant voltage) might be more relevant for SiC-devices, but are still subject of research activities.

Multi-Stress Testing: Interaction between Thermo-Mechanical and Electro-Chemical Stress

To find an evidence of the interaction between the two different stresses, the pre-conditioned devices were stressed in the corresponding second test procedure. The samples were split according to tab. 3 with respect to the respective pre-conditioning status (tab. 1).

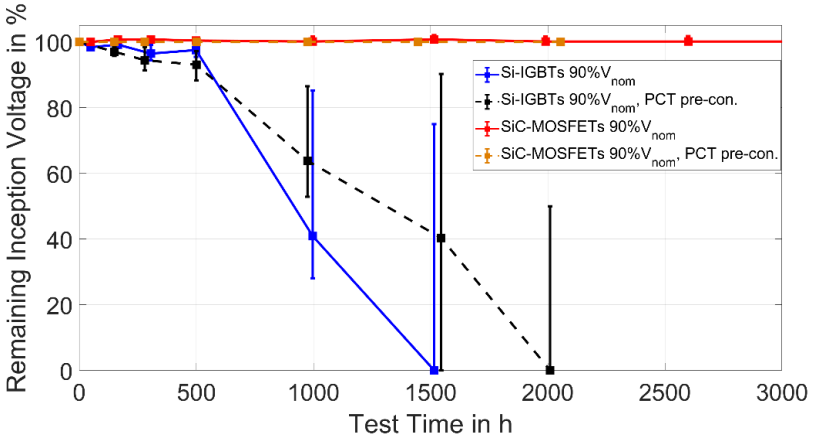

Fig.5. Normalised remaining inception voltage over testing time for Si-IGBTs and SiC-MOSFETs with and without PCT pre-condition

HV-H³TRB after PCT. The test conditions for this combination are identical to the initial humidity testing at 85 °C and 85 % rel.h.. Due to the high robustness of the SiC-MOSFETs, the bias voltage was set to 90 % V_{nom} to achieve a maximum acceleration without changing the climate. Fig. 5 shows the results of 2,000 h of testing in the same manner like fig. 4 (right), with the normalised avalanche inception voltage over testing time. The Si-IGBTs reproduced their initial results with even slightly better performance after pre-conditioning. Reliability-wise, this makes no sense, but the hand-picking of pre-conditioned samples based on an electrical characterisation before the test might have made them "statistically closer" to each other compared to the initial group of IGBTs. Furthermore, an early failure occurred in the initial HV-H³TRB test and therefore, the curve (blue solid line) in fig. 5 is shifted to lower testing times. Overall, both test groups are within the scattering of their counterparts and no significant influence of the pre-conditioning can be found. The situation for the SiC-MOSFETs is identical to the initial results with no degradation in the first 2,000 h.
In summary, the data in fig. 5 shows no significant impact of the PCT pre-conditioning and it is impossible to accelerate the humidity induced degradation to achieve EoL.

PCT after HV-H³TRB. For the PCT after electro-chemical pre-conditioning, a ΔT_{vj} = 70 K was chosen for both the Si-IGBTs and the SiC-MOSFETs. The failure mechanism (bond-wire lift-off) remained the same for all devices within the second test and the results of the Si-IGBTs are shown in fig. 6 and tab. 4. The test split of 6 pre-conditioned Si-IGBTs was extended with another sample, which remained unbiased in the chamber for 4,100 h (Si-70K-021) as a reference to the result in [7].

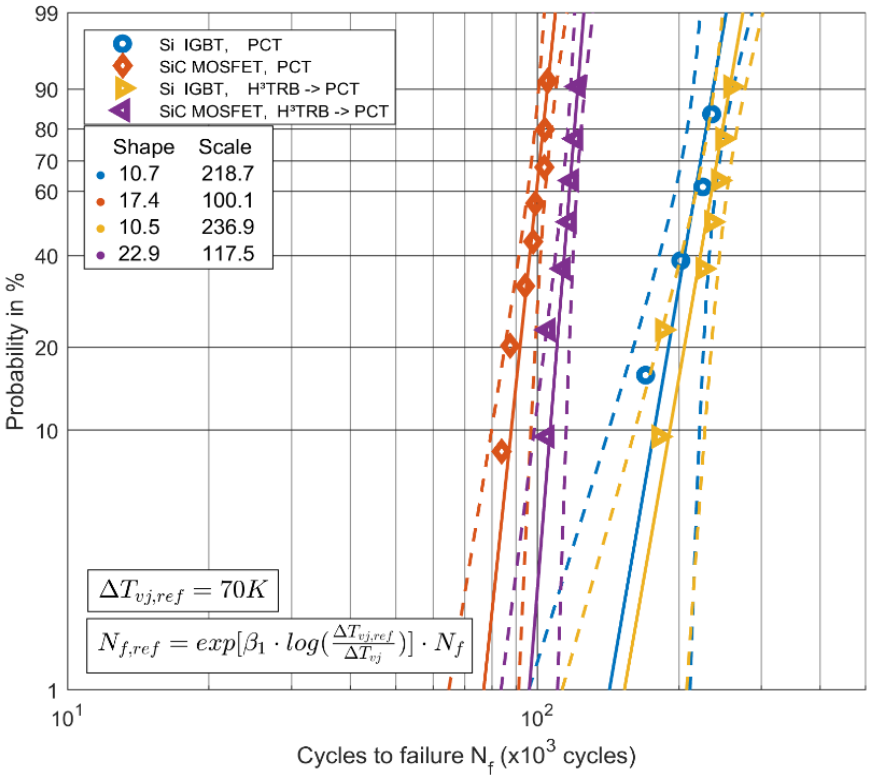

Fig. 6. Weibull distribution for the PCT after HV-H³TRB pre-conditioning with both device types. The failure rates of the initial PCT with SiC-MOSFETs were normalised to ΔT_{vj} = 70 K with respect to the parameters from fig. 2

From the data in fig. 6 and tab. 4, no significant influence of the humidity pre-conditioning can be determined. Both test groups show a similar failure rate and are within their respective confidence intervals. Furthermore, a tendency to a higher lifetime in PCT is linked with a higher pre-conditioning time in the HV-H³TRB, but this is more likely a statistical artefact. The exact same evaluation was done for the SiC- MOSFETs in fig. 6 with a normalisation of the initial PCT result to ΔT_{vj} = 70 K via eq. 2:

$$N_{f,ref} = \exp[\beta_1 \cdot \log(\frac{\Delta T_{vj,ref}}{\Delta T_{vj}})] \cdot N_f \quad (2)$$

This calculation leads to the results in fig. 6 with the corresponding Weibull distribution of the pre-conditioned (orange line) and initial (purple line) devices. Similar to the Si-IGBTs, no influence of the pre-conditioning can be stated and even the unbiased reference (SiC-70K-20) is not able to reproduce the data shown in [7].

Table 4. Cycles to failure for all devices at ΔT_{vj} = 70 K with respect to their pre-conditioning state

DUT	Pre-Con	Cycles to Failure [kc]
Si-70K-022	**4100h @ 65%**	**257.9**
Si-70K-021	**4100h @ 0%**	**248.1**
Si-70K-033	**2358h @ 65%**	**243.0**
Si-70K-023	**1662h @ 90%**	**234.9**
Si-70K-039	**996h @ 90%**	**225.0**
Si-70K-004	**1661h @ 65%**	**184.7**
Si-70K-007	**551h @ 90%**	**181.4**
SiC-70K-26	**1000h @ 90%**	**122.2**
SiC-70K-39	**1000h @ 90%**	**120.7**
SiC-70K-22	**4100h @ 90%**	**118.3**
SiC-70K-30	**4100h @ 90%**	**117.0**
SiC-70K-35	**4100h @ 90%**	**113.5**
SiC-70K-24	**1000h @ 90%**	**105.3**
SiC-70K-20	**6100h @ 0%**	**105.0**

Discussion. This experiment was executed to detect an interference of thermo-mechanical and electro-chemical pre-conditioning on the lifetime in PC and HV-H³TRB tests. From the data in fig. 5 and fig. 6, no significant impact can be found, which is reproducing the data shown in [6]. Moreover, the pre-conditioned devices tend to survive longer in the second test, compared to the initial results. In the humidity test, both Si-IGBT splits are within their scattering and the same is true for the Si-IGBT Weibull distributions in fig. 6. Only SiC-MOSFETs show a small, though not really significant effect. The shape factors in fig. 6 indicate a low scattering in failure times and therefore, the time to failure can be assumed to be accurate for this test vehicle. Nevertheless, the consecutive testing with engineering samples can influence the statistical result and therefore, the result might change if the testing is repeated with fully qualified products in higher number.

Conclusion and Outlook

In this work, the interaction between thermo-mechanical and electro-chemical stress was investigated with 3.3 kV Si-IGBTs and SiC-MOSFETs in identical packages. The performance in the PCT showed an expected result with a higher lifetime for the Si-IGBTs but with a smaller deviation from the SiC-MOSFETs compared to previous investigations on low-voltage devices [8]. Applying thermo-mechanical stress at low temperature swings significantly shifts the lifetime estimation to higher cycles to failure and is therefore, not fully represented in standard silicon models. Overall, PCT could be performed successfully on this engineering package and the corresponding pre-conditioning was applied to the devices. In terms of humidity testing, the Si-IGBTs reproduced the expected result with significant earlier failure rates compared to their SiC-counterparts. The SiC-MOSFETs demonstrate a very high robustness under standard 85 °C / 85 % rel.h. conditions with a lifetime of more than 6,000 h without signs of degradation.

A combination of both stresses with consecutive PC and HV-H³TRB testing did not yield any significant finding. The PCT pre-conditioning was not accelerating the degradation of the SiC-MOSFETs and within > 2,000 h no degradation was observed. A reference test on Si-IGBTs just reproduced the initial result. Vice versa (HV-H³TRB pre-conditioning), the IGBTs reproduced their initial result without any influence of the pre-conditioning status, while the SiC-MOSFETs showed even a slightly higher lifetime. This effect might be related to the test procedure and the experimental character of the investigation. And still, no influence of the pre-conditioning was found, despite a factor of 4 in the pre-conditioning duration.

Considering the data of this investigation and the data for low-voltage baseplate-less modules published in [6], there is no cross-link between PCT and HV-H³TRB. This might be different for discrete devices as shown in [7] but, for Si-gel insulated multi-chip modules no effect could be identified. On the one hand, the combination of these two stresses (either sequence) is not accelerating the degradation and therefore, it is not contributing to an improved test concept. On the other hand, the experiment has shown that the separate investigation of the two stresses is not overlooking a potential source of field failures due to an interference.

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