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Ohmic Contact Resistance in SiC Diodes with Ti and NiSi P^+ Contacts

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Abstract. Ohmic contacts play a major role in the signal transfer between the semiconductor device and the external circuitry. One of the main technological issues to develop high-performance SiC-based devices is the control of metal/SiC contact properties to fabricate low resistance and high stability SiC Ohmic contacts to p-type SiC. This is mostly due to intrinsic SiC characteristics like large work function, low dopant activation for p-type materials and low hole mobility. These limits are even more emphasized in SiC JBS or MPS diodes, where Schottky and Ohmic contacts on the P doped regions embedded in the active area to improve surge ruggedness are usually formed by using the same metallization process. This naturally results either in a high Schottky barrier height in the Schottky contact with consequent increase of the conduction loss at low currents or in a poorly conductive Ohmic contact, leading to reduced IFSM capability. Therefore, the optimization and control of the process parameters like for example the P^+ doping concentration peak underneath the metallization layer and the annealing process temperatures is crucial to obtain a good Ohmic contact and enhance the device´s robustness against surge current.

Introduction

4H-SiC is an attractive semiconductor for high-power and high-temperature electronic applications, due its outstanding material properties such as wide band gap, high critical breakdown electric field, good electron saturation velocity, high thermal conductivity and chemical inertness [1]. Power diodes are present in most of the power electronic circuits. Surge capability has been regarded as one of the most important parameters for this type of devices. Diodes in fact can potentially undergo a high surge current in some situations, potentially leading to early failures triggered by a thermal runaway behavior [2].

4H-SiC merged-PIN-Schottky (MPS) diodes have been demonstrated to provide enhanced surge current capability [2]. MPS diodes are a combination of PIN and Schottky diodes that exhibit high current density conduction capability with fast switching characteristics and low recovery losses. Under normal operation mode at the rated current, the diode is unipolar and the whole current is carried out by the Schottky regions. At higher current levels, the PIN-diode is switched on and the device turns bipolar, by increasing energy dissipation and surge current capabilities [2-3].

The minimization of the P^+ ohmic contact resistance is crucial to reduce the forward voltage drop (V_F) in bipolar conduction, maximizing the surge current ruggedness. A challenging issue currently limiting the processing is the manufacturing of rugged low-resistance Ohmic contacts to p-type 4H-SiC. This is mainly caused by the large p-type semiconductor work function, due to the 4H-SiC wide band gap and high electron affinity (both around 3.2 eV). Another important limitation comes from the technology used for forming contacts in MPS diodes. In such a kind of devices Schottky and Ohmic anode contacts are in fact usually formed by using the same metallization process, which results either in an unsought high Schottky barrier in the Schottky contact or in a poorly conductive Ohmic contact [4-5]. The optimization of process parameters used for ohmic contact formation plays a key role to minimize the P^+ specific contact resistance (ρ_C) and increase robustness against surge current. Several DOEs were carried out to better understand the correlation between ρ_C and relevant process parameters like annealing temperatures, P^+ implant dose and drift layer doping. Here, we

report on the Ohmic contact characteristics of 4H-SiC PIN and MPS diodes with one single Ti metal layer for both Schottky and Ohmic contacts and different Ti and NiSi metal layers used for Schottky and Ohmic contacts, respectively.

Experimental Results

650V 4H-SiC PIN and MPS diodes with 50% Schottky/PIN area ratio were used to measure the voltage drop variation (V_F) in different conduction regimes, as result of the different process DOEs used for this study. In particular, the voltage drop was measured on PIN diodes at wafer level at relatively low current < 20A and on MPS diodes at package level at higher current in bipolar regime up to 80A. PIN diodes were used as test vehicle for the characterization to use wafer level parametric test data only available at relatively low forward currents, given current testing setup limitations. All the diodes investigated in this work have an area of 2.2 mm^2, were included in the same multi-project-wafer and fabricated during the same manufacturing process. The P^+ specific contact resistance (ρ_C) was determined by characterizing the current-voltage relation from transmission line method (TLM) measurements carried out on dedicated test structures included in the mask set for process control monitoring [6]. An Al-doped P^+ enrichment layer was implanted at high temperature (T) (>500°C) and dose (100% Ref~$3x10^{15}$ cm^{-2}) inside the P wells in the active area to create a low resistivity ohmic tunnel contact. Unless otherwise stated, the Ti contact was annealed at T=550°C after metal deposition. A 4H-SiC MPS diode schematic cross-section and typical IV forward characteristics measured on 4H-SiC PIN and MPS diodes investigated in this work are reported in Fig.1.

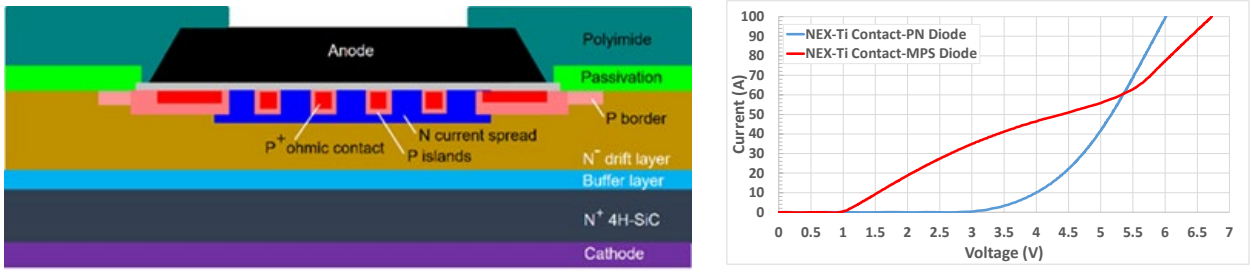

Fig.1. 4H-SiC MPS diode schematic cross-section (left) and typical IV forward characteristics measured on 4H-SiC PIN and MPS diodes used for the P^+ contact resistance study (right).

The doping concentration peak underneath the metallization layer and the annealing process temperatures are extremely sensitive parameters to obtain a good Ohmic contact. To this purpose, process splits were carried out to study the ρ_C and the V_F variation at 10A on PIN and MPS diodes with single Ti anode contact layer, as a function of the temperature and time used for the dopant activation annealing (Fig.2), SiC consumed thickness during surface etching processes following the high temperature activation annealing (Fig.3) and Schottky annealing temperature (Fig.4). Additionally, the V_F variation was measured on PIN and MPS diodes manufactured on epitaxial wafers with different drift layer doping with the purpose to study the dependence of the voltage drop on the injection efficiency of the PN junctions in bipolar regime (Fig.5).

The P^+ specific contact resistance shows a marked decrease with the activation annealing temperature from $7.6x10^{-3}$ Ωcm^2 at 1700°C to $3.4x10^{-3}$ Ωcm^2 at 1770°C, both processes with 30 min duration. A similar trend was measured on PIN diodes V_F. No significant dependence was observed instead on the duration of the activation process at fixed annealing temperatures (Fig.2). High temperature annealing processes increase the activation of Al dopant in the P^+ wells, by reducing in this way the P^+ contact resistance. However, special care must be considered in case annealing temperatures higher than 1700°C are used, due to possible dislocation formation in the epilayer induced by stress effects, potentially leading to the degradation of bipolar device performance during forward biased operation [7]. A dopant activation anneal process at 1700°C with 30 min duration was used in all the subsequent experiments described below in the paper.

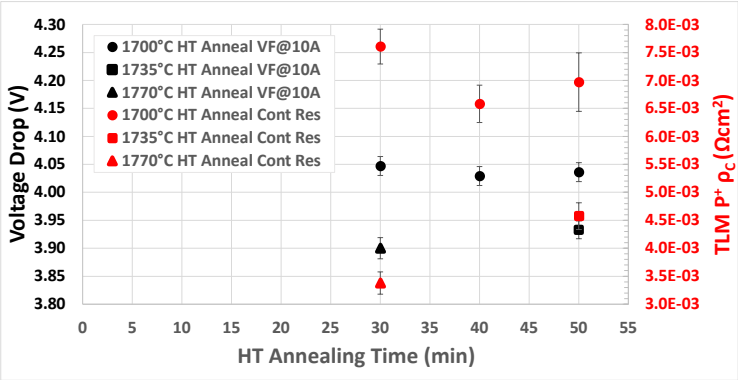

Fig.2. 4H-SiC PIN Diodes V_F at 10A (left y-axis-black data points) and TLM Ti P^+ contact ρ_C (right y-axis-red data points) as a function of the dopant activation annealing temperature and time.

A contact resistance reduction up to almost 80% (from 5.5x10^{-3} Ωcm^2 to 1.2x10^{-3} Ωcm^2) was obtained by removing a thin SiC surface layer, about 60 nm thick, after the high temperature activation process (Fig.3). The etching process allows to further improve the ohmic contact between Ti metal layer and P^+ implant peak, by reducing the tunnel barrier width. Plasma etch, sputter etch, sacrificial oxidation followed by thermal oxide etch or a suitable combination of these processes can be used to this purpose. In the specific case, ρ_C and V_F decrease is more consistent by removing thinner SiC surface layers up to 40 nm thickness while the improvement is more limited by further increasing the etched layer thickness up to 60 nm. It is clear that to make this solution sustainable in an industrial environment, attention needs to be taken to setup etching processes allowing to remove in a controllable and repeatable way very thin SiC surface layers with thicknesses of only few tens of nanometers, depending on the profile and peak of the P^+ implant.

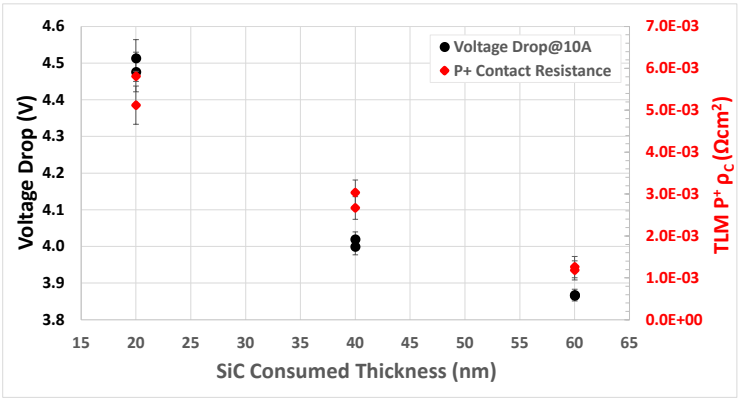

Fig.3. 4H-SiC PIN Diodes V_F at 10A (left y-axis-black data points) and TLM Ti P^+ contact ρ_C (right y-axis-red data points) as a function of the SiC surface thickness etched after the high temperature dopant activation annealing process.

A substantial P^+ specific contact resistance decrease was also measured by increasing the Schottky annealing temperature from 530°C (ρ_C=5.5x10^{-3} Ωcm^2) to 730°C (ρ_C=3.8x10^{-3} Ωcm^2) (Fig.4). A V_F decrease compatible with ρ_C reduction was observed on PIN diodes. On the contrary, the V_F at 10A shows a relevant increase on MPS diodes (from 1.51V at 530°C to 1.73V at 730°C), due to the increase of the Schottky barrier height induced by the higher temperature annealing process. At low current levels, in fact, the forward current in MPS diodes is just generated by the Schottky regions, as PIN diodes are triggered only above ~3V threshold voltage [3]. Therefore, in line with the expectations, these measurements confirm that, in SiC MPS diodes with one single metal layer for Schottky and P^+ ohmic contacts, there is an unavoidable trade-off between the need to lower barrier height and voltage drop in unipolar Schottky regime and that to reduce the P^+ ohmic contact resistance to enhance surge ruggedness in bipolar regime [4]. In this framework, lower temperature Schottky annealing processes are usually preferred to reduce as much as possible conduction losses at low currents in Schottky regime where SiC MPS diodes operate in application during most of their lifetime [8].

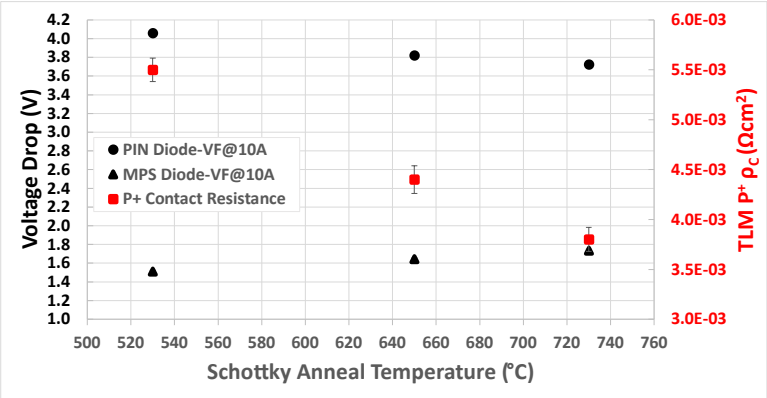

Fig.4. 4H-SiC PIN and MPS Diodes V_F at 10A (left y-axis-red data points) and TLM Ti P^+ contact ρ_C (right y-axis-red data points) as a function of the Schottky annealing temperature.

A significant V_F decrease was measured in bipolar regime on PIN diodes by reducing the doping of the drift layer (Fig.5). The decrease is quite consistent below $1.2x10^{16}$ cm^{-3} doping while it shows a kind of saturation above $1.5x10^{16}$ cm^{-3}. The decrease of the drift layer doping reduces the built-in voltage of the PN junctions, by increasing the injection of bipolar current at lower forward bias. For lower doping values this effect is further amplified by the conductivity modulation mechanism triggered by the injection of minority carriers (i.e. holes) into the high-resistance drift region, causing its resistivity and consequently the voltage drop to further decrease [9]. In contrast, in MPS diodes the V_F increases quite consistently for low epitaxial layer doping. In this type of device, in fact, only the Schottky diode is turned on at 10A and the conduction loss increases, due to lower electrons mobility in the highly resistive drift layer [10]. In the doping range where the V_F starts to appreciably decrease in PIN diodes, the V_F increase in MPS diodes becomes very consistent, making it necessary to increase the die size or the Schottky/PIN ratio with not negligible impact on the device costs and surge ruggedness capability, respectively. These considerations make in first instance the reduction of the drift layer doping a not effective solution to improve surge ruggedness in 4H-SiC MPS diodes.

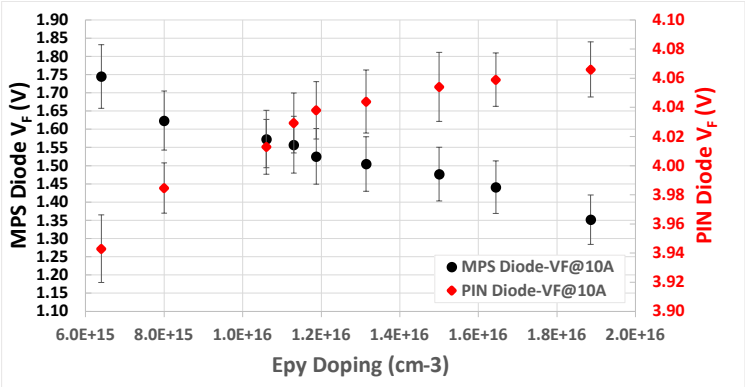

Fig.5. 4H-SiC MPS (left y-axis-red data points) and PIN (right y-axis-red data points) diodes V_F at 10A as a function of the drift layer doping.

The increase of the Al P^+ dose in the enrichment implant inside the P wells is potentially another suitable option to improve surge ruggedness in 4H-SiC MPS diodes. As shown in Fig.6, the increase of the P^+ dose from 100% to 200% produces an appreciable ρ_C reduction from $5.2x10^{-3}$ Ωcm^2 to $3.5x10^{-3}$ Ωcm^2 in PIN and MPS diodes with single Ti anode contact layer. However, it is also evident how the use of P^+ doses above a certain dose threshold (≈125%) consistently increases the leakage current (I_L) at 650V (Fig.7), due to the higher defectivity induced by the P^+ implant process. This indicates the need for fine-tuning the process parameters (e.g., implant and dopant annealing temperatures) to recover the damage generated by the higher dose P^+ implant.

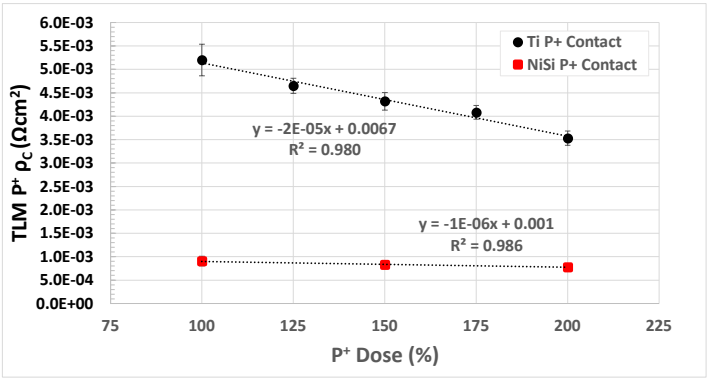

Fig.6. TLM Ti and NiSi 4H-SiC P^+ contacts ρ_C as a function of the P^+ dose (100% Ref. Dose~$3x10^{15}$ cm^{-2}).

On some prototypes a NiSi ohmic contact layer was formed on the P^+ wells through a rapid thermal annealing process carried out at T>950°C, following Ni layer deposition. In MPS diodes a Ti layer annealed at 550°C was still used for the Schottky contact. At 100% reference P^+ dose, ρ_C is about $9x10^{-4}$ Ωcm^2 with NiSi (Fig.6), so better than what measured in any process trial used to reduce the contact resistance with the single Ti contact and quite in line with some literature data [5,11]. The contact resistance dependence with the P^+ dose is much less prominent than with Ti contact while, also in NiSi case, a steep I_L increase at 650V was measured in the high dose range (Fig.7). No appreciable differences were measured in NiSi P^+ ohmic contact behavior for contact annealing temperatures higher than 950°C. A similar increase of the leakage current was also measured on MPS diodes, starting already from 400V reverse bias.

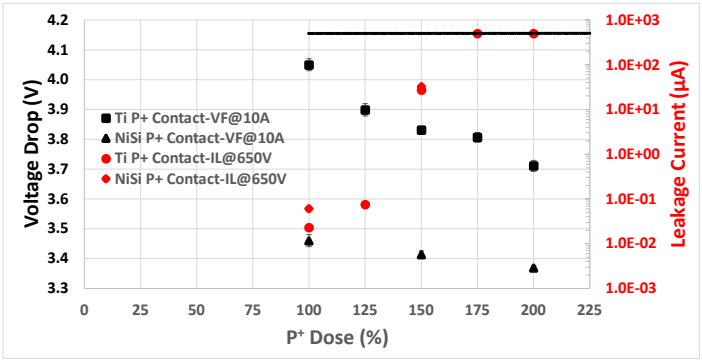

Fig.7. 4H-SiC PIN Diodes V_F at 10A (left y-axis-red data points) and I_L at 650V (right y-axis-red data points) as a function of the P^+ dose and metal contact. The black dashed line represents the compliance current level.

The effectiveness of the NiSi contact in reducing the V_F in bipolar regime is evident in the 650V-10A MPS diodes IV forward characteristics benchmark (Fig.8-Left).

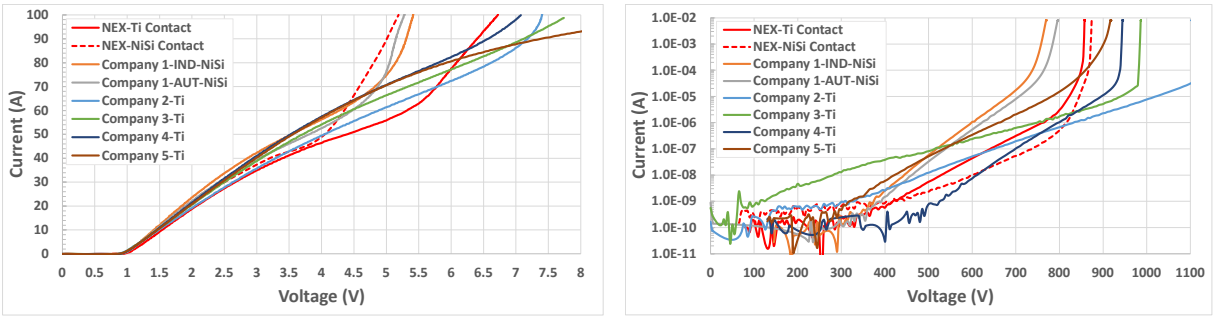

Fig.8. 650V 10A 4H-SiC MPS diodes I-V forward (left) and reverse (right) characteristics benchmark.

The IV measurements were carried out at package level on Nexperia (NEX) and competitor samples in TO-packages rated for 650V voltage class and 10A current. The V_F at 80A on Nexperia (NEX) samples is reduced from 6.1V with Ti to 4.8V with NiSi P^+ contact, in line or slightly better than company 1 state-of-the art automotive and industrial grade 4H-SiC MPS diodes (V_F≈5V), also

using NiSi for the Ohmic contact. No significant changes were observed instead in the IV reverse characteristics of samples with either Ti or NiSi P^+ contacts (Fig.8-Right).

Finally, IFSM destructive tests were done on some selected samples as a function of the temperature. The measurements were carried out by impinging diodes with single (SSS) and 50 Hz/100 cycles repetitive half sinus surge (RSS) current pulses with t_{pulse} = 10ms and 1A step up to the destruction level [12]. SSS values of 78.6A were measured at 25°C on NEX devices with NiSi P^+ contact, against 76.4A measured on company 1 diodes and 73A on NEX diodes with single Ti P^+ contact. The difference becomes more significant for repetitive surge tests where the use of a NiSi contact shows up to 20% higher surge ruggedness. RSS values of 66.1A were obtained in fact at 25°C on NEX diodes with NiSi P^+ contact, compared to 54.3A measured on NEX diodes with Ti P^+ contact. A lower IFSM capability but a similar comparative behavior was found at 150°C on all the tested devices (Fig.9).

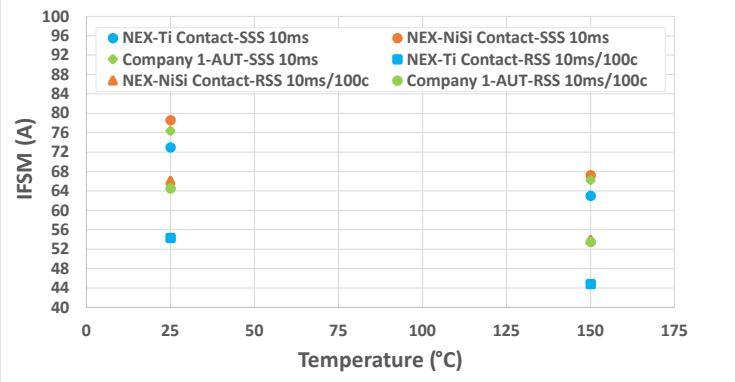

Fig.9. 650V 10A SiC MPS diodes 10ms single (SSS) and 100 cycles repetitive sinusoidal (RSS) surge destructive tests as a function of the temperature.

Reliability tests carried out on NEX 4H-SiC MPS diodes with Ti and NiSi P^+ contacts have proven how the technology with single Ti contact layer annealed at low T is extremely stable under high voltage, temperature, and humidity stress conditions. In contrast 4H-SiC MPS diodes with NiSi P^+ contacts have shown some weaknesses occurring during some high current and temperature tests, pointing to the need to optimize the process module for NiSi P^+ contact creation to increase robustness in harsh environmental conditions. This study, still ongoing, is not reported here for conciseness.

Conclusions

In summary, single Ti P^+ contacts annealed at low temperature (<550°C) and optimized for V_F reduction in Schottky regime can still provide rugged P^+ ohmic contacts with reasonably low contact resistance (ρ_C) and good surge ruggedness in 4H-SiC MPS diodes, despite this requires the optimization and tighter control of the process parameters for P^+ contact formation. The ρ_C can be substantially reduced by increasing the temperature in the annealing process used for dopant activation, by increasing the P^+ dose or by etching a thin SiC surface layer after the high T annealing, a few tens of nm thick depending on the P^+ implant doping and profile, such to create the contact between the metal layer and the P^+ implant peak. Special care must be taken to properly control all the relevant processes used for P^+ contact creation. Not optimized processes like, for example, too high P^+ doses eventually combined to relatively low P^+ implant or activation anneal temperatures or, on the other side, too high dopant annealing temperatures can result in deteriorated or not-stable performances, mostly due to defectivity increase.

Conversely, the use of a second metal layer (e.g. NiSi) annealed at high temperature (>950°C) for P^+ ohmic contact formation leads to a more consistent ρ_C reduction and enhanced repetitive surge current ruggedness without stringent requirements on process parameters like P^+ implant and activation anneal for contact optimization. However, preliminary results have shown how the process module used for creating NiSi P^+ contacts on 4H-SiC MPS diodes could be potentially critical for reliability, especially during high temperature and high current stress tests. This could make necessary

the adoption of more complex device architectures for NiSi P^+ contacts creation, with potential impact on process capability and cycle time.

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