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1.2 kV SiC MOSFET with Low Specific ON-Resistance and High Immunity to Parasitic Turn-On

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Abstract. With the capability to switch at high speed, there are important concerns about Parasitic Turn-On (PTO) when using SiC MOSFETs in switching applications with fundamental half-bridge configuration [1]. In this work, we present 1200V SiC planar MOSFETs with low specific ON-resistance (Rsp), fast switching characteristics and high immunity to PTO. The PTO immunity is verified by experimental comparison to several commercially available SiC MOSFETs.

Introduction

SiC MOSFETs are now widely used in numerous applications, especially automotive applications such as traction inverters and fast charging stations. Thanks to its superior physical properties, SiC MOSFETs are expected to operate with low R_{DSON} and fast switching condition. Nevertheless, under fast switching condition in half-bridge configuration, complementary device, i.e., Body Diode (BD) can experience unwanted PTO [1, 2].

PTO is described as an unwanted effect during MOSFET switch turn-on, i.e., BD turn-off. Here, while BD V_{DS} rising to take V_{DD}, device's internal nonlinear capacitances like C_{GS}, C_{GD} and C_{DS} are also in transient mode. Charging current from C_{GD} unwantedly charge C_{GS} as well as gate resistor R_{G_EXT}+ R_{G_INT} and pull-up the HS V_{GS}. If the HS V_{GS} is pulled over device's VTH, the BD channel will open under a high V_{DS} voltage. The HS V_{GS} pulled-up event during BD turn-off was described as [2]:

$$\frac{dV_{GS}}{dt} = \frac{1}{C_{GS}}\left[C_{GD}\frac{dV_{DS}}{dt} - \frac{V_{GS}}{R_G}\right] \quad (1)$$

Equation (1) qualitatively stated that, HS V_{GS} pull-up depend on device's C_{GS}, C_{GD}, switching speed and total R_G. There were efforts on design novel gate drivers to limit PTO when using SiC MOSFETs in switching application [3]. Therefore, from device design perspective, it is important to design and optimize the device structure to obtain SiC MOSFETs that are highly robust against PTO.

In this work, we introduce 1200V SiC MOSFETs with low R_{DSON}, fast switching characteristics and an optimized capacitance C_{ISS}/C_{RSS} ratio for a highly robust device against PTO.

Device Fabrication and Measurements Set-up

Planar implanted SiC MOSFETs with a total chip area of 24.6mm^2 and optimized cell design for 1200V were fabricated using 150mm SiC epitaxial wafers. Devices were then packaged and measured in TO-247-4L housing. A Keithley S500 integrated test system were used for DC measurements and pulsed high current measurements, using a pulse width of 230 µs. Double Pulse Tester (DPT) were used for switching measurements and PTO evaluation. In our switching measurements, the Low Side (LS) device is the active switch and High Side (HS) device is the BD.

Simplified device structure, measurements set-up and simplified circuit diagram were described elsewhere [4,5].

DC Characteristics

Fig.1a represents the typical measured device's transfer characteristics at RT and at 175°C, with V_{DS}=0.1V. Device's typical V_{TH} is 3V at RT and 2V at 175ºC, respectively (with V_D=V_G @I_D=33mA). Fig.1b shows measured output characteristics at RT and 175ºC, with V_{GS}=18V. Device's typical R_{DSON} is 12 mΩ at RT and 25 mΩ at 175ºC, respectively. The measured device will be referred as device #1 in following sections.

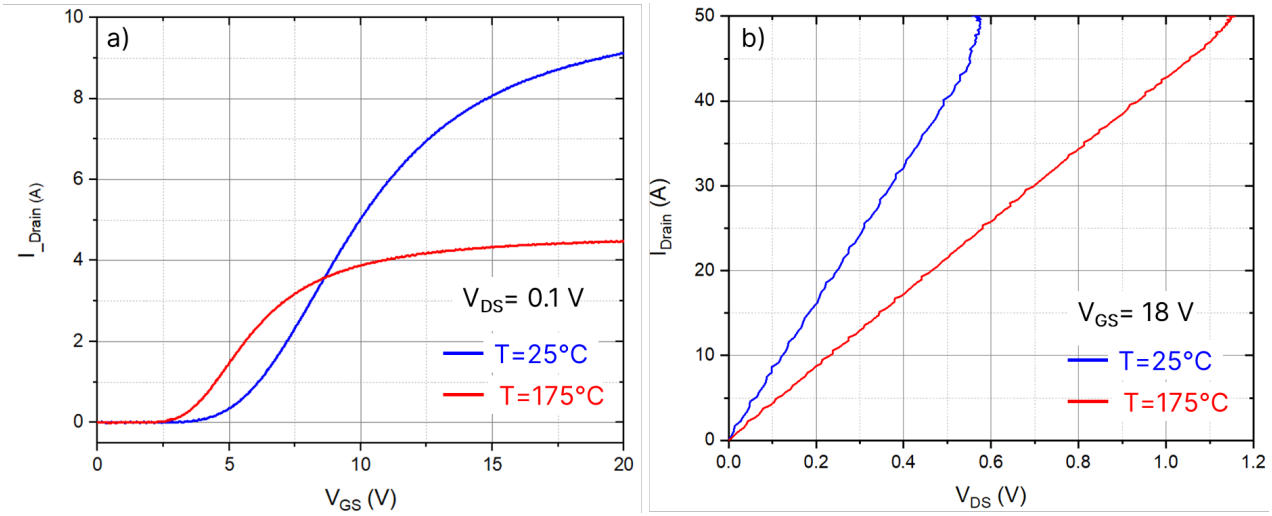

Fig.1a. Measured device #1 typical transfer characteristics at RT and 175°C, with V_{DS}=0.1V;
Fig. 1b. Measured device #1 typical output characteristics at RT and 175°C, with V_{GS}=18V.

Switching Characteristics

For switching evaluation, the same type of device as well as gate driver and R_{G_EXT} was always used on both high side (HS) BD and low side (LS) switch. Fig. 2 show the measured switching turn-on and turn-off characteristics of the device #1 with I_D=140A, corresponding to J=700A/cm^2. Fast switching characteristics is observed where the devices turn-off I_D=140A in less than 20ns, and turn-on at di/dt≈ 6A/ns with extracted E_{OFF}=1160µJ and E_{ON}=1280µJ, respectively. The observed oscillations are difficult to avoid in the DPT system for these fast switching events.

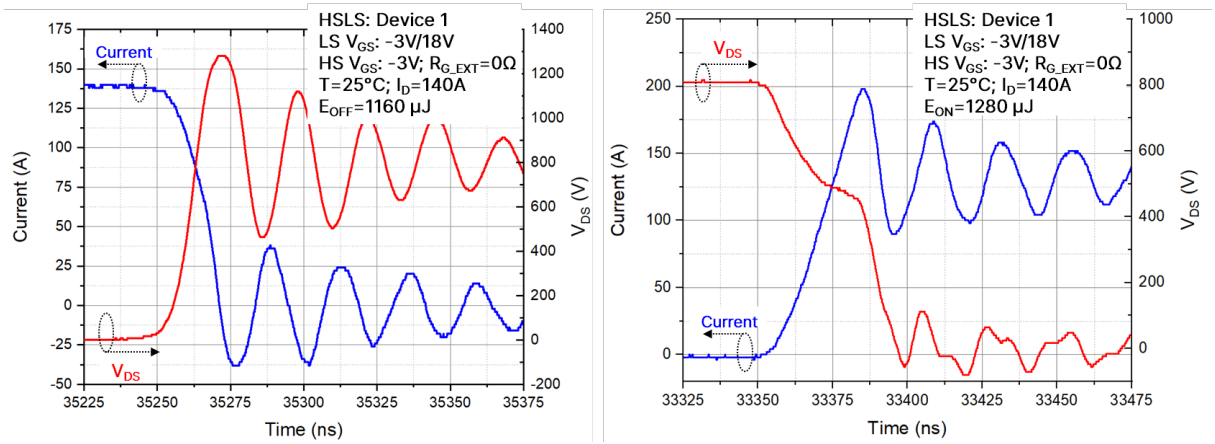

Fig.2. Measured device #1 switching characteristics in high current I_D=140A a) Turn-off; b) Turn-on.

Capacitance-Voltage (C-V) Characteristics

As discussed, PTO occurs during HS BD turn-off and it is caused by the charging current of the reverse transfer capacitance C_{RSS} as it creates a voltage drop across the total gate resistance (R_{G_INT}+R_{G_EXT}) and the input capacitances C_{ISS} [1, 2]. If the V_{GS} induced by this C_{RSS} charging event exceeds device's VTH, then PTO is triggered in the HS MOSFET and creates additional BD "reverse recovery" current. PTO is therefore dependent on device capacitances like C_{RSS} and C_{ISS}, the total gate resistance (R_{G_INT}+R_{G_EXT}), the switching speed, VTH, and temperature. Fig.3a shows high voltage C-V characteristics of device #1 with good C_{ISS}/C_{RSS} ratios over a wide V_{DS} range. For comparing different devices, we present the area independent C_{ISS}/C_{RSS} ratio. Fig.3b displays measured C_{ISS}/C_{RSS} ratio of the devices #1 and three reference commercially available SiC MOSFETs. Device #1 shows significantly higher C_{ISS}/C_{RSS} ratio compared to the other devices for the whole V_{DS} range.

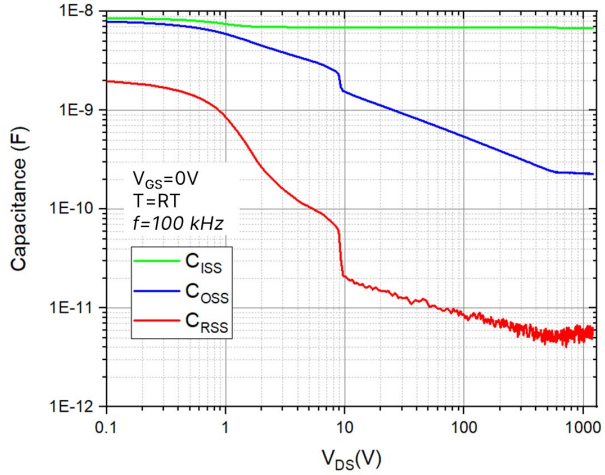

Fig. 3a. Measured C-V characteristics from device #1.

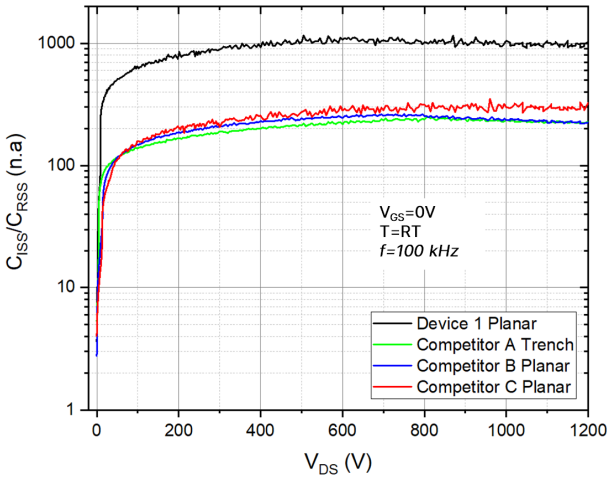

Fig. 3b. Measured C_{ISS}/C_{RSS} ratio of the devices considered in this work.

Other parameters that could affect device's PTO characteristics like devices R_{G_INT} and VTH as well as its RT R_{DSON} were also listed in Table #1.

Table 1. Summary of measured R_{G_INT} and VTH as well as R_{DSON} of device considered in this work

	Device #1	Competitor A Trench	Competitor B planar	Competitor C Planar
R_{G_INT} (Ω) (@1 MHz)	4.5	1.57	1.2	7.7
V_{TH}(V)	3	4.06	1.82	3.07
RT R_{DS_ON} (mΩ)	12	14	20	70

Parasitic Turn-On

To investigate PTO, LS switch conditions (e.g., V_{GS}, Temperature, R_{G_EXT}) were kept constant to maintain a fixed di/dt. HS V_{GS}=0V were applied and HS device were varied in HS R_{G_EXT} and in temperature (from RT to 175°C). V_{DD}=800V were applied in this study.

Fig. 4a shows measured switching turn-on characteristics using the device #1 at RT as the HS BD, with different HS R_{G_EXT}. No switching turn-on dependence on HS R_{G_EXT} is observed even with very high HS R_{G_EXT}. Same measurements with even higher R_{G_EXT} up to few hundreds Ω or device with even lower RT VTH, e.g., VTH=2.1V also show almost no sign of PTO (data not shown).

Fig. 4b-d) represent measured switching turn-on characteristics with different HS R_{G_EXT}, using competitor A (trench), competitor B (planar) and competitor C (planar) as the HS BD at RT, respectively. Different degrees of PTO can be observed when using these devices as the HS BD. We believe the excellent C_{ISS}/C_{RSS} ratio as shown in Fig. 3b is the critical factor for the high immunity to PTO that is observed for the device #1, and that this C_{ISS}/C_{RSS} ratio is more important to suppress PTO than the VTH level.

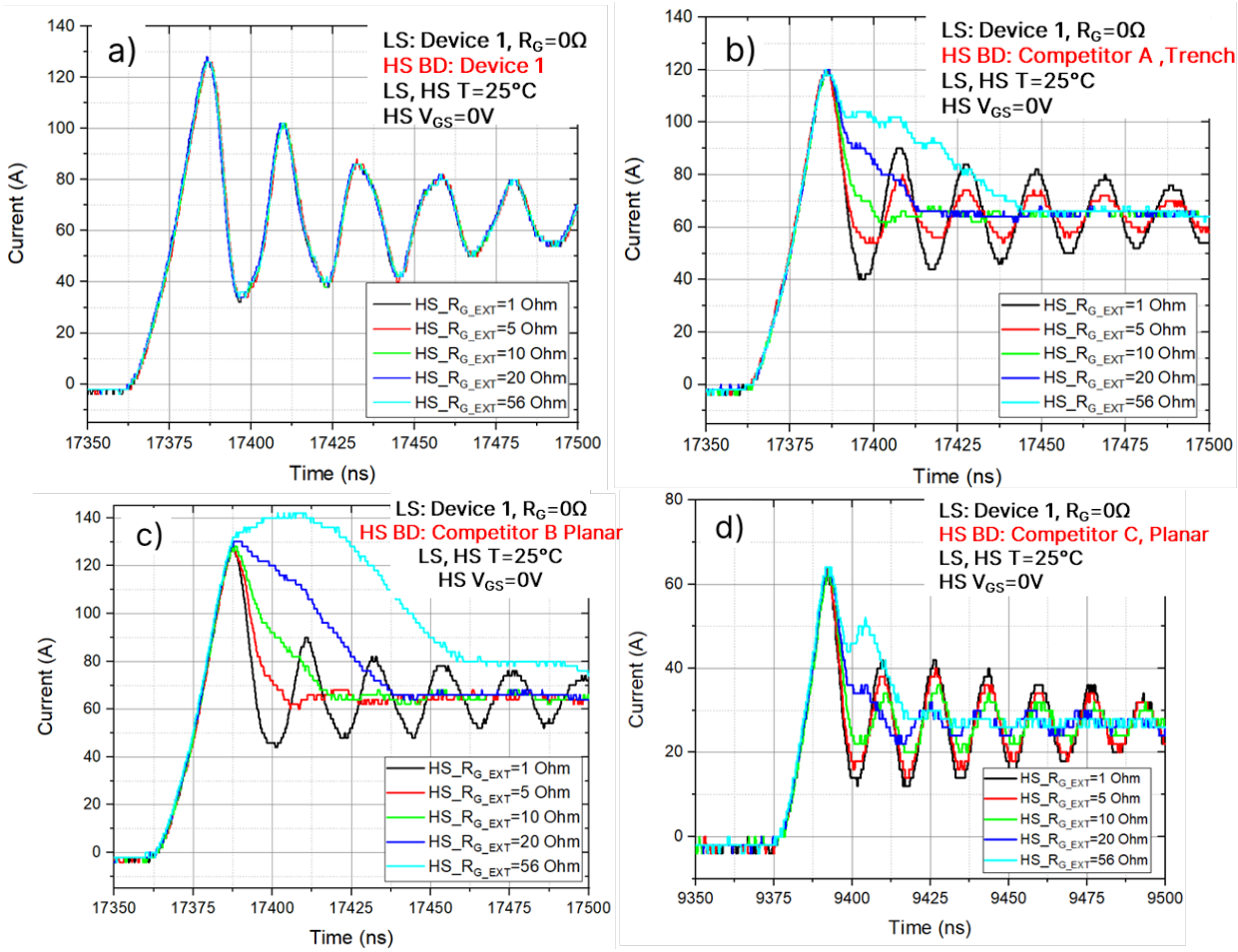

Fig. 4. Measured switching turn-on with HS R_{G_EXT} variation for PTO evaluation by using different devices as the BD: a) Device #1; b) Competitor A Trench; c) Competitor B Planar; d) Competitor C Planar.

High Temperature Parasitic Turn-On

Fig.5 displays measured turn-on characteristics vs. R_{G_EXT} using device #1 as the HS BD at 175°C, at different current densities. At T=175°C (with a lower VTH compared to RT) at different current densities with V_{DD}=800V and a turn-on di/dt=6A/ns, no sign of PTO can be observed, even with a high R_{G_EXT}=56Ω. These results further highlight the strong immunity of device #1 against PTO.

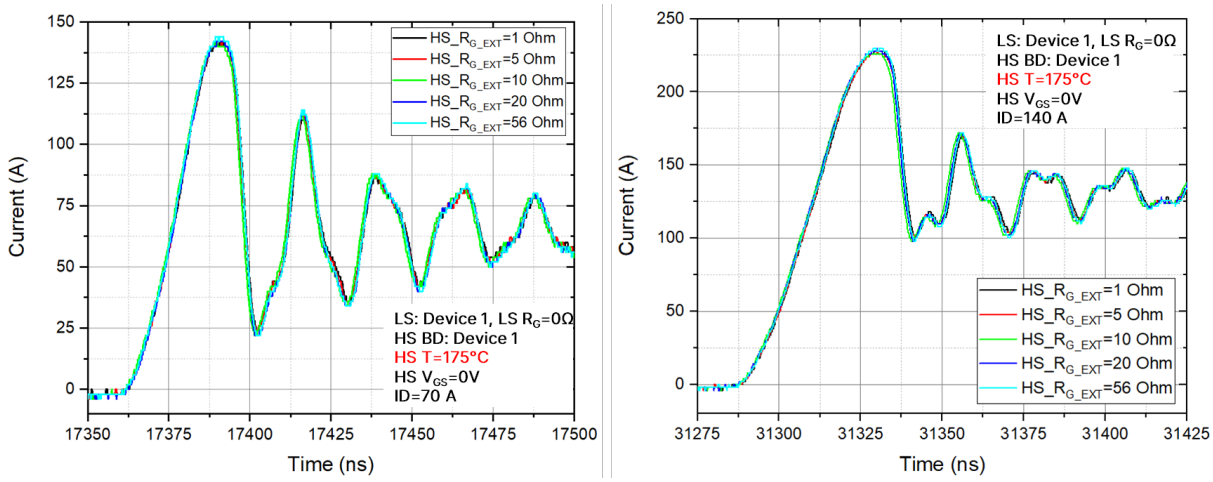

Fig. 5. Measured switching turn-on with HS R_{G_EXT} variation for PTO evaluation measured by using device 1 as the HS BD in T=175°C with different current densities.

Summary

In this work, we demonstrated a 1200V planar SiC MOSFETs with low R_{ON}, competitive R_{SP}, fast switching characteristics and a superior C_{ISS}/C_{RSS} ratio. Thanks to its superior C_{ISS}/C_{RSS} ratio, the device is highly robust against PTO even under fast switching, high V_{DD}, high temperature and high R_{G_EXT}.

References

[1] K. Sobe, T. Basler, and B. Klobucar, “Characterization of the parasitic turn-on behavior of discrete CoolSiC™ MOSFETs,” *in PCIM Europe*, pp. 1-7, 2019.

[2] S. Jahdi, O. Alatise, J. A. O. Gonzalez, R. Bonyadi, L. Ran, and P. Mawby, “Temperature and switching rate dependence of crosstalk in Si-IGBT and SiC power modules,” *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 849–863, Feb. 2016.

[3] A. Maerz, T. Bertelshofer, M. Bakran and M. Helsper, "A Novel Gate Drive Concept to Eliminate Parasitic Turn-on of SiC MOSFET in Low Inductance Power Modules," *in PCIM*, Nuremberg, Germany, 2017, pp. 1-7.

[4] T.-T Pham, J. Franchi, M. Domeij, “Body diode of 1.2kV SiC MOSFET: unipolar and bipolar operation”, in Materials Science Forum, Vol. 1091, pp 37-41 (2023).

[5] T. -T. Pham, J. Franchi, K. Lee and M. Domeij, "1.2 kV SiC MOSFET Body Diode Turn-Off in Fast Switching: Channel Conduction, Carrier Plasma and Parasitic Turn-On," *in 35th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Hong Kong, pp. 334-337 (2023).