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Analysis of Electrothermal Imbalance of Hard-Switched Parallel SiC MOSFETs Through Infrared Thermography

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Abstract. This paper provides an experimental investigation through infrared thermography of the steady-state temperature imbalance arising in parallel SiC MOSFETs. A switched-mode boost power converter based on two arrays of 4 parallel 1.2 kV MOSFETs is selected as a case-study. The analysis aims at proving that a proper device arrangement can minimize the thermal imbalance in the absence of circuit layout optimization.

Introduction

Parallel SiC MOSFETs are becoming a viable alternative to wide-area Si devices for switched-mode power converters requiring high current capacity [1, 2]. Nevertheless, both inherent devices mismatch and circuit layout asymmetry should be jointly considered during the design of the converter to achieve the full potential of SiC MOSFETs while limiting the electrothermal imbalance. Both active [3, 4] and passive [5, 6] current balancing techniques, as well as simulation methodologies for variability assessment [7] – [10] have been proposed in the literature. Recent scientific contributions stress the importance of a symmetrical layout for a uniform current distribution [11] and report how the common source parasitic inductances can be designed to compensate current imbalances [12]. In this paper, infrared thermography (IRT) is used to experimentally quantify the impact that device and circuit asymmetries can have on the steady-state temperature distribution of discrete parallel SiC MOSFETs. The objective is proving that the unbalancing effects caused by layout asymmetries and technological fluctuations can cancel out if the devices are optimally arranged.

Methodology

A half-bridge-based (HB) synchronous DC-DC boost converter consisting of 8 discrete SiC MOSFETs (4 parallel MOSFETs per switching side) was selected as a case-study. A schematic of the circuit is reported in Fig. 1 while a picture of the assembled printed circuit board (PCB) is provided in Fig. 2. The MOSFETs (not shown in Fig. 2) are placed along the opposite long edges of the PCB to minimize mutual thermal interaction between them.

It has been shown that a more balanced current distribution can be achieved by a symmetrical layout of the power traces [11], with the most critical being the trace intersecting the power-source terminals. Nevertheless, symmetrical power routing adds complexity to the design phase and might not be compatible with large-scale industrial applications [13]. In our design, two 71-mm long power tracks connect the HS drain and LS source terminals. Therefore, the increasing length of the trace connecting the common power ground to the individual source terminals introduces a mismatch among the various source stray inductances L_σ, with MOSFET LS1 (LS4) being the one seeing the highest (smallest) inductance to ground. Each device is controlled by its own gate-driver network;

however, two common control signals separately actuate the HS and LS gate drivers. The PCB was designed to be compatible with MOSFETs in both three- and four-leads TO-247 packages. The high-voltage capacitors (C_{DC1} and C_{DC2}) are mounted onto the PCB, whereas the load inductor L_{MP} and the load resistor R_{LOAD} are externally connected.

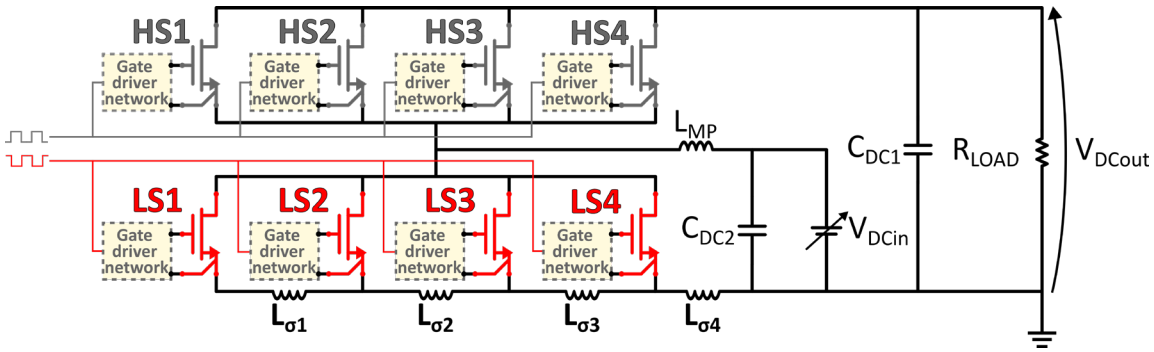
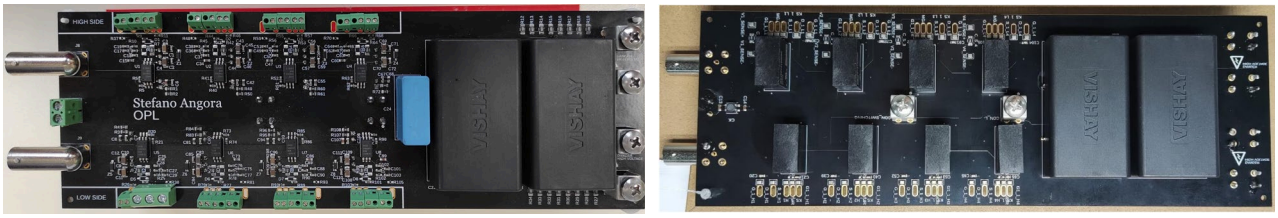


Fig. 1. Schematic of the half-bridge-based DC-DC converter in boost configuration emphasizing the high-side (HS) and low-side (LS) parallel MOSFETs, as well as the stray inductance (L_σ) along the ground path.



(a) (b)

Fig. 2. (a) Top and (b) bottom view of the assembled printed circuit board of the DC-DC converter.

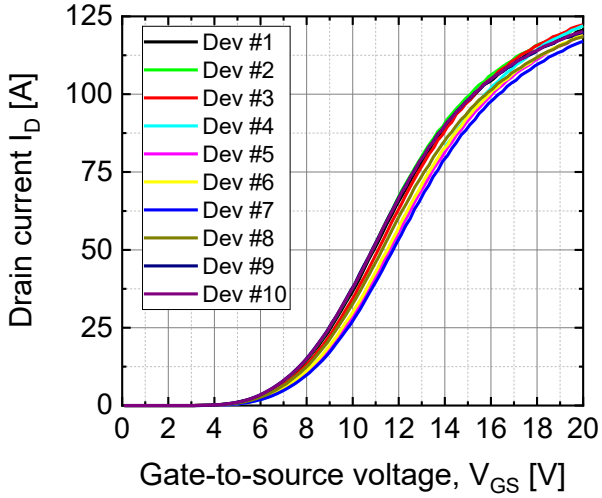


Fig. 3. Isothermal transfer characteristics at 25°C and V_{DS}=10 V of 10 samples of the commercial SiC MOSFET C3M0075120K.

Third-generation 1.2 kV-30 A SiC MOSFETs (C3M0075120K [14]) were chosen for this study. First, the isothermal transfer characteristics (I_D-V_{GS}) of 10 devices were measured at room temperature. These are reported in Fig. 3. Successively, the threshold voltage (V_{TH} [V]) and the current factor (K [A/V^2]) were extracted from the I_D-V_{GS} curves through the quadratic extrapolation method. The individual values of both parameters are reported in Table I. As witnessed by Fig. 4a-b, the statistical dispersion of both K and V_{TH} was found to be significantly lower than that of second-generation devices with similar ratings (1.2 kV-63 A, C2M0025120D [15]) [8]. A comparison of both

the expected value and the standard deviations for both classes of devices is given in Table II. Interestingly, both generations of devices showcase a very similar average value of V_{TH}, however, a three-times smaller normalized standard deviation is observed for the C3M0075120K. As for K, a similar reduction is found in terms of statistical dispersion.

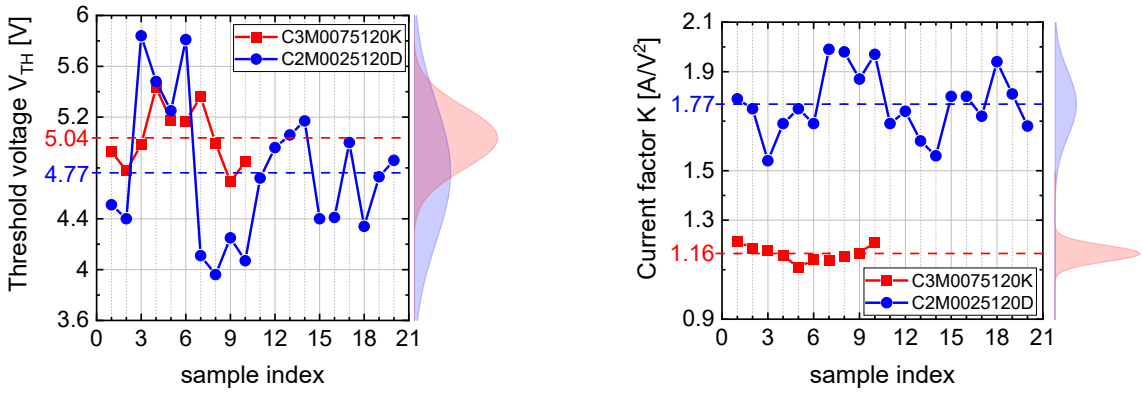


Fig. 4. Values and marginal fitting normal distributions of (a) the threshold voltage and (b) the current factor extracted from the I_D-V_{GS} curves of Fig. 3.

Results

This section reports the results of the electrothermal investigation. All the experiments summarized here were run on the DC-DC converter featuring only C3M0075120K devices.

The MOSFETs labelled as HS and LS in Table I were connected in parallel to the high side and the low side of the HB, respectively, and arranged as per the schematic of Fig. 1. The converter efficiency was preliminary characterized at different switching frequencies during synchronous boost operation to verify that the circuit meets the power performance expected from such a topology. The efficiency was found to be above 95% in a frequency range spanning from 25 kHz to 200 kHz, with a maximum of 98.2% at 50 kHz (Fig. 5).

Table I. Individual values of threshold voltage and current factor extracted from the transfer characteristics of Fig 3.

C3M0075120K	High Side				Low Side				Not connected	
Circuit position	HS1	HS2	HS3	HS4	LS1	LS2	LS3	LS4		
Sample index (dev#)	6	4	1	5	8	7	2	3	9	10
V_{TH} [V]	5.17	5.43	4.93	5.17	4.98	5.36	4.78	5.00	4.69	4.85
K [A/V^2]	1.42	1.16	1.21	1.11	1.18	1.14	1.19	1.15	1.17	1.21

Table II. Mean value and standard deviation of V_{TH} and K for samples of both C3M0075120K and C2M0025120D.

Part number	Threshold voltage V_{TH}		Current factor (K)	
	Mean value [V]	Relative standard deviation [%]	Mean value [A/V^2]	Relative standard deviation [%]
C3M0075120K	5.04	4.60	1.16	2.68
C2M0025120D	4.77	14.86	1.77	7.98

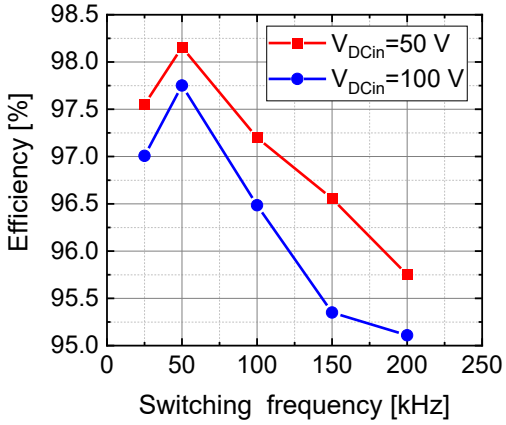
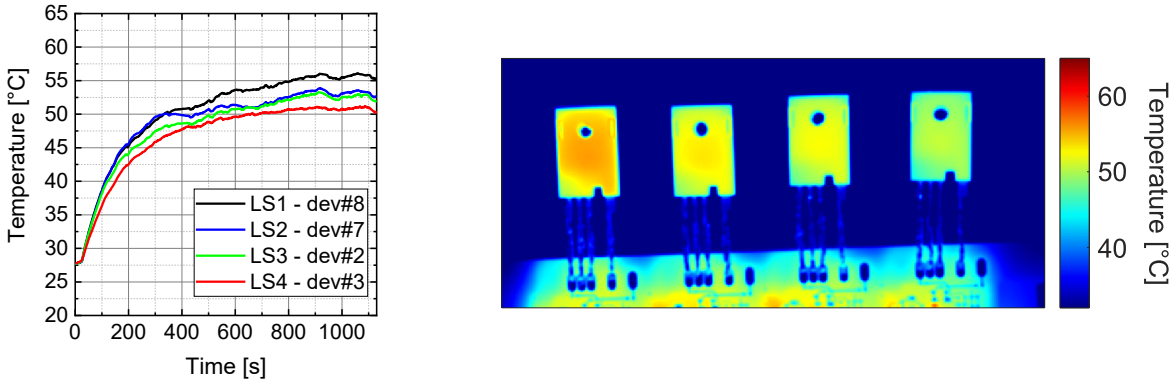
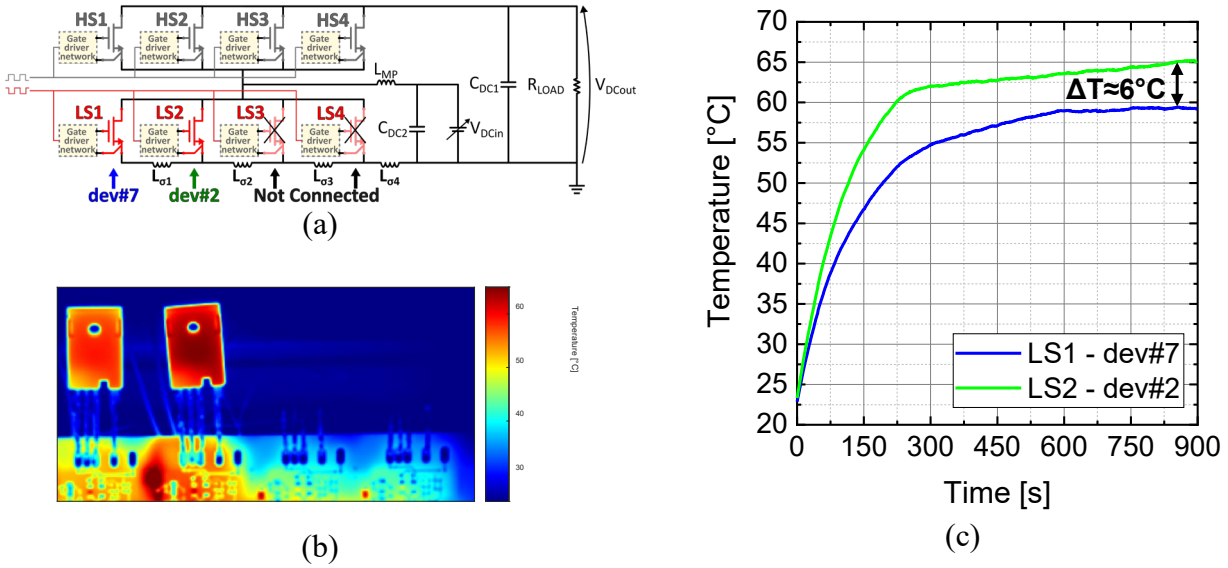


Fig. 5. Efficiency of the DC-DC converter measured during boost operation at different input voltages (V_{DCin}); the remaining test conditions are duty cycle 50 %, deadtime 120 ns, L_{MP}=1.8 mH and R_{LOAD}=90 Ω.



(a) (b)

Fig. 6. (a) Temperature evolution of the LS MOSFETs during 20 minutes of operation in boost mode at 100 kHz, V_{DCin}=75 V, V_{DCout}=150 V, L_{MP}=1.8 mH, R_{LOAD}=50 Ω, and (b) temperature map at 20 minutes.



(a) (b) (c)

Fig. 7. (a) Circuit configuration with dev#7 and dev#2 in positions LS1 and LS2, respectively; (b) temperature map at 15 minutes and (c) temperature evolution of the LS1 and LS2 MOSFETs during 15 minutes of operation in boost mode at 100 kHz, V_{DCin}=75 V, V_{DCout}=150 V, L_{MP}=1.8 mH, R_{LOAD}=50 Ω.

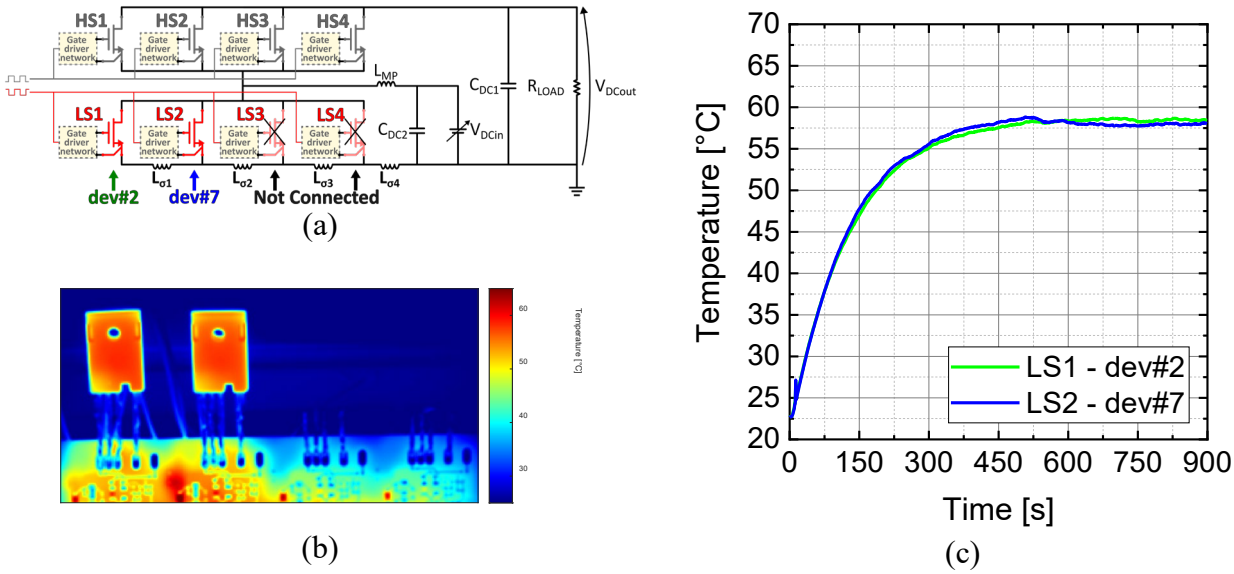


Fig. 8. (a) Circuit configuration with dev#2 and dev#7 in positions LS1 and LS2, respectively; (b) temperature map at 15 minutes and (c) temperature evolution of the LS1 and LS2 MOSFETs during 15 minutes of operation in boost mode at 100 kHz, V_{DCin}=75 V, V_{DCout}=150 V, L_{MP}=1.8 mH, R_{LOAD}=50 Ω.

The IRT investigation, performed through a FLIR SC7000 IR camera, only focused on the LS devices since only these switches experience hard switching at both turn on and turn off during boost operation. The graphs depicted in Figs 6a, 7c and 8c report the evolution over time of the temperature measured as the spatial average over the surface of the package. Since a heat sink would interfere with the IRT analysis, the converter input power was kept low enough to allow for safe operation even in the absence of external heat dissipation. Fig. 6a reports the temperature evolution of the 4 LS switches during 20 minutes of boost conversion at 100 kHz and shows that the temperature difference stays within 5 °C. The temperature map of Fig. 6b shows that the temperature decreases going from the MOSFET in position LS1 to the one in position LS4.

Successively, only the MOSFETs dev#7 and dev#2 (the samples exhibiting the widest V_{TH} difference among the LS devices) were left in the LS parallel array to exacerbate the electrothermal stress and clarify the interplay between the source stray inductance and the spread of the inherent device parameters. The converter was operated in two different configurations: the one of Fig. 7a, where dev#7 is placed in position LS1 and dev#2 in position LS2, and the one of Fig. 8a, where dev#2 is placed in position LS1 and dev#7 in position LS2.

In the first case (Fig. 7a), a steady-state temperature imbalance of 6°C is reached (Fig. 7b-c). This can be explained by the fact that the detrimental earlier turn-on switching due to the lower V_{TH} of dev#2 is further enhanced by the ease of commutation given by a lower source stray inductance.

On the other hand, the second configuration (Fig. 8a) provides both a very even temperature distribution and an overall lower maximum temperature (Fig. 8b-c), thus improving performance as well as long-term reliability. Remarkably, the maximum temperature reached in the second configuration (≈58 °C) is very close to that of the coldest MOSFET in the first configuration (i.e., dev#7 in position LS1), hence indicating a better converter efficiency.

Summary

In this paper, the steady-state temperature imbalance of parallel SiC MOSFETs has been experimentally investigated through infrared thermography. Third-generation 1.2-kV SiC MOSFETs have been selected for the analysis. Their static characteristics have been found to have a three-times smaller statistical dispersion than second-generation devices.

After the static characterization, the MOSFETs have been connected in parallel in a half-bridge configuration, which has been operated as a synchronous boost converter. The traces connecting the

individual power-source terminals of the LS MOSFETs to ground were designed to have different lengths so as to provide dissimilar stray inductances. This allowed for the analysis of the interaction between the fluctuation of the devices parameters and the circuit asymmetries. The experimental results have shown that, when optimally arranged, the MOSFETs discrepancies can be exploited to mitigate the temperature imbalance arising from layout asymmetries.

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