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Non-Linear Gate Stack Effect on the Short Circuit Performance of a 1.2-kV SiC MOSFET

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Abstract. In this paper, the effect of a non-linear dielectric gate stack on the short-circuit performance of a 1.2 kV SiC MOSFET was analyzed through TCAD simulations. Starting from the TCAD model of a commercial 1.2 kV, its standard gate oxide was replaced with a stack formed by oxide and a non-linear dielectric, characterized by a temperature dependent permittivity. This variation on temperature can be exploited to reduce the current conducted during short-circuit events, lowering the temperature reached through the device by about 30%, without affecting its static and dynamic performance.

Introduction

Silicon Carbide (SiC) power MOSFETs are gaining significant traction in the industry as a viable substitute for traditional silicon-based power MOSFETs. This shift is attributed to their superior performance characteristics, including enhanced breakdown voltage, faster switching speeds, and reduced on-resistance [1, 2]. These exceptional attributes position SiC power MOSFETs as strong contenders across various medium and high voltage applications, such as automotive, aerospace and photovoltaics [3, 4]. A well-engineered device must not only deliver optimal performance under standard operating conditions but also exhibit resilience in harsh operating scenarios. One crucial assessment to gauge the reliability of a SiC power MOSFET design is the short-circuit (SC) test [5, 6]. Current 1.2 kV SiC MOSFET are required to have a minimum short-circuit withstand time (SCWT) of 5 μs, that is hard to achieve due to the thermal properties of the material, since one of the main failure mechanisms during short-circuits event is thermal runaway. In this work, Technology Computer Aided Design (TCAD) simulations provide insights on the effect of a non-linear dielectric (NLD) gate stack, whose permittivity is temperature-dependent, in order to relieve the temperature increase during SC events. In particular, the standard gate oxide of a commercial 1.2 kV SiC MOSFET was replaced with a stack formed by oxide and a non-linear dielectric, as shown in Fig. 1, in order to counterbalance the current increase due to temperature during short-circuit events.

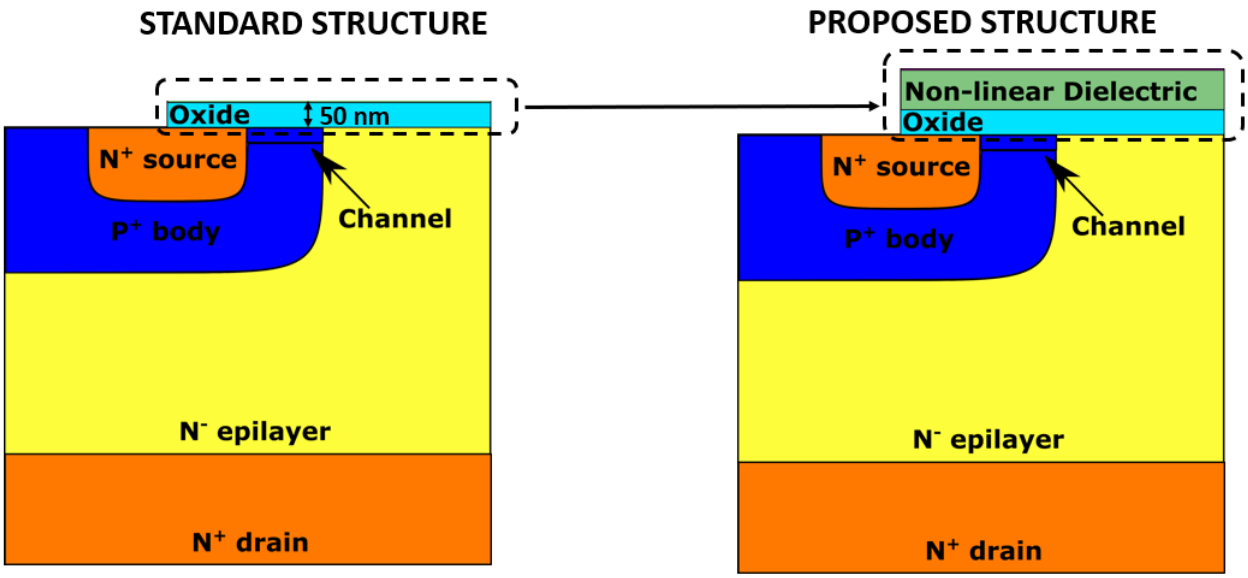


Fig. 1. Cross section of a standard power MOSFET compared with the proposed design, with an oxide/non-linear dielectric stack as gate insulator.

Non-Linear Dielectric Modeling

For non-linear dielectric we mean a dielectric with a temperature-dependent permittivity. This behavior is typical, for example, of ferroelectric materials. A ferroelectric material is characterized by a remanent polarization, whose direction can be modified by applying an external electric field and maintained even if the field is zero. When the temperature of the material overcomes a critical value, called Curie temperature (T_C), the material loses its ferroelectric properties, and the material goes to a paraelectric state, in which there is no remanent polarization when the applied electric field is zero. More in detail, the behavior of a ferroelectric material is governed by Landau's theory for the dependance of the polarization on the electric field and temperature, and by Curie-Weiss law for the dependence of the permittivity on temperature [7], which is the phenomenon we are interested in. The latter reads as follows:

$$\varepsilon = \lambda \frac{C_{CW}}{T - T_C} \quad with \begin{cases} \lambda = -1/2 & for\ T < T_C \\ \lambda = 1 & for\ T > T_C \end{cases}, \tag{1}$$

where T is the temperature of the material, T_C is the Curie temperature, that is the demarcation temperature between the ferroelectric phase (for $T<T_C$) and the paraelectric phase ($T>T_C$), and C_{CW} is the material dependent Curie-Weiss constant, which can be different in the ferroelectric phase and paraelectric phase. A suitable material for this kind of application is hafnium oxide (HfO_2), which is CMOS-compatible and can be made ferroelectric by doping. HfO_2 is particularly interesting because its T_C can be tuned by the dopant species, doping concentration, and grain size [8]. Currently, ferroelectric HfO_2 is widely used for nonvolatile direct access memories and negative capacitance field-effect transistors, where HfO_2 is properly doped to achieve a very high T_C to ensure operation in the ferroelectric phase and take advantage of the hysteretic beahviour of polarization [9].

For our application, we aim to have a T_C around the operating temperature of the device to benefit from the decreasing permittivity with temperature. Unfortunately, due to the novelty of the concept we are proposing, there is a lack of data in the literature for T_C in our range of interest. A desirable permittivity profile for our application is that of vinylidene fluoride trifluoroethylene P(VDF-TrFE) [10, 11], as reported in Fig. 2. This material is characterized by a T_C of 355 K and a C_{CW} of 3429 K for the ferroelectric phase and 11878 K for the paraelectric phase. However, P(VDF-TrFE) is a polymer compound and cannot withstand the temperatures reached during a typical SC event.

Since this work aims to investigate the effect of the temperature-dependent permittivity itself, the NLD was modelled with the same properties as an oxide but with the permittivity of P(VDF-TrFE). This approach allows us to focus on the impact of temperature-dependent permittivity rather than the specific material.

The capacitance of the NLD/oxide stack, fixing the thickness of the layers, was evaluated with an ac simulation, and it is reported in Fig. 3. As the capacitance is directly proportional to the permittivity, it increases as the temperature increases in the ferroelectric phase and starts to decrease in the paraelectric phase, according to the permittivity behaviour of Fig. 2.

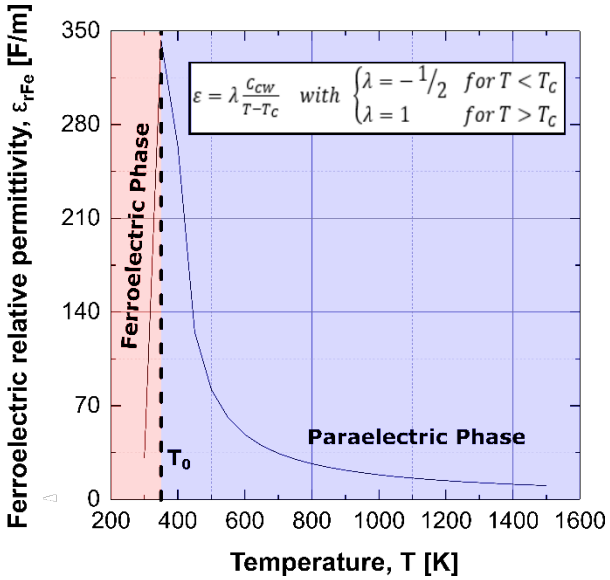


Fig. 2. Relative dielectric permittivity of the ferroelectric material P(VDF–TrFE), used to model the non-linear dielectric. Inset of the figure: general analytical model of the relative dielectric permittivity of a ferroelectric material.

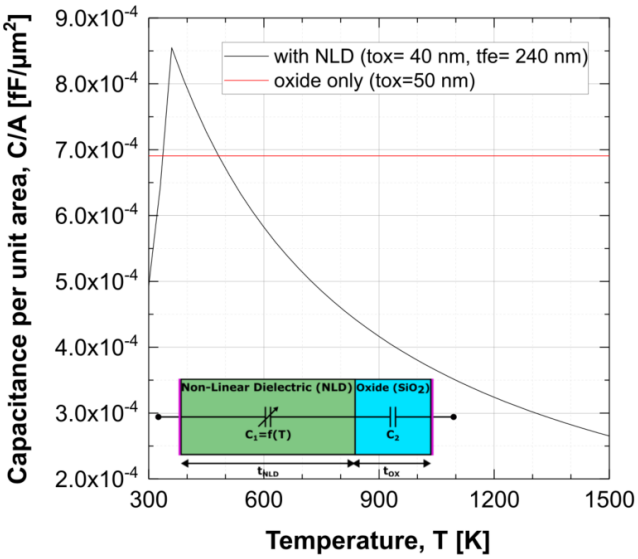


Fig. 3. Resulting capacitance of the oxide/NLD stack. The increase of temperature causes an increase of the capacitance exhibited by the stack if T is lower than T_C; after T_C, the capacitance decreases as the temperature increases.

Structure and Behaviour of the Device with Non-Linear Dielectric Gate Stack

For the simulations, the TCAD model of a commercial C2M0080120D manufactured by CREE, previously calibrated on experimental data [12-14], was used. First of all, the thickness of the materials composing the stack was chosen in order to match the static performance of the proposed device with a reference one, with a standard gate oxide of 50 nm, typical thickness for a 1.2 kV SiC MOSFET. In Figs. 4 and 5 the match of the transfer and output characteristics achieved for an oxide thickness (t_{OX}) of 40 nm and a NLD thickness (t_{NLD}) of 240 nm is reported, showing a good agreement both in terms of threshold voltage and saturation current. The comparison was conducted at a temperature of 340 K, typical operative temperature in automotive applications.

The switching behavior the proposed device was also simulated with a double pulse test and compared with the standard one. The resulting waveforms are reported in Fig. 6a. A focus on the turn-off and turn-on is also reported in Figs. 6b and 6c, showing a good agreement also of the dynamic behaviour, as confirmed by the value of the turn-off and turn-on energies (E_{OFF} and E_{ON}), reported in Table 1.

Table 1. Comparison turn-off and turn-on energies for proposed and standard structures.

	E_{OFF} [µJ]	E_{ON} [µJ]
With NLD	68.5	595
Oxide only	72.8	607

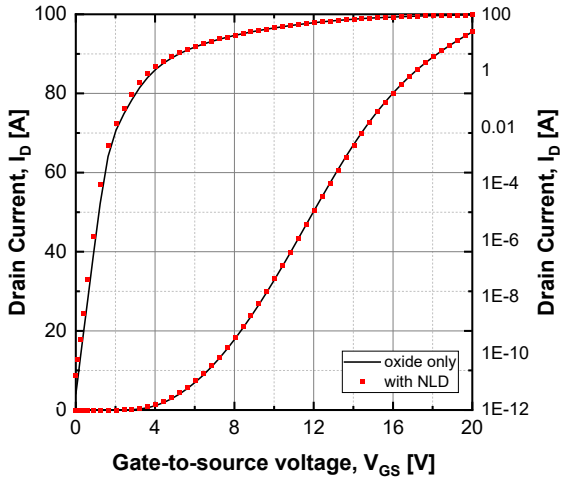


Fig. 4. Comparison between isothermal transfer characteristics of the reference MOSFET (with a 50 nm-thick oxide as gate insulator) and the proposed design (with the oxide/NLD stack, t_{ox}=40 nm and t_{NLD}=240 nm) at T=340 K (V_{DS}=20 V).

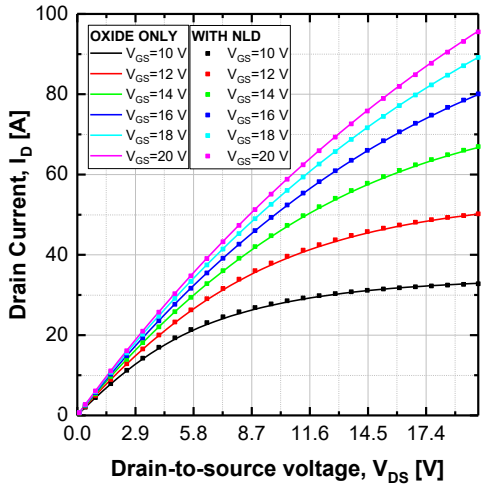
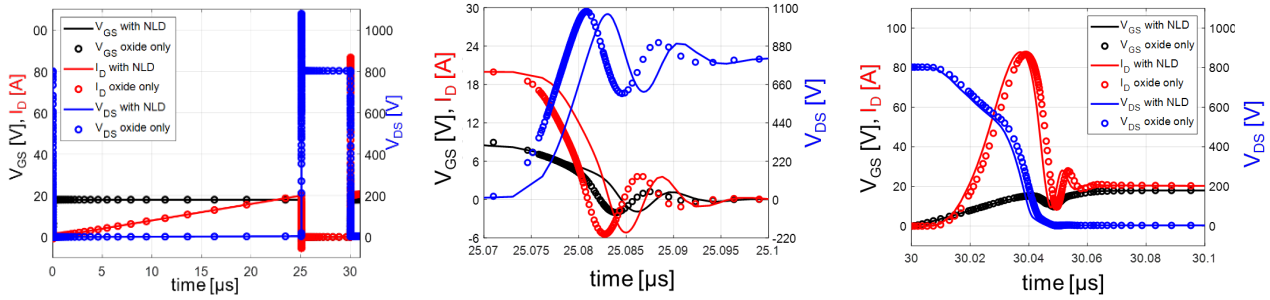


Fig. 5. Comparison between isothermal output characteristics of the standard MOSFET (with a 50 nm thick oxide as gate insulator) and the proposed design (with the oxide/NLD stack, t_{OX}=40 nm and t_{NLD}=240 nm) at T=340 K.

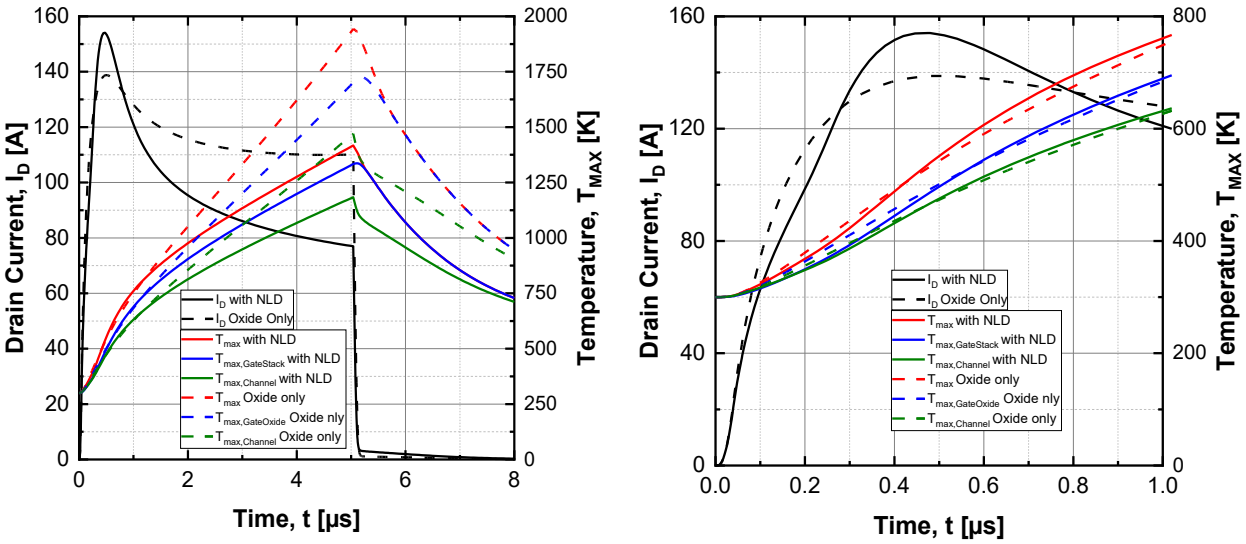


(a) (b) (c)

Fig. 6. Comparison between isothermal dynamic characteristics of the standard MOSFET (with a 50 nm thick oxide as gate insulator) and the proposed design (with the oxide/NLD stack, t_{OX}=40 nm and t_{NLD}=240 nm) at T=340 K. (a) whole double pulse test; (b) focus on turn-off; (c) focus on turn-on.

Short-circuit capability

The improved device was simulated and compared with the standard one during short-circuit conditions using electrothermal mixed-mode simulations [15, 16]. The test was conducted with a V_{GS} of 18 V and a supply voltage of 800 V, with an on-state time (T_{ON}) of 5 µs. As shown in Fig. 7a, the proposed structure shows better SC performance, since its maximum temperature is 30% lower than the reference structure (1410 K instead of 1940 K). This behaviour can be justified analyzing the temperature dependence of the permittivity. In Fig. 7b, a focus of the first micro-second of the transient is reported. Up to 0.3 µs, the temperature is such that the capacitance of the standard structure is larger than the one of the proposed structure, so the former conduct a larger current. From 0.3 µs to 0.8 µs the capacitance of the structure with the oxide/NLD stack overcomes that of the only-oxide structure, so the current of the former exceeds the latter, resulting in a larger current peak. Finally, beyond 0.8 µs, the capacitance of the proposed structure become lower again, causing its current to decrease more rapidly compared to the standard structure. As the threshold voltage shows no substantial difference between proposed and standard structure (see Fig. 8), the capacitance affects the current conducted through the term µCW/L.



(a) (b)

Fig. 7. Short-circuit waveforms for a supply voltage of 800 V applied for 5 µs. (a) whole short-circuit test; (b) focus on the first micro-second.

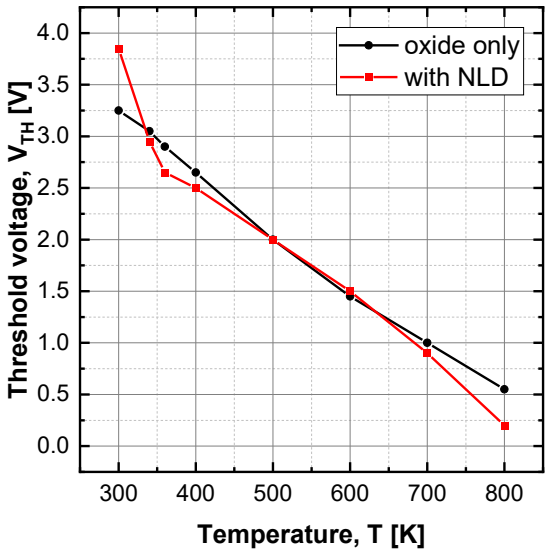


Fig. 8. Comparison between the threshold voltage of the standard and proposed structure, varying the temperature. The threshold voltage is evaluated as the voltage at which the electron concentration in the channel reaches the dopant concentration for V_{DS}=0 V.

Summary

In this paper, the effect of a non-linear dielectric gate stack on a 1.2 kV SiC MOSFET is analyzed using TCAD simulations. Starting from a TCAD model of a commercial 1.2 kV SiC MOSFET, the standard gate oxide was replaced by a stack formed by oxide and a non-linear dielectric, whose permittivity varies with temperature. The thicknesses of the layer forming the stack were chosen in order to match the static and dynamic characteristics of the standard device. Simulations shows that, although the standard operation of the device is unchanged, during short-circuit events the oxide/NLD stack device reached a maximum temperature 30% lower than the standard structure, suggesting an improved SC capability.

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