

A Geometry-Scalable Physically-Based SPICE Compact Model for SiC MPS Diodes Including the Snapback Mechanism

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Abstract. In this paper, a simple compact model for the static behavior of SiC MPS diodes is developed in the form of a SPICE-compatible subcircuit. The model is suited to describe the undesired snapback mechanism likely to occur in unoptimized high-voltage MPS structures with narrow width of the PiN portion and/or very thick drift layer; in particular, the model accounts for the snapback mechanism both as the cell extension varies and as individual portions of Schottky and PiN vary. Sentaurus TCAD simulations of a 10-kV MPS diode are used as a reference for the calibration of the model parameters and accuracy verification.

1 Introduction

Silicon Carbide (SiC) belongs to the class of semiconductors with a wide bandgap, that is, with a wider forbidden energy band than silicon (Si). Therefore, SiC is particularly suitable for fabricating devices for power applications. The wide bandgap of SiC results in higher breakdown voltages and lower susceptibility to intrinsic conduction effects. Conversely, because of the larger forbidden bandgap, standard SiC PiN rectifiers suffer from a more pronounced voltage drop than the Si counterparts due to the higher built-in potential (~2.8 V). Consequently, Merged-PiN-Schottky (MPS) diodes are usually adopted to overcome this issue [1]–[6]. The MPS structure offers low conduction losses and Schottky-like switching performance, but at the same time, low leakage currents in the off-state similar to PiN diode. However, the geometric dimensions of MPS diodes must be properly chosen to prevent the snapback mechanism [7]–[9]. The snapback consists in the presence of a negative-differential-resistance (NDR) branch in the I_A - V_{AK} characteristics (A =anode, K =cathode), which hinders the safe parallelization of multiple devices. Parallel-connected devices are particularly adopted in SiC technology to increase the current rating of the final module [10] without compromising the yield of the technological process. Nonetheless, the current might not be equally distributed among the individual chips and compact device models can help the early assessment of such imbalances in the circuit design phase [11]–[13].

This work presents a compact model for the static behavior of SiC MPS diodes that can be easily adopted in any SPICE-like simulator. The model accurately describes the behavior of a SiC MPS diode as a function of the width of the cell (W_{Cell}) and of the PiN portion (W_{PiN}/W_{Cell}), while also accounting for the detrimental snapback mechanism. The manuscript is arranged as follows: Section 2 gives a thorough description of the snapback mechanism, whereas Section 3 is mainly devoted to TCAD simulations of a single SiC MPS cell, used as a reference for the development and parameter optimization of the compact model. Equations and parameters used in the compact model are provided in Section 4. Conclusions are then drawn in Section 5.

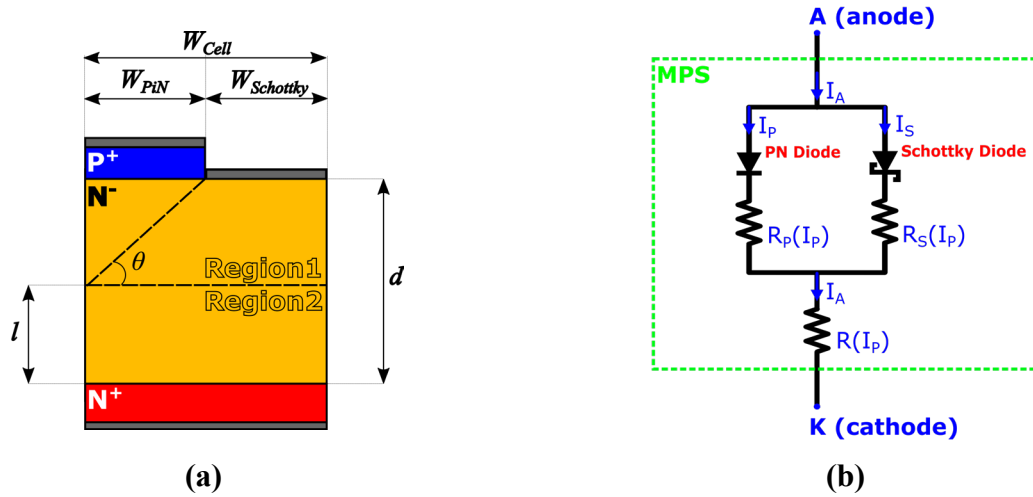


Fig. 1. (a) Sketch of the cross-section of the MPS rectifier; (b) SPICE-compatible subcircuit.

2 Snapback Mechanism

The snapback mechanism is associated to the presence of an NDR branch in the I_A - V_{AK} characteristic. In an MPS structure, two conditions are necessary for the occurrence of the snapback: (i) the ratio W_{PIN}/d is not sufficiently high (Fig. 1a) to ensure the full polarization of the P⁺N⁻ junction, and (ii) there is an increase in conductivity when the P⁺N⁻ junction injects minorities into the drift region (conductivity modulation). The first condition is explained with the help of Fig. 2, which compares the electrostatic potential distributions of a snapback-affected device and a snapback-free one (Fig. 2a-b). A low ratio W_{PIN}/d , like the one of the elementary cell in Fig. 2a, only allows a small part of the voltage applied to the ends of the device (V_{AK}) to actually bias the P⁺N⁻ junction. For this reason, a V_{AK} significantly greater than built-in potential (V_{BI}) must be applied to turn on the P⁺N⁻ junction. Such a mechanism can be further clarified through the lumped-parameters model of Fig. 1b. The model consists of two branches in parallel, the first composed of a Schottky diode and a series resistance R_s and the second by a P⁺N⁻ diode and a series resistance R_p . Both connect to a common resistance R .

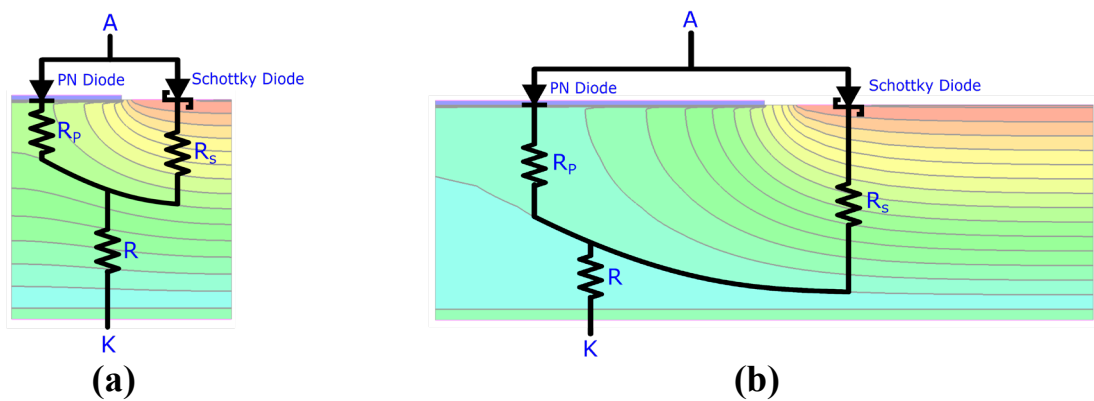


Fig. 2. Overlap between the simplified lumped element circuit and the potential distribution for (a) a snapback-affected and (b) snapback-free device.

When the Schottky diode begins to inject electrons, the current will flow into both R_s and R , thus producing two voltage drops with two opposite effects. While the voltage drop on R_s promotes the activation of the P⁺N⁻ diode, the voltage drop on R will have the effect of delaying the activation of the P⁺N⁻ diode. In a structure with a low W_{PIN}/d (Fig. 2a), the value of R is large enough to produce a voltage drop such as to delay the activation of the P⁺N⁻ junction. On the other hand, in a structure with a high value of W_{PIN}/d (Fig. 2b), the value of R is negligible with respect to that of R_s and most of V_{AK} is applied to the P⁺N⁻ junction (Fig. 2b). Once the P⁺N⁻ junction begins to inject holes into the

drift region, the concentration of minorities approaches and then exceeds that of the N^- doping. This increase in minorities within the drift region results in an increase in conductivity known as conductivity modulation; hence, the V_{AK} (initially due to the Schottky current only) reduces, thus increasing the effective portion of V_{AK} falling across the P^+N^- junction (positive feedback). As a result, a further increase in the MPS current I_A (which now includes the bipolar PiN current) is sustained by a reduction in V_{AK} , that is, a snapback point followed by an NDR branch is observed (Fig. 3).

A criterion allowing to distinguish between a snapback-affected (unoptimized) and a snapback-free (optimized) structure was developed in [7]. Specifically, a device where $W_{PiN}/d < 1/\tan \theta$ is unoptimized, whereas a device with $W_{PiN}/d > 1/\tan \theta$ is optimized, θ being the spreading angle of the Schottky unipolar current.

3 TCAD Simulations

The dc simulations of the individual 2-D MPS cell were conducted in the Sentaurus TCAD environment. Sentaurus simultaneously solves the Poisson and continuity (for electrons and holes) equations using a FEM-based approach. The structure of the 4H-SiC cell under test, inspired by the device explored in [7], presents an N^- drift layer and a P^+ region both grown by epitaxy. The drift doping $N^- = 7 \times 10^{14} \text{ cm}^{-3}$ and thickness $d = 95 \text{ }\mu\text{m}$ of the epitaxial drift layer were chosen to ensure a blocking capability of about 10 kV. The first simulation campaign was conducted by varying the width of the entire cell (W_{Cell}) in a range of 100 to 300 μm , keeping equal the widths of the Schottky and PiN regions, i.e. $W_{Schottky} = W_{PiN}$ (Fig. 3). Afterwards, a second simulation campaign was conducted by varying the W_{PiN}/W_{Cell} ratio and keeping the cell width fixed at 100 μm (Fig. 4). For all the simulations, the temperature was fixed at $T = 300 \text{ K}$. The Sentaurus mesh of the structure with $W_{Cell} = 100 \mu\text{m}$ and $W_{PiN} = W_{Cell}$, shown in Fig. 5a, includes ~ 3000 grid points and ~ 6000 elements (triangles). Simulations were performed by using the model libraries available for the 4H-SiC polytype and optimizing the Schottky barrier (to 1.09 eV) to get results in agreement with those obtained in [7]. The computation of a single characteristic with a small step size required a CPU time of about 5 mins on a workstation equipped by four e7-8880V4 2.2 GHz CPUs and 250 GB RAM. The output current (expressed in $\text{A}/\mu\text{m}^2$ since a 2-D cell was simulated) was multiplied by a factor equal to 10^6 to obtain the current that flows in an MPS with 1 cm^2 area. Additional Sentaurus simulations were also performed by alternately removing the PiN and Schottky portions. The results were used as a reference for the calibration process of the parameters of the SPICE compatible compact MPS model mentioned in Section 2 and discussed more specifically in Section 4.

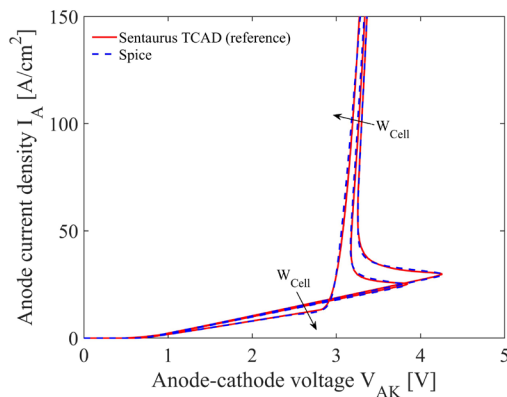


Fig. 3. TCAD (red) and SPICE (blue) I_A – V_{AK} characteristics by varying W_{cell} (100, 120 and 300 μm) for W_{PiN} equal to $W_{Schottky}$ and a constant device area.

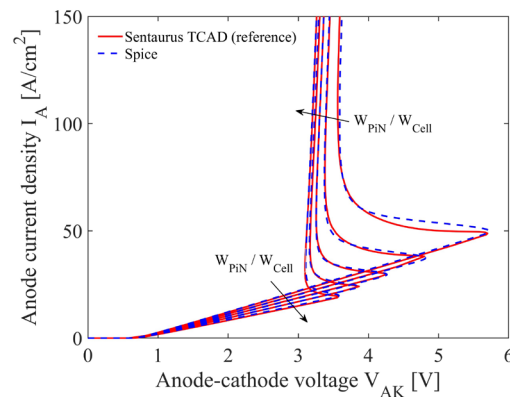


Fig. 4. TCAD (red) and SPICE (blue) I_A – V_{AK} characteristics by varying W_{PiN}/W_{Cell} ratio (0.2, 0.3, 0.4, 0.5, 0.6 and 0.7) for W_{Cell} equal to 100 μm and a constant device area.

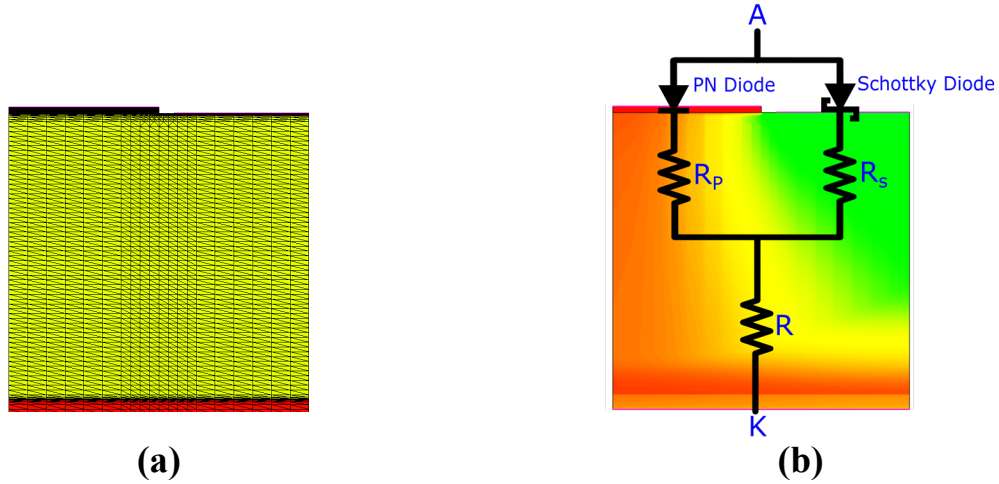


Fig. 5. (a) Setaurus TCAD mesh of the simulated MPS; (b) overlap between the simplified circuit model and the holes distribution at the conductivity modulation onset.

4 MPS Model and Fitting Functions

4.1 MPS Model

The MPS model was implemented in the form of a SPICE compatible subcircuit and is drawn in Fig. 1b. The model, as mentioned in Section 2, consists of two parallel branches placed in series with a current-dependent resistor R ; one branch includes the series of a P^+N^- diode and a current-dependent resistor R_P , while the other branch is composed by the series of a Schottky diode and a current-dependent resistor R_S : the I_P current dependence of R and R_P is ascribable to conductivity modulation. This is supported by the holes distribution reported in Fig. 5b (obtained from TCAD simulations) which shows that R and R_P lay in the holes-flooded region; therefore, when the I_P current increases, R and R_P decrease. Nevertheless, R_P tends to a limit value R_o ; the functional dependences of R and R_P on the PiN current can be expressed as follows:

$$R(I_P) = \frac{R_2^u}{1 + \alpha \cdot I_P} \quad (1)$$

$$R_P(I_P) = \frac{R_1^u}{1 + \alpha \cdot I_P} + R_o \quad (2)$$

where R_1^u and R_2^u are the resistance values under Schottky unipolar current condition ($I_P=0$) offered by Region1 and Region2, respectively (Fig. 1a), while R_o as well as α are geometry-dependent fitting functions. Conversely, the value of R_S grows with increasing I_P and this can be attributed to the shrinking of the region crossed by the unipolar Schottky current I_S ; this is witnessed by the hole density distributions of Fig. 5b. The relation between R_S and I_P was modeled according to the following equation:

$$R_S(I_P) = R_1^u + \gamma \cdot I_P \quad (3)$$

where γ is a fitting parameter shown in Table III.

The approach adopted to derive the expressions of R_1^u and R_2^u is based on the JBS (junction barrier Schottky) current distribution model [14]. In this approach, the 2-D current flow during the unipolar operation is assumed to be divided into two parts as shown in Fig. 1a: the current spreading region (Region1) and the uniform current-flow region (Region2). In particular, the current is assumed to linearly diffuse in Region1 with a spreading angle θ . For a given doping N^- , θ is almost insensitive to the MPS geometry, and therefore, it is considered constant. Then, considering that the current flux distribution is uniform in Region2, it is possible to exploit the formula:

$$R_2^u = \rho \frac{l}{W_{\text{Cell}} \cdot H} = \rho \frac{d - \frac{W_{\text{Cell}}}{2} \cdot \tan \theta}{W_{\text{Cell}} \cdot H} \quad (4)$$

where H is the dimension orthogonal to the cross section (Fig. 1a) shown in Table I, while ρ is the resistivity value obtained from TCAD simulations under unipolar current condition ($I_p=0$), which is reported in Table I. Then, through the TCAD I_A - V_{AK} characteristics under unipolar conduction condition ($I_p=0$), it was possible to determine for each W_{Cell} the value of the sum $R_1^u + R_2^u$, that was described with a second-order polynomial function as W_{cell} varies, the coefficients of which are reported in Table II:

$$R_{\text{TOT}}^u(W_{\text{Cell}}) = R_1^u + R_2^u = W_{\text{Cell}}^2 \cdot p_1 + W_{\text{Cell}} \cdot p_2 + p_3. \quad (5)$$

Eventually, R_1^u is easily deduced from (4) and (5). Fig. 3 shows the comparison between the I_A - V_{AK} characteristics of the SPICE model and those obtained from TCAD simulations by varying W_{Cell} , keeping the same widths of the Schottky and PiN portions. Subsequently, the model accuracy was verified for $W_{\text{PiN}} \neq W_{\text{Schottky}}$; Fig. 4 shows TCAD and SPICE I_A - V_{AK} characteristics by varying the $W_{\text{PiN}}/W_{\text{Cell}}$ ratio. Also in this case, the value of R_{TOT}^u was extracted from the TCAD I_A - V_{AK} characteristics under unipolar-conduction condition ($I_p=0$). The relation of R_{TOT}^u by varying $W_{\text{PiN}}/W_{\text{Cell}}$ was represented with the hyperbolic-type function shown below:

$$R_{\text{TOT}}^u \left(\frac{W_{\text{PiN}}}{W_{\text{Cell}}} \right) = \frac{a_1}{1 - \frac{W_{\text{PiN}}}{W_{\text{Cell}}}} + a_2 \cdot \frac{W_{\text{PiN}}}{W_{\text{Cell}}} + a_3 \quad (6)$$

the coefficients of which are listed in Table II.

Similarly to (4), the resistance offered by Region2 (R_2^u) can be calculated through the JBS distribution model:

$$R_2^u = \rho \frac{l}{W_{\text{Cell}} \cdot H} = \rho \frac{(d - W_{\text{PiN}} \cdot \tan \theta)}{W_{\text{Cell}} \cdot H} \quad (7)$$

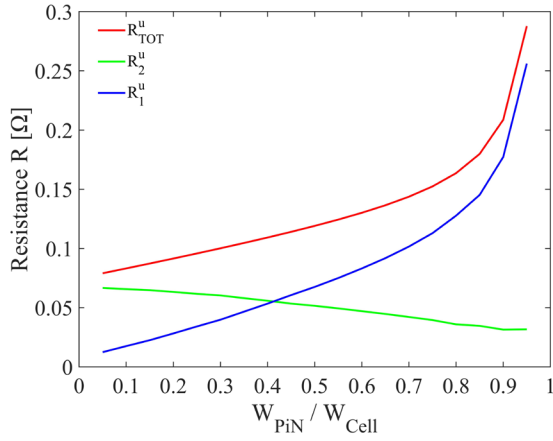
The resistances R_1^u , R_2^u and R_{tot}^u for different values of the $W_{\text{PiN}}/W_{\text{Cell}}$ ratio are shown in Fig. 7, while Fig. 8 shows the snapback-voltage (V_{sb}) as a function of the $W_{\text{PiN}}/W_{\text{Cell}}$ ratio. When the PiN portion increases, R_2^u decreases and electrical behavior of MPS diode tends to that of PiN diode and the snapback tends to disappear as V_{sb} approaches the built-in potential (V_{BI}) of P^+N^- junction.

Table I. Physical and geometrical parameters of the MPS diode designed with Sentaurus TCAD.

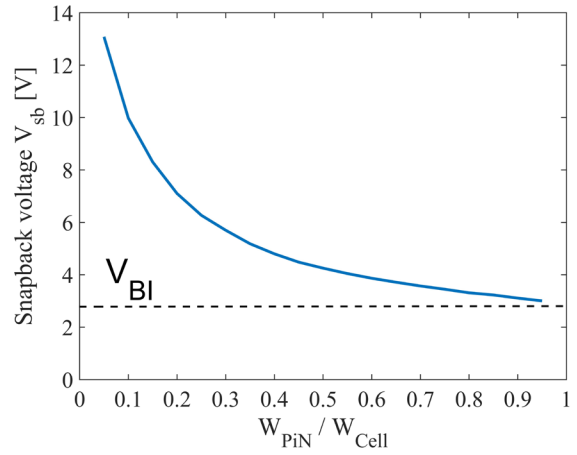
N^-	$7 \times 10^{14} [\text{cm}^{-3}]$
P^+	$10^{19} [\text{cm}^{-3}]$
N^+	$10^{19} [\text{cm}^{-3}]$
W_0	$100 [\mu\text{m}]$
H	$1 [\mu\text{m}]$
d	$95 [\mu\text{m}]$
θ	42°
ρ	$9.65 [\Omega \times \text{cm}]$

Table II. Coefficients of the polynomial functions reported in (5) and (6).

p_1	$-5.475 \times 10^{13} [\Omega/\text{cm}^2]$
p_2	$402.4 \times 10^4 [\Omega/\text{cm}]$
p_3	$8.42155 \times 10^2 [\Omega]$
a_1	$7.548 \times 10^3 [\Omega]$
a_2	$7.302 \times 10^2 [\Omega]$
a_3	$6.743 \times 10^2 [\Omega]$

**Fig. 7.** Trends of the individual resistance by varying the $W_{\text{PiN}}/W_{\text{Cell}}$ ratio.**Table III.** Optimized values of the model parameters.

α_0	$0.475 [\text{A}^{-1}]$
k	$2.5 [\text{A}^{-1}]$
η	$1.06 \times 10^{-3} [\Omega]$
μ	$2.88 \times 10^5 [\Omega^2/\text{cm}^2]$
γ	$1.15 \times 10^{-3} [\Omega/\text{A}]$

**Fig. 8.** Snapback-voltage V_{sb} by varying the $W_{\text{PiN}}/W_{\text{Cell}}$ ratio.

4.2 Fitting Functions

The fitting functions α and R_o were identified by comparing the Sentaurus I_A - V_{AK} characteristics of the MPS diode with those of SPICE under bipolar-current condition ($I_p > 0$).

The parameter α can be described as the rate of conductivity modulation and its dependence on the geometry can be explained as follows: a wider W_{PiN} causes a better polarization of the P^+N^- junction and thus, a higher injection rate of the holes into the drift region. As described by (8), α was modeled as a linear function of both $x = W_{\text{PiN}}/W_{\text{Cell}}$ and W_{Cell} , where α_0 is a fitting parameter shown in Table III and W_0 is a reference width reported in Table I.

$$\alpha(W_{\text{Cell}}, x) = \alpha_0 + \frac{W_{\text{Cell}} - W_0}{W_0} + k \cdot (x - 0.5). \quad (8)$$

Finally, the parameter R_o represents the lower bound of the conductivity-modulated resistance. Differently from α , it only depends on the total cell extension (W_{Cell}) and not on the ratio $W_{\text{PiN}}/W_{\text{Cell}}$ and its variation was modeled as follows:

$$R_o = \eta + \sqrt{\mu \cdot (W_{\text{Cell}} - W_0)} \quad (9)$$

where η and μ are fitting parameters shown in Table III.

5 Conclusions

In this paper, a compact model for the static simulation of SiC MPS diodes has been proposed and implemented in the form of a simple SPICE-compatible subcircuit. The model is designed to describe the detrimental snapback mechanism as a function of both the total extension of the elementary cell and of the ratio of the PiN and Schottky areas. This SPICE-compatible model can be particularly useful and convenient in evaluating and preventing the impact of snapback to ensure safe parallelization of multiple devices. Moreover, thanks to this compact model, it is possible to estimate with good accuracy the effect of the snapback in conditions not feasible for TCAD analysis, such as converter-level simulations. Therefore, the presented model can be a valuable support for both the design and optimization of SiC MPS cells and for an estimation of the impact of snapback. Results of Sentaurus TCAD simulations of a 10 kV device have been used as a case-study and adopted as a reference to optimize the parameters of the model and for the final accuracy verification. It has been found that the SPICE simulations are immune from convergence problems and last less than 1 s on a normal PC.

References

- [1] T.R. McNutt, A.R. Hefner Jr., H.A. Mantooth, J. Duliere, D. W. Berning, and R. Singh, "Silicon carbide PiN and merged PiN Schottky power diode models implemented in the Saber circuit simulator," *IEEE Trans. Power Electronics*, vol. 19, no. 3, pp. 573–581, May 2004.
- [2] V. d'Alessandro, A. Irace, G. Breglio, P. Spirito, A. Bricconi, R. Carta et al., "Influence of layout geometries on the behavior of 4H-SiC 600V Merged PiN Schottky (MPS) rectifiers," *Proc. IEEE International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, 2006, pp. 165–168.
- [3] S. Palanisamy, S. Fichtner, J. Lutz, T. Basler, and R. Rupp, "Various structures of 1200V SiC MPS diode models and their simulated surge current behavior in comparison to measurement," *Proc. IEEE International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, 2016, pp. 235–238.
- [4] Ł. Starzak, A. Stefanskyi, M. Zubert, and A. Napieralski, "Improvement of an electro-thermal model of SiC MPS diodes," *IET Power Electronics*, vol. 11, no. 4, pp. 660–667, 2018.
- [5] A. Wang, Y. Bai, Y. Tang, C. Li, Z. Han, J. Lu et al., "Analysis of transient surge current mechanism in SiC MPS diode with the transition region," *IEEE Trans. Electron Devices*, vol. 68, no. 12, pp. 6330–6337, Dec. 2021.
- [6] M. Boccarossa, A. Borghese, L. Maresca, M. Riccio, G. Breglio, and A. Irace, "TCAD analysis of the impact of the metal-semiconductor junction properties on the forward characteristics of MPS/JBS SiC diodes," *Proc. IEEE workshop on Wide bandgap Power Devices and Applications in Europe (WiPDA Europe)*, 2022.
- [7] H. Niwa, J. Suda, and T. Kimoto, "Ultrahigh-voltage SiC MPS diodes with hybrid unipolar/bipolar operation," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 874–881, Mar. 2017.
- [8] S. Fichtner, "Ruggedness of 1200V SiC Schottky and MPS diodes," PhD dissertation, Technical University of Chemnitz, 2018.
- [9] Y. Huang, "Simulation and modelling for SiC high-power diodes," PhD dissertation, Technical University of Munich, 2020.
- [10] A. Borghese, M. Riccio, A. Castellazzi, L. Maresca, G. Breglio, and A. Irace, "Statistical Electrothermal Simulation for Lifetime Prediction of Parallel SiC MOSFETs and Modules," in *Proc. IEEE International Conference on Industrial Electronics for Sustainable Energy Systems (IESES)*, Cagliari, Italy: IEEE, Sep. 2020, pp. 383–386.

- [11] A. Borghese et al., “An Experimentally Verified 3.3 kV SiC MOSFET Model Suitable for High-Current Modules Design,” in Proc. IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD), Shanghai, China, May 2019, pp. 215–218.
- [12] A. Borghese, M. Riccio, L. Maresca, G. Breglio, S. Kicin, and A. Irace, “A Scalable SPICE-Based Compact Model for 1.7 kV SiC MOSFETs,” MSF, vol. 1062, pp. 658–662, May 2022.
- [13] A. Borghese, M. Riccio, L. Maresca, G. Breglio, and A. Irace, “A Scalable SPICE Electrothermal Compact Model for SiC MOSFETs: A Comparative Study between the LEVEL-3 and the BSIM,” KEM, vol. 946, pp. 135–140, May 2023.
- [14] L. Zhu and T. P. Chow, “Analytical Modeling of High-Voltage 4H-SiC Junction Barrier Schottky (JBS) Rectifiers,” IEEE Trans. Electron Devices, vol. 55, no. 8, pp. 1857–1863, Aug. 2008.