Solid State Phenomena
ISSN: 1662-9779, Vol. 360, pp 75-80
doi:10.4028/p-lhRi4M

Submitted: 2023-09-30
Revised: 2024-05-30
Accepted: 2024-06-10
Online: 2024-08-23

SiC GAA MOSFET Concept for High Power Electronics Performance Evaluation Through Advanced TCAD Simulations

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Keywords: TCAD, SiC, Power Electronics, SiC-MOSFET, Gate All Around.

Abstract. In this work a groundbreaking SiC power MOSFET based on innovative vertical Gate All Around (GAA) concept is presented. Extensive TCAD simulations are performed to analyze the performance in forward as well as in reverse conditions for this new device concept. The proposed design has a target rating voltage of 1200V, suitable for e-mobility applications.

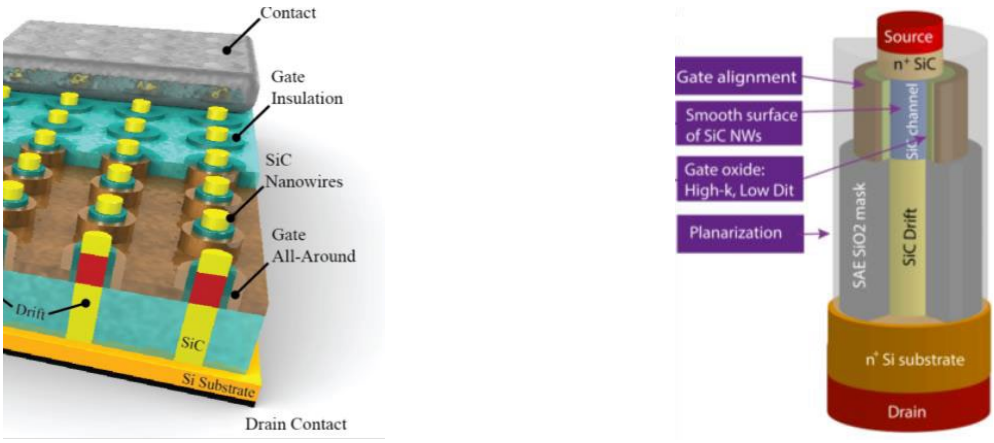
Introduction

The next generation of power electronic devices should offer high energy efficiency with high power conversion density. Silicon Carbide (SiC) is the most promising semiconductor for power electronics due to its high critical electric field, high switching frequency and high temperature operation capability. The remarkable performance of SiC, in contrast to silicon (Si), serves as the driving force behind the relentless pursuit of enhancing SiC device quality. SiC boasts a wide bandgap, high electron mobility, and exceptional thermal conductivity [1]. Many technological challenges are open to fully exploit the material properties. From the device design point of view, different approaches are present in literature to implement a high voltage SiC MOSFET device. Two main approaches are adopted to design the active section of the device: *i)* planar Gate and *ii)* trench Gate designs. The bulk section of the device is typically implemented by *i)* a constant doping profile Drift-layer or *ii)* a Super-junction and semi super-junction approaches. All the device concepts proposed in literature need a termination region, that in high voltage device takes a relevant portion of the device area. Therefore, the termination region, that defines the breakdown voltage (BV) of the device, strongly contributes to the cost of the device.

In this work a new SiC MOSFET design, without a termination region, is proposed and analyzed through TCAD simulations. The design concept is based on SiC pillars, grown on a Si substrate, surrounded by silicon dioxide. In the GAA SiC MOSFET design the Gate contact surrounds a portion of the pillar. The proposed design does not need a termination region since the electric field peak arises in the oxide. In a first section, the design geometrical features are illustrated, together with adopted TCAD model. In the second section TCAD simulations results are reported and commented.

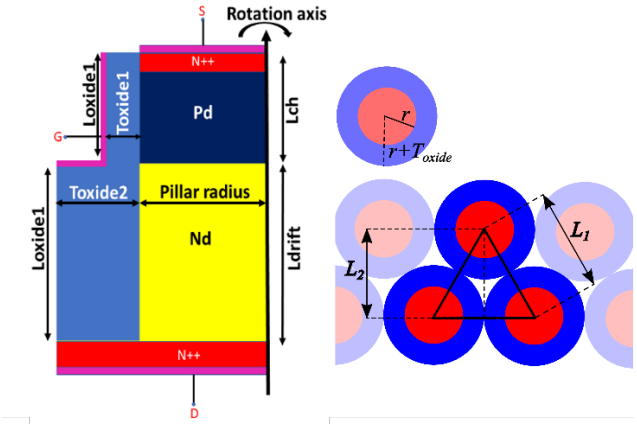
The Proposed Device

A sketch of the proposed device is reported in Fig. 1. The overall device is composed by many N-type SiC cylindrical pillars surrounded by silicon dioxide (the single cell), in cellular parallel mode connection. The pillars are grown starting from a n+ Si substrate, connecting all pillars to the same Drain region. The top P-Body layer is surrounded by the Gate oxide layer, connected to the Gate contact. The Gate oxide layer may be implanted by High-k oxide. However, in this work the Gate oxide in made by Silicon Dioxide to evaluate the performances of the device with standard materials.



a) b)

Fig. 1. a) A sketch of the overall SiC GAA MOSFET design concept. b) A detail of the single pillar structure.



a) b)

Fig. 2. A sketch of the TCAD structure. a) A vertical section of a single pillar and b) the spatial distribution assumed among the pillars within this work.

Table I. Design parameters	
Toxide1	**50 nm**
Loxide1	**0.7 µm**
Toxide2	**0.2 µm**
Lch	**0.5 µm**
Ldrift	**6 µm**
Nd	**$1.1*10^{16}$ cm^{-3}**
Pd	**$4*10^{17}$ cm^{-3}**

The device TCAD model is assumed to be rotationally symmetric around vertical right edge in Fig. 2. To the active area of the device contributes both the pillar and the surrounded oxide. Therefore, in this work the ratio among the pillar area and oxide area will be calculated from the geometry reported in Fig. 2b, where $L_1 = 2(r + T_{OXIDE})$ and $T_{OXIDE} = Toxide1$. Further design details are reported in Table I. The geometry of the single pillar (See Fig. 1b) allows a suitable TCAD simulation by using cylindrical coordinates, therefore a 2D mesh is considered to simulate a 3D cylindrical device. Standard physical models are adopted to run numerical simulations and only fixed charges are considered at the SiC/SiO_2 interface. When the radius of the proposed structure is lower than tens of nanometers, a very accurate description of the channel mobility is mandatory [2], therefore the MLDA model is used to model the channel electron density by quantum mechanical equations [3]. The length of the Drift region (L) is 7µm to allow a Breakdown Voltage (BV) of about 1300 V, *without the presence of a termination region*. The extensive numerical characterization of the proposed structure is presented in this work through the simulation of both the static forward (J_D-V_{GS} and J_D-V_{DS}) and reverse characteristics. Finally, all the numerical results reported in this work refer to a structure where the Source region is connected to the P-Body region through an ohmic contact, laying on the symmetry axes.

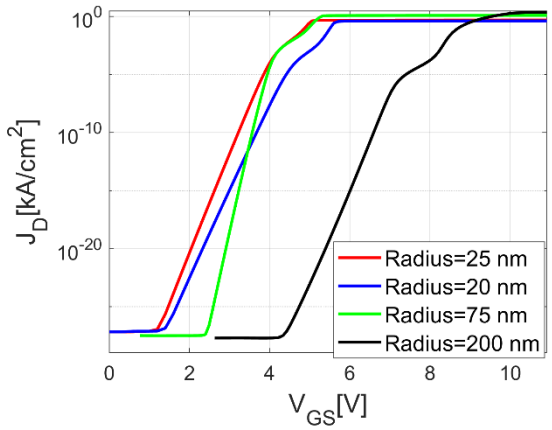


Fig. 3. Sub-threshold transfer characteristics for different pillar radius.

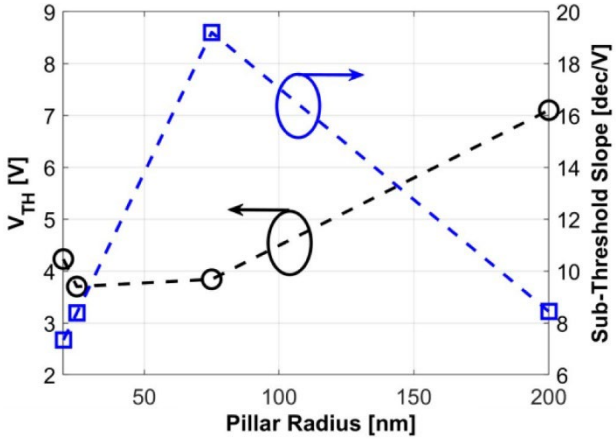


Fig. 4. V_{TH} and Sub-threshold slope dependence on the pillar radius.

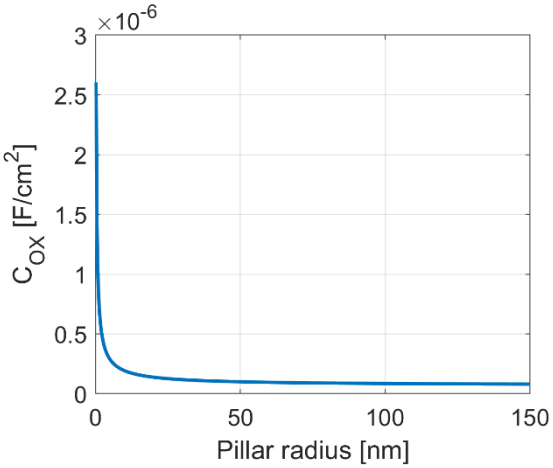


Fig. 5. Analytical C_{OX} dependence on the pillar radius.

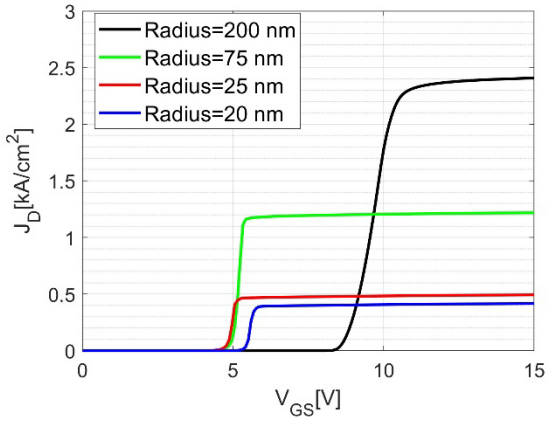


Fig. 6. High current transfer curves for different pillar radius

Simulation Results and Discussion

In Fig. 3 the sub-threshold J_D-V_{GS} are reported for the devices with a radius of 20 nm, 25 nm, 75 nm, and 200 nm. Assuming that the Vth is evaluated as the V_{GS} at 10 A/cm^2 and the sub-threshold slope is evaluated at $J_D = 10^{-10}$ A/cm^2, a peculiar behavior of the Vth is visible: it decreases when the radius decreases until 75nm, but it increases when the radius is lower than 25 nm (See Fig. 4). More in detail, the sub-threshold region has two coexisting behaviors that affect the Vth dependence on the radius: *i)* The more the radius decreases, the more the current increases for very low V_{GS} (e.g., V_{GS} = 2.5 V); *ii)* The sub-threshold slope increases until 75 nm and then it decreases for smaller radius. The latter effect is due to the ratio between C_{OX} and C_D when the radius strongly reduces. The slope in the sub-threshold region is given by eq. 1, where k is the Boltzman constant, T is the absolute temperature, C_{OX} is the oxide capacitance and C_D is the depletion region capacitance in a MOSFET device [4].

$$Slope = \frac{q}{log(10)kT}\left(\frac{C_{OX}}{C_{OX}+C_D}\right) \quad (1)$$

$$C_{OX} = \frac{\varepsilon_{OX}}{log\left(\frac{R+t_{OX}}{R}\right)R} \quad (2)$$

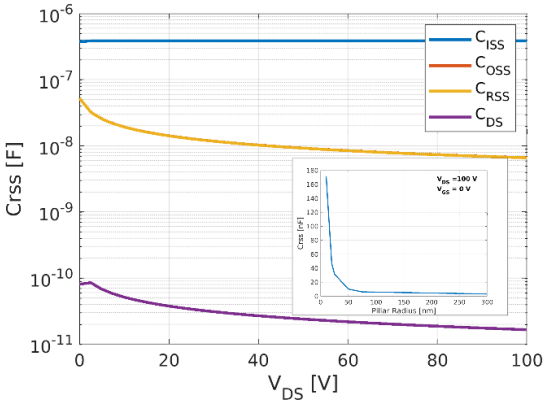


Fig. 7. C_{ISS}, C_{OSS}, C_{RSS} and C_{DS} values for pillar radius of 75 nm. In the insert the dependence of the C_{RSS} vs the pillar radius. Active Area = 1 cm^2.

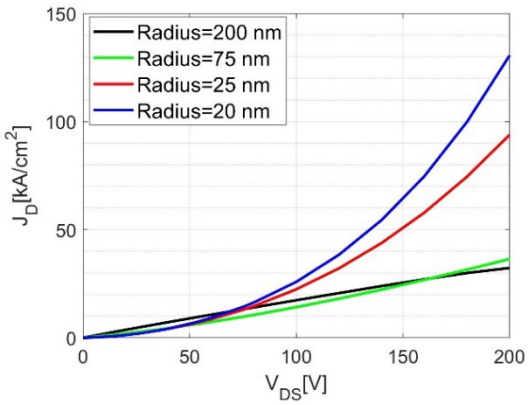


Fig. 8. Output curves for different pillar radius. V_{GS}=15 V, T=25°C. Active Area = 1 cm^2.

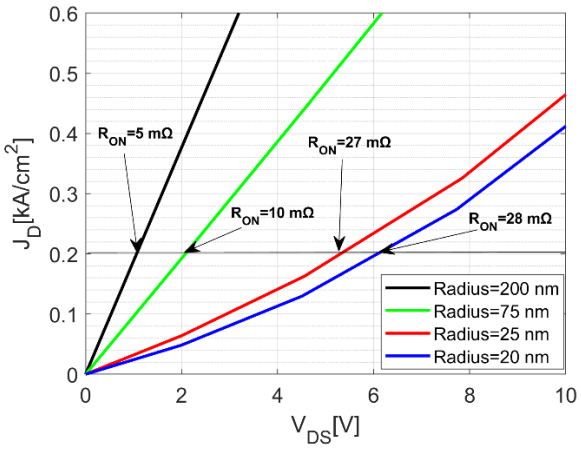


Fig. 9. A zoom of the output curves for different pillar radius. V_{GS}=15 V, T=25°C. Active Area = 1 cm^2.

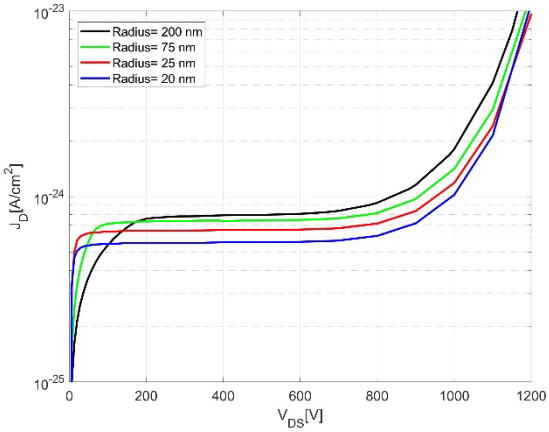


Fig. 10. blocking J_D-V_{DS} curves for different pillar radius.

The Capacity per unit of area of a cylindrical capacitor (C_{OX}) comes from eq. 2, where ε_{OX} is the oxide permittivity. It is visible as the C_{OX} increases when the radius decreases (See Fig. 5), leading to the reduction of Vth that is, in turn, inversely proportional to C_{OX}. When the radius of the pillar becomes very small, the P-Body depletion region reaches the other side of the pillar. At this point the capacitance of the P-Body region is the capacitance of capacitor with cylindrical shape and a permittivity of Silicon. When the pillar radius decreases, the C_{OX} value increase (from eq. 2) and the C_D increases faster and the slope decreases, leading to the Vth increase. Whether the radius is lower than 50nm the C_D contribution becomes dominant, leading to the reduction of the slope, with the consequent increase of the Vth.

The analysis of the high current performances is here carried out considering the current density into the SiC area of the pillar. Assuming that the oxide spacer among the pillar has a constant thickness, the current density per unit of area of the device scales down by a constant geometrical factor.

The high current density J_D-V_{GS} curves in Fig. 6 show that the reduced radius increases the series resistance at high current levels. For this design the channel resistance is comparable or lower than that of the narrow Drift-region, leading to a current limitation by the Drift-layer for low Gate voltage. The proposed design has the main advantage of having the channel region extended all over the border of the pillar. On the other hand, the Ron is limited to the narrow Drift-layer region.

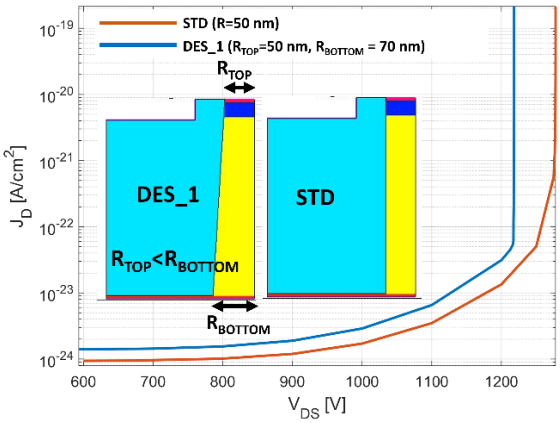


Fig. 11. Blocking J_D-V_{DS} curves for a pillar radius (R) of 50 nm, compared with a non-vertical pillar with a bottom radius of 70 nm. In the insert, a detail of the structures is reported QF = 0 cm^{-3}.

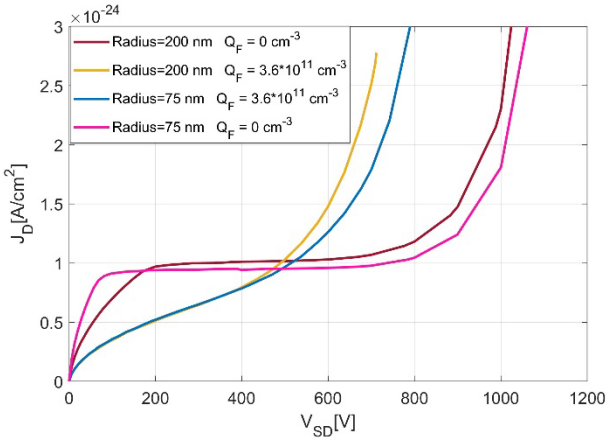


Fig. 12. Blocking J_D-V_{DS} curves for two Q_F values (0 cm^{-3} and $3.6*10^{11}$ cm^{-3}) and two pillar radius values. Pillar radius = 200 nm and pillar radius = 75 nm.

In Fig. 7 the C_{ISS}, C_{OSS}, C_{DS}, and C_{RSS} values are reported for a radius of 75 nm. Results show that the G/D and G/S overlaps are almost negligible. Interestingly, as C_{DS} values seem to be very low, this leads to $C_{RSS} \approx C_{OSS}$ and both having a similar variation with the drain voltage. In Fig. 8 the J_D-V_{DS} curves are reported for four radius values. For a Radius > 75nm the saturation current slowly decreases, while it increases more than linearly for 20 nm and 25 nm. Ron, reported in Fig. 9, is specifically evaluated at 200 A/cm^2. In Fig.10 the blocking J_D-V_{DS} characteristics are shown for designs in Fig. 3. For a constant fixed charges (Q_F) at the SiC/Ox interface, the BV is almost constant.

To account for processing variation (where the etching of the oxide mask would not yield 90° walls), Fig. 11 shows the blocking J_D-V_{DS} of a pillar with uniform radius is compared to the one of a pillar with a bottom radius larger than the standard, as well as a pillar with a smaller radius. The larger is the bottom radius, the lower is the BV of the device. Finally, in Fig. 12 the reverse J_D-V_{DS} curves are reported for two Q_F values, for two radius values. Q_F has a significant impact on the BV, and the higher is its value, the lower is the BV.

Conclusion

In this work a GAA SiC MOSFET design is presented and through TCAD simulations the main performances are addressed. The proposed design has a BV up to 1.3 kV with a pillar height of 7 µm. It shows a negligible G/D and G/S overlap, with a very low C_{DS}, leading to high switching performances. The pillar radius affects the on-state performances, and an optimal Ron is achieved with a pillar radius of 200 nm, with $R_{ON} = 5\ m\Omega$. For pillar radius lower than 75 nm, effects due to the narrow section of the pillar lead to the performance degradation in terms of conductivity. The main limitation of the proposed design is the narrow size of the Drift-layer, that for a small radius pillar has a series resistance which is higher than that of the channel region and becomes dominant. Finally, the BV of the proposed device is strongly affected by the SiC/OX interface traps concentration.

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