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Normally-off 1200V Silicon Carbide JFET Diode with Low V_F

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Keywords: Silicon carbide, JFET (Junction Field-effect Transistor), JBS (Junction Barrier Schottky), diode, forward voltage drop, capacitive charge

Abstract. Novel diode structure which looks like DMOSFETs with the gate-shorted to n^+ source has been developed for the first time. The lateral JFET channel as a built-in channel instead of gate oxide is integrated and it is pinched-off under the zero bias condition. As JFET diode decreases the forward voltage drop using JFET channel efficiency rather than the cell pitch reduction or the increase of doping concentration in n-SiC drift region, V_F and capacitive charges which have a trade-off relationship typically could be decreased simultaneously and a better switching performance is also expected accordingly. Figure-of-Merit ($=V_F x Q_C$) of the proposed JFET diode has been improved by 20.2% in average compared to that of JBS diode and this FOM would be the best in class among 1200V SiC diode products.

Introduction

Silicon Carbide has become an important electronic material due to the potential of SiC power devices to provide efficient energy distribution and management for applications such as smart grids and electric vehicles. In power devices such as high voltage diodes, low turn-on voltage can reduce the on-state power loss. However, lowering turn-on voltage of Schottky barrier diodes also reduces the associated barrier height to block the current flow at the reverse bias [1-2]. As a result, Schottky barrier diodes which adjusted the barrier height might experience the high leakage current and get into the thermal runaway particularly under the high temperature. A thermal runaway event can damage the entire system. Therefore, high voltage diodes which are less susceptible to high leakage current tend to have higher forward voltage drop which impact the conduction losses and efficiency in the application.

Results and Discussion

Fig. 1(a) shows the cross-section of conventional 1200V JBS diode and the cross-section of proposed 1200V JFET diode is shown in Fig. 1(b). JFET diode was fabricated in a way that resembles DMOSFETs with the gate-shorted to n^+ source [3]. However, the lateral JFET channel has been introduced as a built-in channel instead of gate oxide and it is pinched-off under the zero bias condition. The lateral JFET channel is electrically coupled with n^+ anode for ohmic contact. The normally-off operation of JFET channel can be controlled by using the bottom p-Gate. Both Schottky gate and bottom p-Gate are shorted through the anode metal, therefore JFET diode consists of the dual gate configuration shown in Fig. 1(b). If the forward bias is applied to the anode metal, Schottky gate and bottom p-Gate become biased positively with respect to JFET channel. Such a positive bias can turn on the channel so that it starts to be conductive. Most of channel modulation is done by the closer gate but the bottom p-Gate mainly supports a complete pinch-off aiming for the normally-off operation.

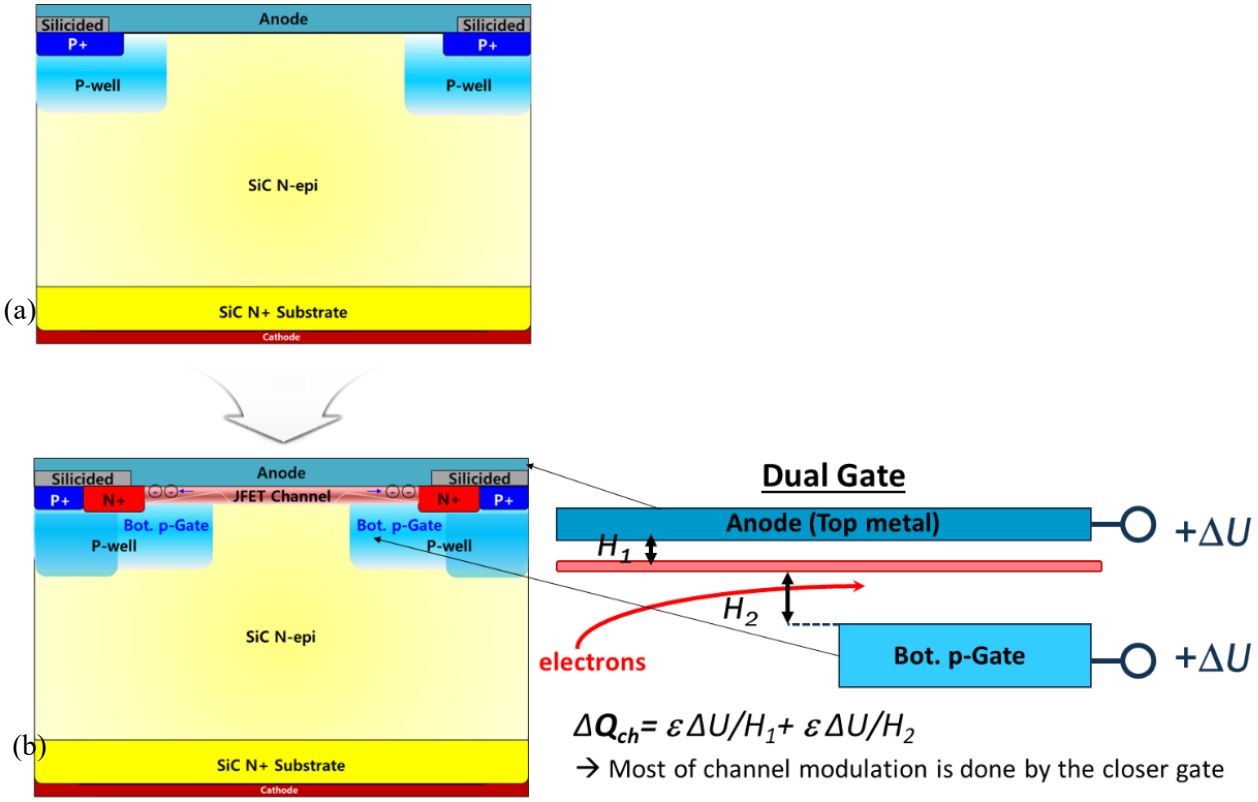


Fig. 1. Cross-section of (a) Conventional 1200V JBS diode and (b) Proposed 1200V JFET diode

Conduction mechanism of JFET diode incorporated with the nickel silicided contact process is described in Fig. 2. JFET channel is normally-off being fully depleted at V_R=1200V showing 5.6μA leakage current. Electrons through JFET channel are accumulated under Schottky metal, then Schottky metal/n-SiC barrier height becomes lowered by the potential difference. If V_{ON} greater than contact potential of Schottky metal/n-SiC is applied, Schottky current starts to flow from the anode metal to n-SiC. Here, nickel silicidation on n^+ anode region affects the channel modulation significantly, controlling the anode potential, so the conduction or pinch-off of JFET channel by the transformation of depletion region becomes effective.

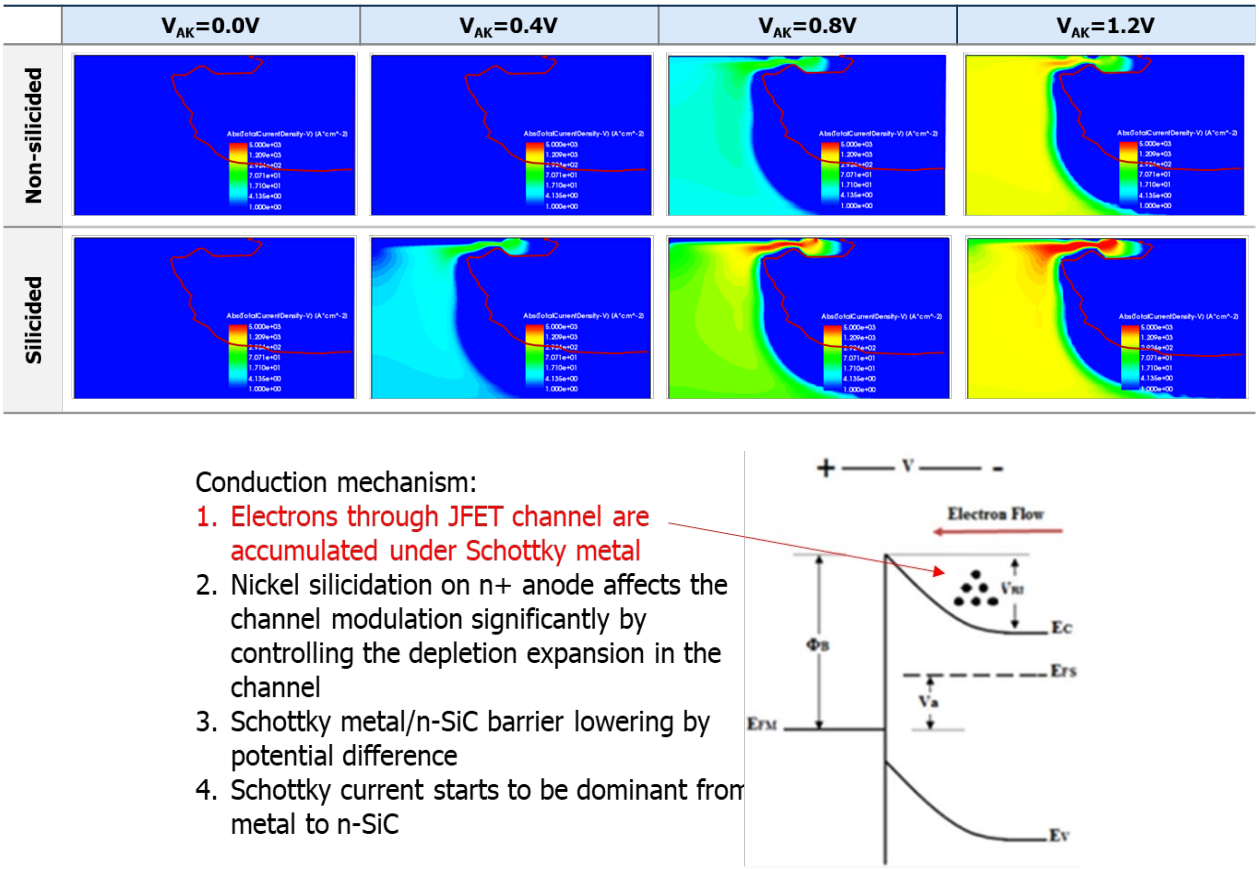


Fig. 2. Conduction mechanism of JFET diode incorporated with the nickel silicided contact process

P/N dimension of JFET diode was optimized considering the overlap windows which satisfy V_F, Q_C, and I_R criteria simultaneously as shown in Fig. 3.

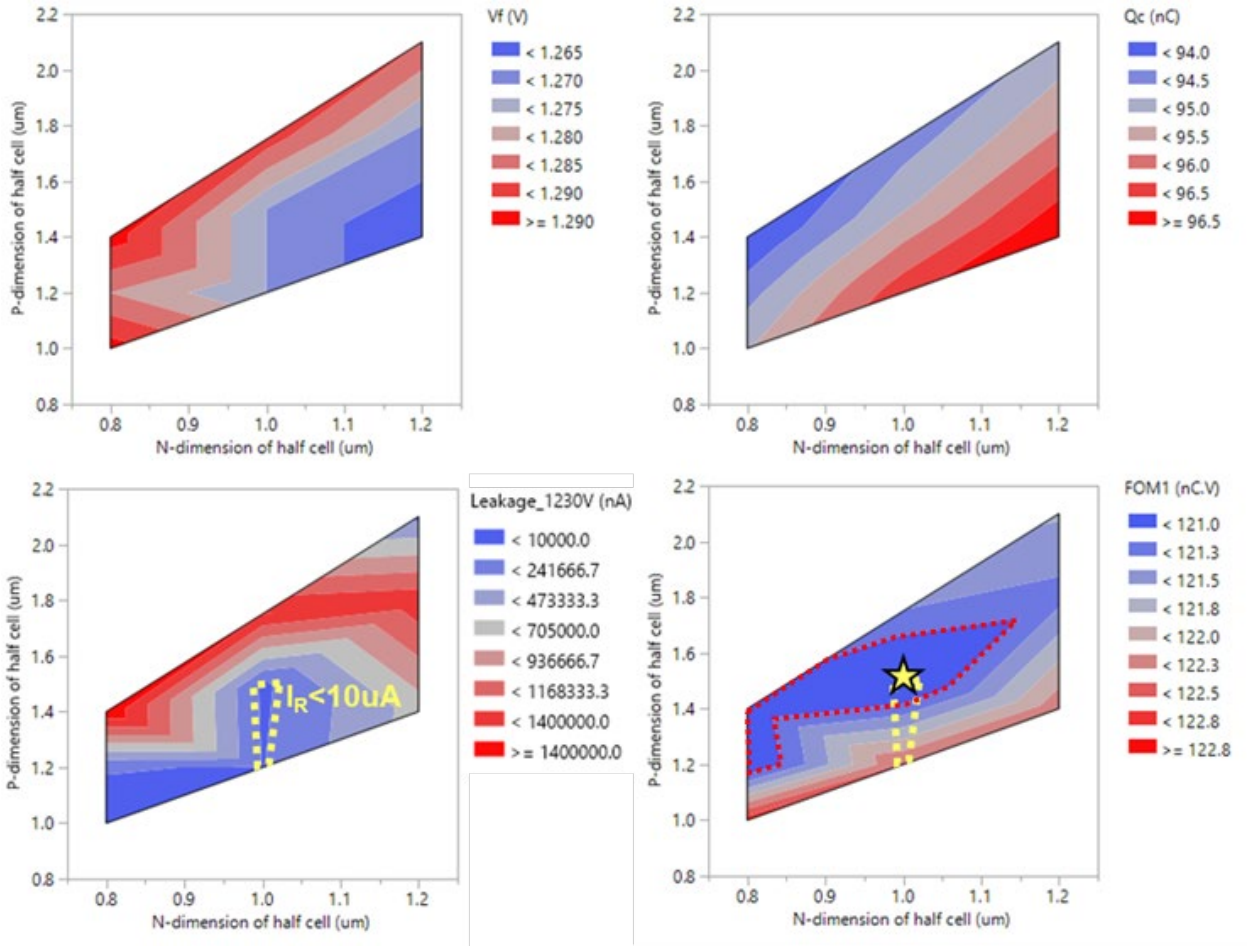


Fig. 3. Optimized P/N dimension of JFET diode based on V_F, Q_C and I_R windows

Fig 4. shows measured (a) forward, (b) reverse, (c) capacitance and (d) capacitive charge characteristics of JBS & JFET diodes. Much lower V_{ON}@6μA (0.61→0.31V) and V_F@15A (1.26→1.22V) have been achieved due to JFET channel efficiency compared to JBS diode. Even though V_{ON} was reduced significantly, I_R was constrained by 5.6μA@V_R=1200V which is similar to that of competitors due to the complete pinch-off of JFET channel. The lower drift resistance of JBS diode leads to the smaller chip size, but it would increase the capacitance simultaneously and RC product might be increased. This means the lower V_F doesn't always come up with the lower switching loss. JFET diode doesn't increase the doping concentration of n-SiC drift region to reduce V_{ON}, therefore the capacitive charge at V_{KA}=800V has been decreased by 17% compared to JBS diode and a better switching performance is also expected.

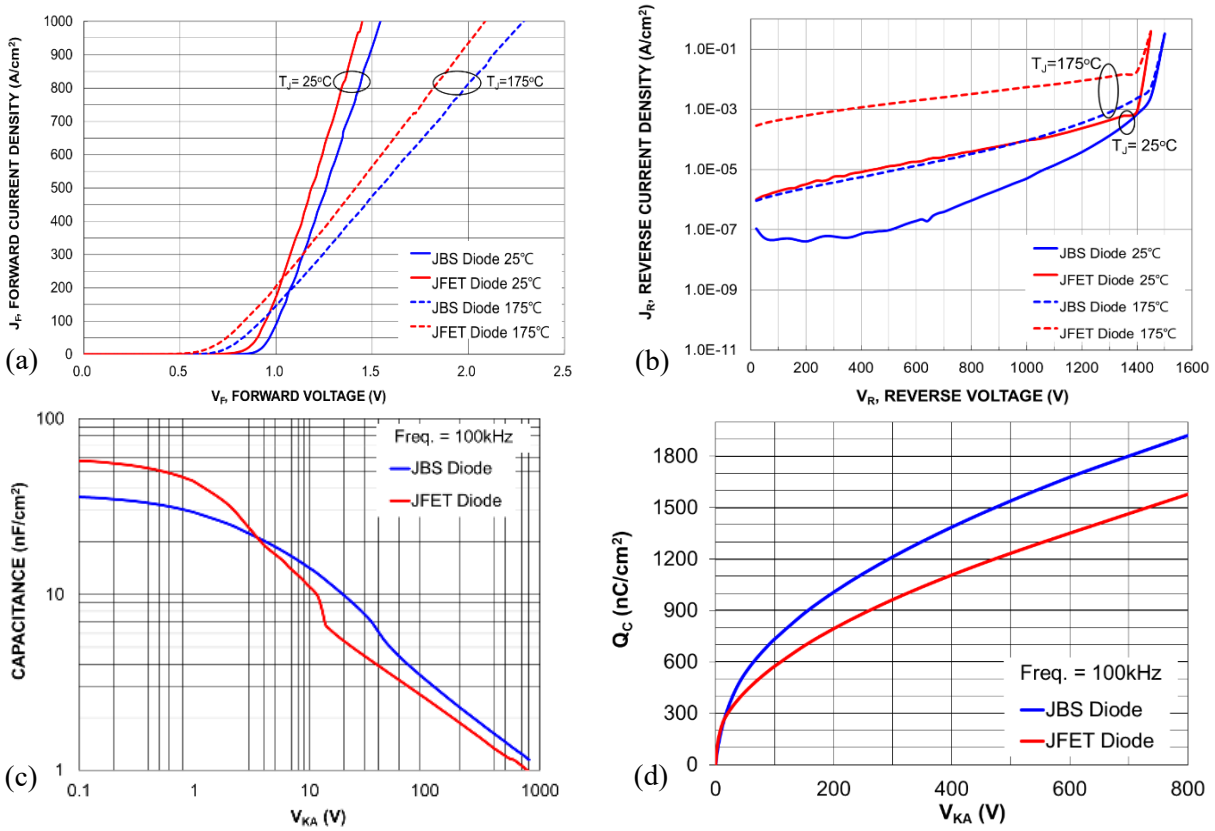
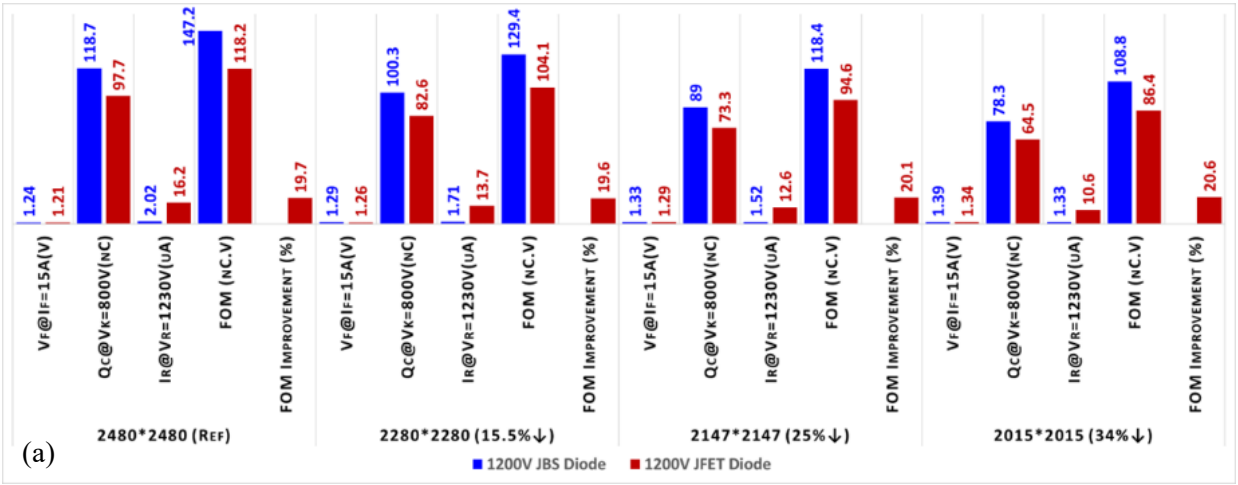
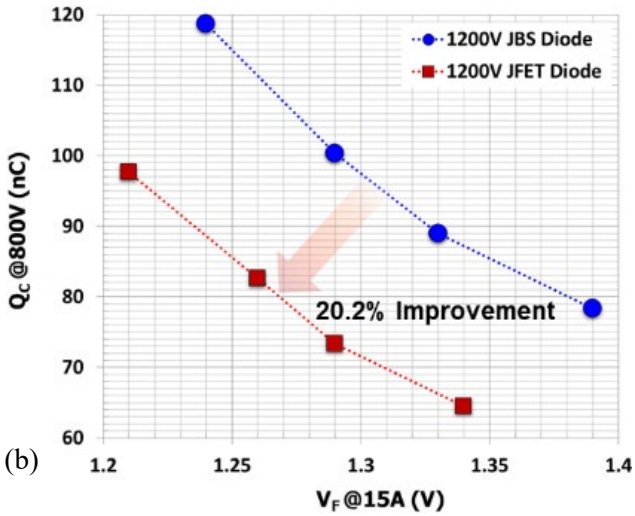


Fig. 4. Measured (a) Forward, (b) Reverse, (c) Capacitance and (d) Capacitive charge characteristics of 1200V JBS & JFET diodes

Performance comparison between JBS diode and JFET diode has been assessed by (a) Figure-of-Merit depending on different active areas and it has been plotted using (b) technology trend lines as shown in Fig. 5. V_F, Q_C, and I_R criteria were reviewed in each active area. As JFET diode decreased V_F using JFET channel efficiency rather than the cell pitch reduction or the increase of doping concentration in n-SiC drift region, V_F and Q_C which have a trade-off between each other were decreased together by 3.2% and 18% respectively.





(b)

Fig. 5. Performance comparison by (a) Figure-of-Merit depending on active areas and (b) Technology trend of 1200V JBS & JFET diodes

Summary

Figure-of-Merit (=V_FxQ_C) of the proposed JFET diode has been improved by 20.2% in average compared to that of JBS diode and this FOM would be the best in class among 1200V SiC diode products. The FOM V_FxQ_C for diodes is not fully independent of area, as the V_F decrease with increasing area is less pronounced compared to the increase in Q_C with increasing area. For this reason, FOMs become better for smaller area diodes.

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