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Investigation of the Trapping and Detrapping Behavior by the On-State Resistance at Low Off-State Drain Bias in Schottky p-GaN Gate HEMTs

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Abstract. GaN power HEMTs enable the design of power electronic systems with highest efficiencies and reduced size. Despite strong advancements in device reliability, charge carrier trapping is still an important challenge. The applied methodology allows to characterize defects that cause the dynamic $R_{DS,on}$ in GaN power devices at product level with flexibility in duty cycle, number of pulses and mission profile. A pronounced trapping is observed for lateral GaN-on-Si HEMTs with Schottky p-GaN gate structure at low drain bias and long off-state pulses (> 100 ms). The effect is investigated by fast determination of the on-state resistance $R_{DS,on}$ under different trap capturing conditions: a) different drain bias b) off-state time and number of cycles c) variation of temperature. The trapping and detrapping effects are characterized and the activation energy is extracted from time constants. An elevated on-state resistance was present for up to 3 hours. The threshold voltage modification due to high drain bias does explain the significant $R_{DS,on}$ increase.

Introduction

The investigations of the trapping behavior on GaN power devices focus on instabilities of the threshold voltage and the on-state resistance $R_{DS,on}$. Different studies investigated the impact of drain bias on the threshold voltage of Schottky p-GaN devices [1]–[3]. In [1], a positive threshold voltage shift and low drain bias ($V_{DS,q}$ = 50 V) was highlighted in short term (< 10 ms) and long term stress of several seconds. The $V_{G,th}$ shift at long term stress increased by approx. 70 % and was observed for more than 30 minutes. This particular trapping condition presents a reliability issue and requires further investigation. A positive threshold voltage shift implicates an increase in $R_{DS,on}$ and entails higher conduction losses, but also increases the switching losses. In this investigation, the impact of drain bias stress, mission profile and temperature on the trapping behavior are visualized by the on-state resistance under pulsed-IV-conditions.

Dynamic on-state resistance $R_{DS,on}$ in Schottky p-GaN Gate HEMTs

The dynamic $R_{DS,on}$ is defined in the ohmic region of GaN devices [4]. There are various parameter that influence the dynamic $R_{DS,on}$ such as the applied bias in quiescent (preconditioning) condition (drain bias $V_{DS,q}$/ negative gate bias $V_{GS,q}$), the device temperature T, quiescent off-time (t_{off}) and the mission profile. It is therefore advisable to vary only one parameter and keep the other parameters unchanged. As an example, the preconditioning time t_{off} was varied at constant off - conditions ($V_{DS,q}$ = 50 V, $V_{GS,q}$ = 0 V), constant temperature and constant drain current pulse (I_D = 19 A, $V_{GS,on}$ = 6 V). An additional delay of 1 s between the single measurement points was introduced to reduce self-heating as well as the accumulation of the stress and thus the impact on the consecutive measurement points. The result is depicted in Fig. 1 and two effects are visible in the course of the $R_{DS,on}$: First, an overall elevation of 10 % is present even in the range of microseconds, which is in the same temporal range as the positive threshold voltage shift observed in [1], [2]. For longer off-

state times, the on-state resistance rises strongly by more than 30 % between 1 s and 100 s. This increase could be caused by ionization of buffer traps [1], [4], [5], [6]. For a single, discrete trap energy level, the capture dynamic of an electron can be described as

$$n_{T,filled}(t) = N_T \cdot \left[1 - \exp\left(\frac{\mathrm{t}}{\tau_{cn}}\right)\right]$$

with the total amount of traps N_T, $n_{T,filled}$ being the filled portion of N_T and the electron emission time constant τ_{cn} [5]. The saturation of the trap level is reached for $\frac{n_T}{N_T} \approx 1$. The exponential progression allows to determine the time constants of the filling and consecutive recovery process.

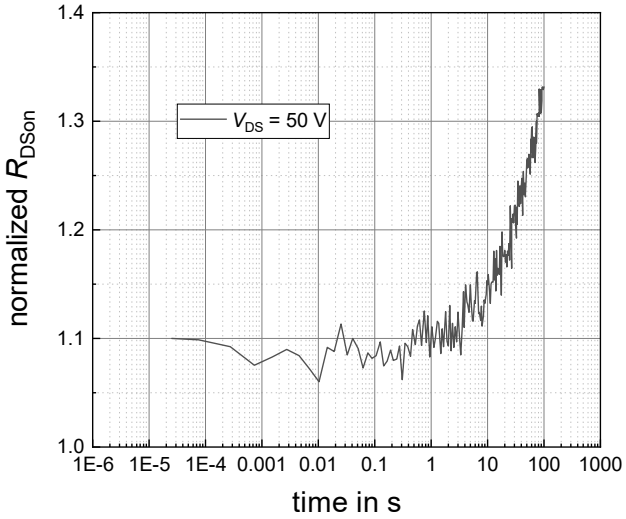

Fig. 1. Behavior of the dynamic $R_{DS,on}$ with increasing off-state stress time t_{off} at T = 25°C for pristine 25 mΩ device [6] under consecutive measurement acquisition with delay of 1 s ($V_{DS,q}$ = $V_{GS,q}$ = 0 V)

Methodology and Setup

For this work, a self-built pulsed IV test from [7] is used, which allows to apply a high quiescent drain voltage $V_{DS,q}$ as preconditioning to the device under test (DUT). The test circuitry is depicted in Fig. 2. The drain bias at the DUT and drain current are controlled separately by the V - and I - switch, respectively. The three switches are controlled by separated gate drivers for the MOSFETs and a suitable gate driver for the DUT GaN HEMT. The control is performed according to the pulse pattern in Fig. 3. The measurement approach operates under an experimental (not application-close) soft-switching operation without overlap of drain current I_D and drain bias V_{DS}. Any operation in the active area of the DUT is to be avoided and thus also any degradation related to hard switching. The free adjustment of the drain bias allows to drive different mission profiles and also to perform a static $R_{DS,on}$ measurement without preconditioning of $V_{DS,q}$ prior to the examination.

The focus of this investigation is on the trapping and detrapping behavior at long off-state preconditioning times > 1 s. The studied DUTs are commercially available Schottky p-GaN gate HEMTs with a rated voltage of 650 V. Two different specimens with a rated on-state resistance of 25 mΩ and 150 mΩ were used. In general, a pristine component was used for each series of measurements to avoid any influence on the subsequent stress. The measurement sequence is divided into three different states as illustrated in Fig. 5. INITIAL: static $R_{DS,on}$ measurement; TRAPPING: repetitive $R_{DS,on}$ measurements until saturation of the $R_{DS,on}$ is reached; DETRAPPING: static $R_{DS,on}$ measurements in four stages, where each has a dedicated off-time and number of repetitive cycles. For reproducibility and subsequent analysis, the DUT is turned on for a time interval of 5 µs ($V_{GS,on}$ = 6 V), in which the $R_{DS,on}$ is characterized by drain current pulse of 3 µs. The averaging window for $R_{DS,on}$ determination is always between 2.5 µs and 2.6 µs (see Fig. 4). For the initial static $R_{DS,on}$ of every device value, ten repetitive static pulses were performed with an interval of 10 ms each. The dynamic measurements are normalized to the average of this values. After the on-state

resistance of the device has reached saturation, the detrapping can be determined in different stages with static measurement pulses and no drain bias applied.

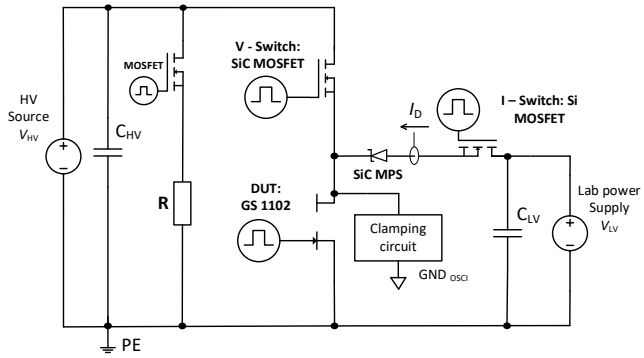

Fig. 2. Test circuit for preconditioning pulsed IV operation with separate current and voltage adjustment

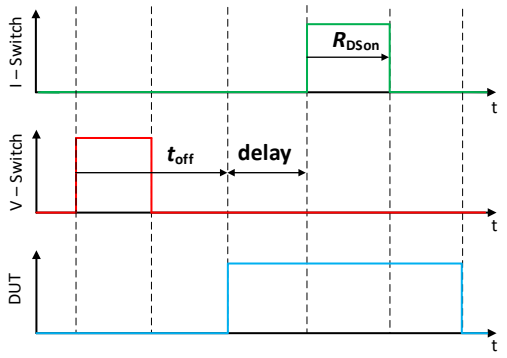

Fig. 3. Pulse pattern of the 3 switches with off time, delay and $R_{DS,on}$ determination

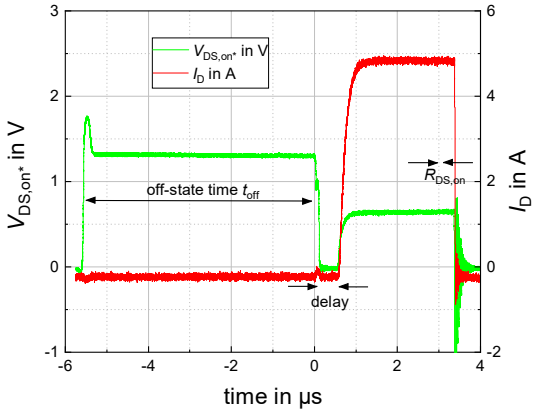

Fig. 4. Exemplary waveform of clamped $V_{DS,on}$ and I_D with off-state time, delay and $R_{DS,on}$ measurement window at $V_{DS,q}$ = 50 V, t_{off} = 5 µs, T = 25°C; 150 mΩ device [8]

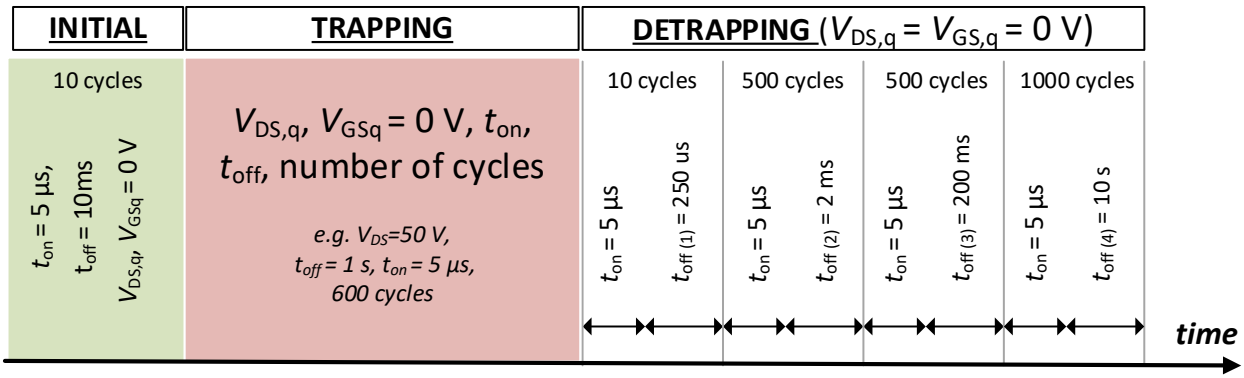

Fig. 5.Illustration of the initial stage as well as trapping and detrapping phase for the dynamic $R_{DS,on}$ measurement

The worst-case temperature increase due to the repetitive drain current pulses occurs at the end of the detrapping stage 1. The temperature increase is equal to the thermal impedance divided by the power dissipation. The single pulse power dissipation of 7.5 W at an applied duty cycle of 0.02 results with the thermal impedance at 2.5 ms of approx. 1 K/W in a low temperature increase of 0.09 K. The capacitive losses E_{OSS} by charging and discharging the output capacitance during the trapping phase to drain bias are neglected at frequency of 1 Hz (t_{off} = 1 s).

Results and Significance

Trapping and detrapping were characterized by determining the on-state resistance variation as function of drain bias, time and temperature and number of cycles. The devices were stressed by 600 consecutive preconditioning pulses of 1 s. The drain bias $V_{DS,q}$ is varied and without negative gate bias ($V_{GS,q} = 0$ V). In doing so, the trap-filling process can be accelerated by increasing the quiescent drain voltage $V_{DS,q}$ from 50 V to 400 V (Fig. 6). The curves are normalized to the average of the 10 initial, static $R_{DS,on}$ values. An analysis of the first dynamic value alone is associated with a certain uncertainty of the initial state. Hence, the last values at 600 s were transferred to Fig. 7. Between 50 V – 200 V, the dynamic $R_{DS,on}$ is significantly elevated at 600 s and has its maximum value at 150 V. Nevertheless, it must be noted that pristine devices were measured and variations between the single specimen can have an influence. However, the required cumulated off-time to reach saturation decreases significantly with drain bias e.g. at 200 V. At higher drain voltages, a compensation effect to the trapping occurs due to increased buffer leakage current [9]. In [1], the change in threshold voltage saturated and was constant above a drain bias 50 V. As a result of the constant degradation and for comparison, a drain bias of 50 V was chosen to investigate the trapping behavior. In Fig. 8, the stress time of 600 s was varied by setting different mission profiles. Since there is only a very short relaxation during the measurement window of 5 µs, the 600 s stress can be accumulated by one pulse as well as by 600 individual pulses.

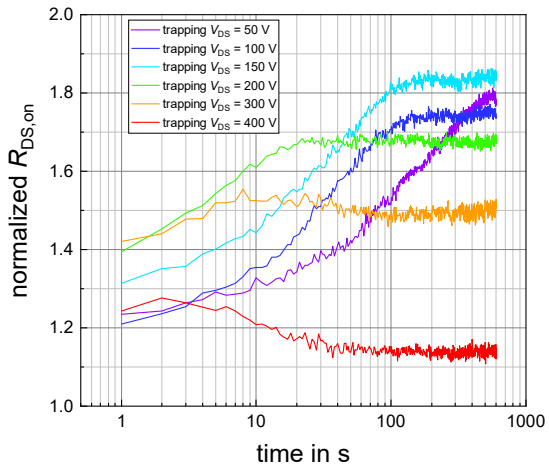

Fig. 6. Impact of the trapping on the $R_{DS,on}$ at different drain bias $V_{DS,q}$ and $T = 25$°C; shown for different preconditioning voltages (25 mΩ devices [6])

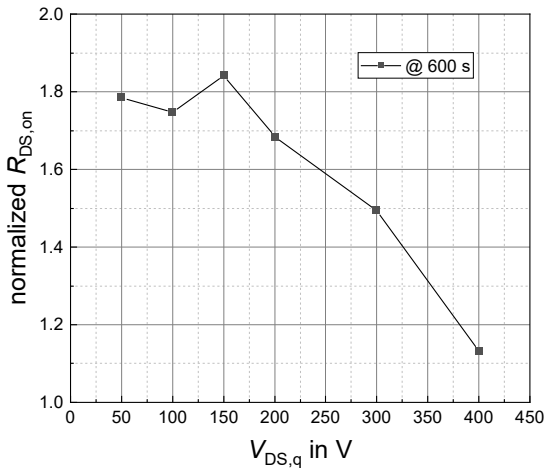

Fig. 7. Dynamic $R_{DS,on}$ depending on different quiescent drain bias $V_{DS,q}$ ($T = 25$°C) extracted from Fig. 6 (25 mΩ devices [6])

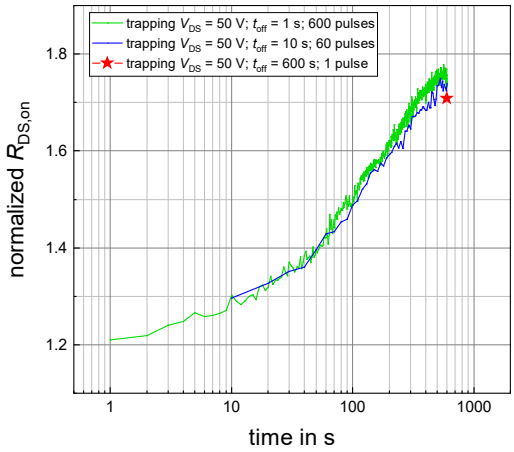

Fig. 8. Trapping accumulation by measurement of the $R_{DS,on}$ under different off-state conditions at $V_{DS,q} = 50$ V, $T = 25$°C

The temperature dependent investigation was performed on the second type of the devices with 150 mΩ. The trapping behavior at quiescent condition of 50 V and 25°C is even more distinctive. A

strong thermal activation of the trapping and detrapping was observed. At 120°C, approx. 7 s are sufficient to reach saturation of the trapping process at 50 V (see Fig. 9). On the other hand, as depicted in Fig. 10, the temperature can accelerate detrapping time. One significant exponential rise is visible during the trapping process and two exponential decays were observed during the detrapping. Hence, two time constants are expected to be present. Whereas, the condition of 600 pulses with off time of 1 s transitions the time constant described in [1] are in the range of milliseconds. The trapping phenomenon is particular critical at lower temperature, as it takes 10 ks (approx. 3 hours) for complete recovery. At elevated temperature, the detrapping process is completed in shorter time. At 90°C and 120°C, after declining of the exponential detrapping process, the resulting $R_{DS,on}$ values did not reach the initial value, but were decreased. The separation point of the 2 detrapping characteristics fit very well to the results presented in [1]. The time constants of the trapping process were extracted to an Arrhenius plot in Fig. 11. The slope reveals an activation energy of $E_A = 0.314$ eV for the trapping process. This is in good alignment with the activation energy of 350 meV during the detrapping in [9]. The determination of time constant is challenging and higher precision of the activation energies can be achieved by increasing number of temperature levels.

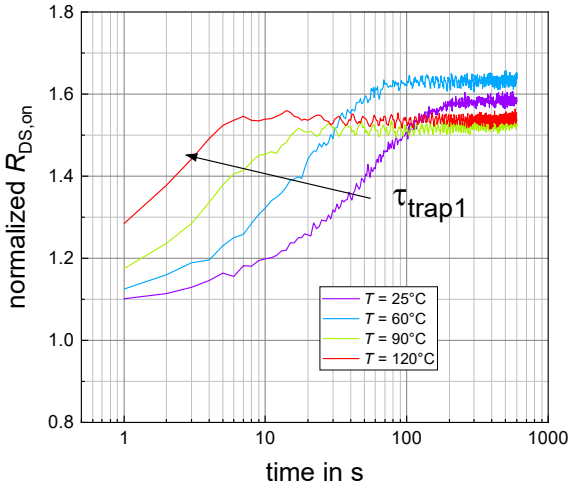

Fig. 9. Temperature dependent trapping behavior under repetitive operation

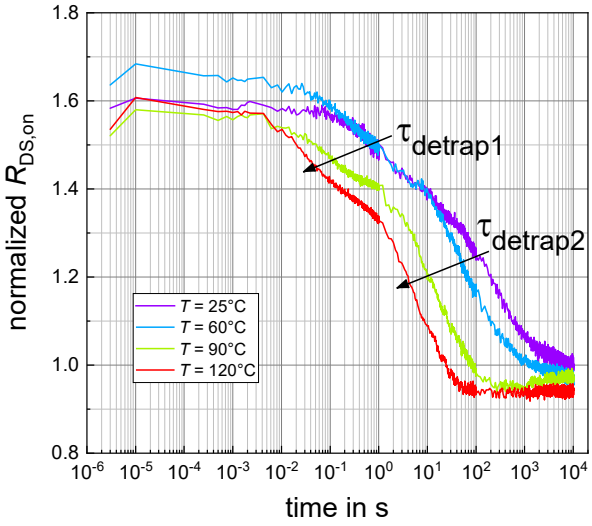

Fig. 10. Temperature dependent detrapping behavior under repetitive operation

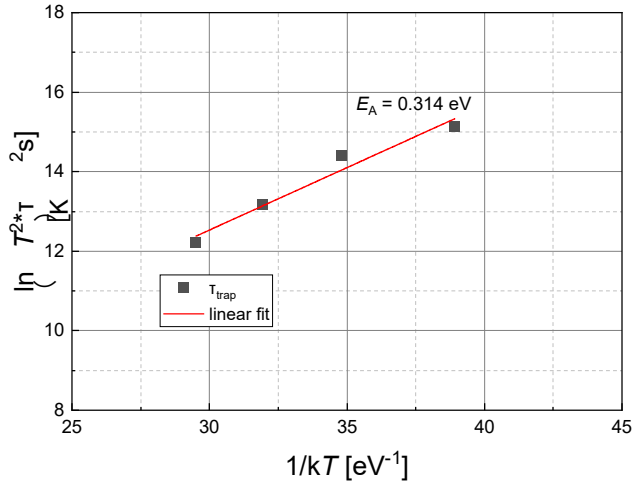

Fig. 11. Arrhenius plot of the trapping time constant with an activation energy of $E_A = 0.314$ eV

Additionally, static measurements of the threshold voltage were performed using a Keysight SMU (Source-Mea surement-Unit) in a different setup. A pristine DUT was stressed in the dynamic setup with $V_{DS,q} = 50$ V for 600 s and subsequently characterized by shorted drain-gate. Fig. 12 shows an increase of 53% at 120 s after the stress, which is in very good agreement with [1]. Similarly, static

leakage current I_{GSS} and I_{DSS} were conducted. No significant changes were observed. An evaluation of the threshold voltage by means of the $R_{DS,on}$ for GaN HEMTs is complex due to the different shares of the $R_{DS,on}$ and the lateral device structure. Fig. 13 displays the $R_{DS,on}$ against change in gate voltage with respect to the nominal gate voltage of 15 V and 6 V for the SiC MOSFET and the GaN HEMT, respectively. It can be seen, that the change in threshold voltage has only a minor impact on the $R_{DS,on}$ of the GaN HEMT. Hence, the threshold voltage is not responsible for the strong change in $R_{DS,on}$. It is therefore likely that the change is caused by buffer trapping [9]. Compared to SiC MOSFETS the influence of the $V_{G,th}$ to $R_{DS,on}$ changes is found to be smaller for GaN HEMTs.

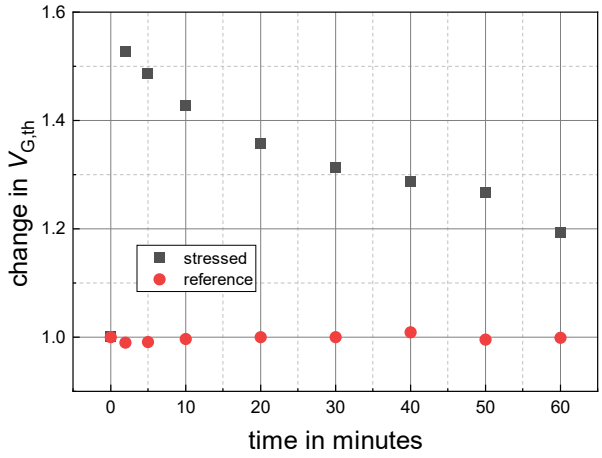

Fig. 12. $V_{G,th}$ after preconditioning with $V_{DS,q} = 50$ V for 600 s in comparison to an unbiased reference device ($T = 25$°C)

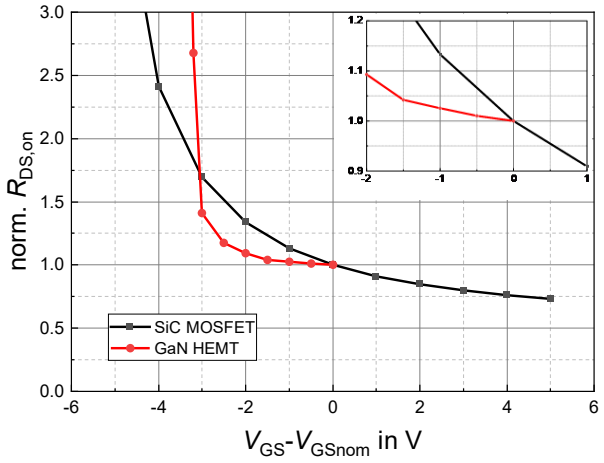

Fig. 13. Normalized $R_{DS,on}$ against change of gate voltage with respect to the nominal gate voltage for GaN HEMT [8] and SiC MOSFET [10] ($T = 25$°C)

Conclusion

The presented methodology for dynamic $R_{DS,on}$ acquisition enables very fast determination under pulsed IV condition with high flexibility in preconditioning and pulse pattern. A pronounced trapping effect of on-state resistance rise by more than 80% can be introduced by low drain bias of 50V. Moreover, the dynamic $R_{DS,on}$ can be accumulated by different mission profiles. The process implies recovery process of 3 hours and must be kept in mind for dynamic $R_{DS,on}$ characterization, reliability testing or converter application. Also, the saturated value of the $R_{DS,on}$ reduces above 200 V. An elevated threshold voltage was observed, but cannot be linked to the increase in on-state resistance. The methodology is not limited to GaN, but could be adapted to SiC MOSFETs or β-Ga_2O_3 devices.

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