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On the TCAD Modeling of Non-Permanent Gate Current Increase During Short-Circuit Test in SiC MOSFETs

Jaume Roig[1,a*], Sara Kochoska[2,b], Basil Vlachakis[1,c], Jimmy Franchi[3,d] and Thanh-Toan Pham[3,e]

[1]onsemi, Westerring 15, 9700 Oudenaarde, Belgium

[2]onsemi, Einsteinring 28, 85609 Aschheim, Germany

[3]onsemi, Isafjordsgatan 32C, 16440 Kista, Sweden

[a]jaume.roig@onsemi.com, [b]sara.kochoska@onsemi.com, [c]basil.vlachakis@onsemi.com, [d]jimmy.franchi@onsemi.com, [e]Thanh-Toan.Pham@onsemi.com

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Abstract. Under short-circuit (SC) testing SiC MOSFETs exhibit an exceptional increase of gate current (100's mA) which is not observed in their Si counterparts. Electro-thermal TCAD simulations are capable to accurately mimic all the details of measured gate current waveforms (i_G) by capturing multiple physical mechanisms. One of these mechanisms is the thermionic or Schottky emission effect occurring at extreme temperatures (>1300K) for relatively thick gate oxides (>40nm). For the first time, it is proven that TCAD tunneling models, recommended for very thin oxides (<3nm), are suitable to reproduce the thermionic effect and predict i_G in SiC MOSFETs under SC test.

Introduction

SiC power devices have gained significant attention in recent years due to their superior performance compared to traditional silicon-based devices. However, the design and optimization of SiC power devices pose unique challenges, particularly in the realm of Technology Computer-Aided Design (TCAD) modeling. TCAD physical models play a crucial role in simulating and predicting the behavior of semiconductor devices, aiding in their design, fabrication, and reliability assessment.

The transition from Si to SiC introduces several complexities that make TCAD modeling for SiC power devices a challenging task. First, SiC exhibits unique material properties, such as wide bandgap, high breakdown voltage, and high thermal conductivity, which significantly improve device performance [1, 2, 3]. Most of these material properties lack a standardized material parameter database for SiC. Second, SiC devices can exhibit complex physical phenomena, including trapping and recombination mechanisms, interface states, electro-thermal anisotropy, and surface roughness effects [4, 5, 6, 7, 8]. Third, SiC power devices often operate at higher temperatures and switching frequencies, leading to increased power densities and self-heating effects.

An accurate representation of electro-thermal effects in TCAD models is crucial for predicting device behavior in short-circuit (SC) test. SC withstanding time (SCWT) is a critical success criterion in inverters for motor control and its simulation requires a combination of TCAD and SPICE elements in the so called mixed-mode (MM) approach. Reproducing SC measured waveforms is only possible by accounting for test circuitry and parasitic elements [9, 10]. Moreover, it has been recently discovered that SiC MOSFETs under SC exhibit unique physical mechanisms that may shape i_G waveforms (see Fig. 1) [11, 12, 13]. Here, i_G refers to non-permanent current and unrelated to thermo-mechanical degradation [12]. In a previous work [13], i_G in Regions 1 and 2 was categorized as displacement current. Differently, i_G in Region 3 is dominated by thermionic effect through the gate oxide [14]. This work is devoted to the TCAD modelling of Region 3 by means of tunneling models offered by a software vendor [15]. In a first section, these models will be succinctly explained. A second section is focalized on 1D TCAD simulations of SiC MOS to investigate these models and their dependencies. In the end, a third section focuses on 2D TCAD simulations with calibrated power MOSFET structures using tunneling models and being eventually compared with measurements.

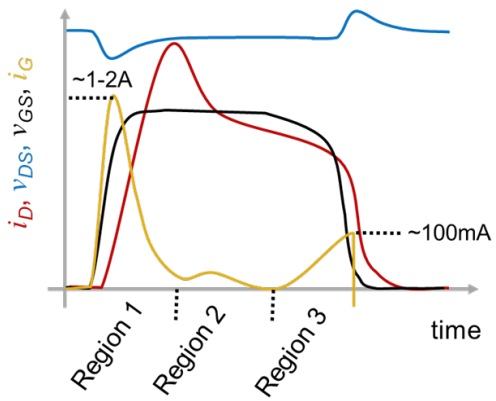

Fig. 1. Schematic representation of i_G, v_{GS}, v_{DS} and i_D waveforms in SiC MOSFETs during a non-destructive SC test. This work is focused on TCAD physical models for Region 3.

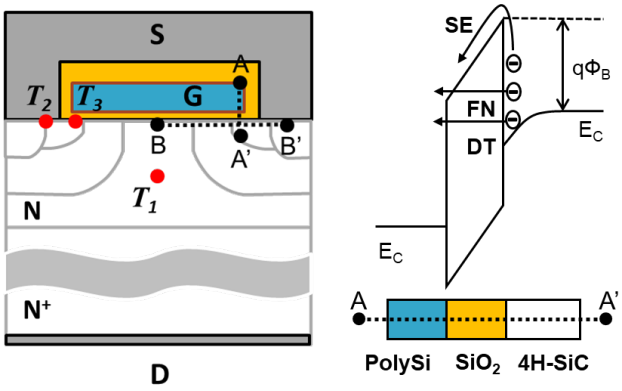

Fig. 2. Schematic cross-section of planar SiC MOSFET with a description of temperature points T_1, T_2, T_3, cutlines AA‘ and BB‘, and band diagram along AA‘ cutline in inversion conditions.

Physical Models for Tunneling and Schottky Emission

Electron tunneling models for MOS structures play a fundamental role in nanoscale dimensions [16]. It refers to the phenomenon where electrons traverse an oxide barrier in MOS devices, influencing device characteristics such as leakage current, gate capacitance, and subthreshold slope. For relatively low temperature and high electric fields (>6MV/cm) the Fowler-Nordheim (FN) model is commonly used to analytically calculate the tunneling electron current density by

$$j_{FN} = \frac{q^3}{8\pi h \Phi_B} \cdot {E_F}^2 \cdot e^{-\frac{8\pi\sqrt{2m_{ox}{\Phi_B}^3}}{3qhE_F}} \tag{1}$$

where q is the elementary charge, h the Plank’s constant, Φ_B the semiconductor-oxide barrier height, m_{ox} the effective mass of electron in the oxide and E_F the electrical field magnitude. SC temperatures can surpass 1200K in the gate oxide (T_3 in Fig. 2), thus enhancing the electron energy over the potential barrier energy as it occurs in Schottky emission (SE). Hence, a more suited model for a scenario with medium E_F and high T_3 is the analytical formula for SE in [14]

$$j_{SE} = \frac{4\pi q k^2 m_{ox}}{h^3} \cdot T^2 \cdot e^{\frac{-\Phi_B + \sqrt{q^3 E_F/(4\pi\varepsilon_r\varepsilon_0)}}{kT}} \tag{2}$$

where T is temperature, k is Boltzmann’s constant, ε_r and ε_0 are the relative and vacuum permittivities. A fundamental difference between Eq. 1 and Eq. 2 is the Φ_B dependence with T. In Eq. 1, $\Phi_B(T)$=2.914 - 7.116·10^{-4}·T eV, whereas Φ_B=2.7eV is constant in Eq. 2 due to the explicit T^2 dependence. In TCAD simulations there are two available tunneling models for 1D, 2D and 3D MOS structures that are described in the following. Aside from capturing tunneling effects like FN and direct tunnelling (DT), the SE mechanism is also supported for electrons with energies above the potential barrier as schematically described by the energy band diagram in Fig. 2. Other tunneling mechanisms like trap-assisted-tunneling (TAT) are neglected in this study but they may be relevant for gate oxides with low quality and a high density of near-interface traps.

Direct Tunneling Model (DT) is a robust and simple approach to compute the tunneling currents in MOS structures. Its application is restricted to tunneling through insulators due the assumption of a trapezoidal energy barrier and it incorporates the concept of the transmission coefficient (ϒ) in accordance with the model presented in [15]. The electron current density is expressed as

$$j_{DT} = \frac{qm_c k}{2\pi^2 h^3} \int_0^\infty \Upsilon(E) S(E) dE \quad (3)$$

where m_C is a mass prefactor (m_C=0.32m_0) and E is the energy of the elastic tunneling process. Inside the integral in Eq. 3, S(E) is a function derived from the integration of the Fermi–Dirac distribution function, multiplying the temperature at the two sides of the oxide barrier. $\Upsilon(E)$ is the transmission coefficient, which is a measure of the probability that an electron will successfully tunnel through the barrier. $\Upsilon(E)$ has intrinsic dependences on Φ_B, E_F, effective thickness of the barrier (d), and effective masses in gate contact, insulator and semiconductor substrate (m_G=m_0, m_{ox}=0.5m_0 and m_{SiC}=0.23m_0 for electrons in SiC MOS). For a 1D MOS structure, d is merely the oxide thickness (t_{ox}), however a 2D scenario requires an analysis along different d paths for every SiC/SiO_2 interface point. A complete description of the model formulation and implementation is available in [15].

Non-Local Tunneling Model (NLT) is the most versatile modeling approach used to accurately simulate carrier tunneling but it also implies high computational cost. NLT considers the electron transport through the entire device region, accounting for a spatial variation of E_F and its impact on the tunneling probability. As in DT, it is also based on a transmission coefficient Υ, however Υ computation follows the WKB approximation, and it could be optionally done with 1D Schrödinger equation [18]. Differently from DT, NLT handles arbitrary barrier shapes, includes carrier heating terms, and allows to describe tunneling between the valence band and conduction band.

1D MOS Analysis

In order to perform a simplified comparison between models, a 1D MOS TCAD structure is built following the layer stack described by AA' in Fig. 2. This basic structure is constituted by a SiO_2 layer with t_{ox}=50nm sandwiched between two highly doped n-type 4H-SiC and PolySi layers. An area factor to convert current density into current (I_A) is roughly estimated by considering the die area and the overlap between N^+ source and PolySi gate in a commercial 1.2kV SiC MOSFET [19], named as DUT1 in this manuscript. Electrical simulations are conducted by sweeping the AA' potential ($V_{AA'}$) in stationary conditions for different temperatures. The simulated I_A vs. $V_{AA'}$ and I_A vs. T curves are plotted in Figs. 3 and 4, respectively, including the analytical calculations from the sum of Eq. 1 and Eq. 2. It is inferred from Fig. 3 that all the models generate an I_A in a range between mA and A for the typical SC conditions of V_{GS} and Temperature (V_{GS}~$V_{AA'}$).

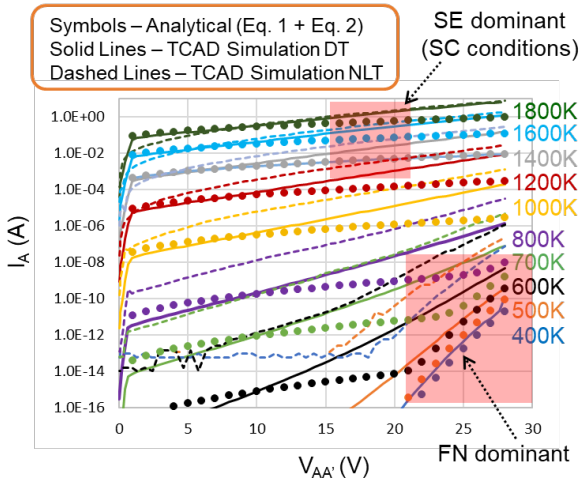

Fig. 3. I_A vs. $V_{AA'}$ for different Temperatures (400K-1800K) comparing 1D TCAD simulations (NLT & DT) and analytical calculations (Eq. 1 + Eq. 2). DT uses Φ_B (T).

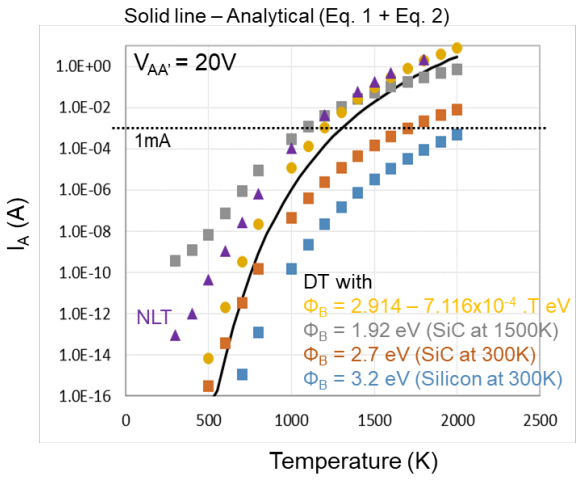

Fig. 4. I_A vs. Temperature at $V_{AA'}$=20V comparing 1D TCAD simulations (NLT & DT) and analytical calculations (Eq. 1 + Eq. 2). DT uses Φ_B (T) and constant Φ_B.

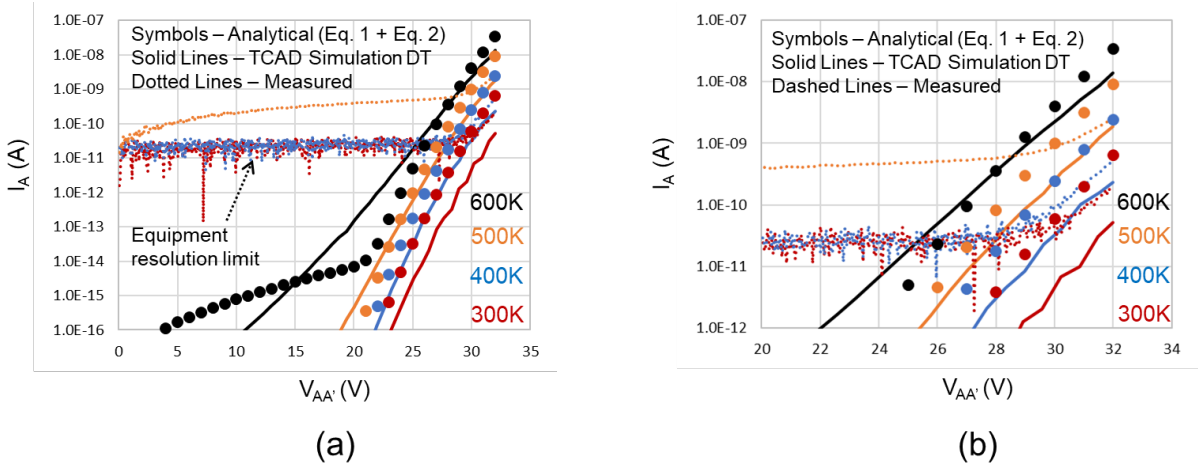

Fig. 5. (a) I_A vs. $V_{AA'}$ for different temperatures (300K-600K) from measurements, 1D TCAD simulations (DT) and analytical calculations (Eq. 1 + Eq. 2). (b) Zoom in (a) for the region dominated by FN effect ($V_{AA'}$>20V)

The good match between NLT and DT models at $V_{AA'}$=20V is better observed from the yellow and violet symbols in Fig. 4 when T>1200K, where both models show an I_A above the analytical calculations. In terms of computational speed, DT runs two times faster than NLT and is less prone to suffer convergence issues. To further simplify the DT model, a constant Φ_B is evaluated. It can be observed by Fig. 3 (grey symbols) that using an average Φ_B=1.92eV, which is the value provided in [20] at 1500K, is also a reasonable approach. On the other hand, fixing Φ_B=2.7eV (orange symbols), which is the value assumed at 300K, leads to an I_A drop of two orders of magnitude in the I_A-Temperature space of interest. Finally, it is also interesting to observe that Φ_B=3.2eV, typically used in Si at 300K, diminishes I_A in one order of magnitude compared to SiC at 300K. This means that i_G Region 3 is not expected to be noticeable in Si MOS devices due to the larger barrier height.

A deeper analysis of a scenario dominated by FN is possible from Fig. 5. Moreover, Fig. 5 includes I_G stationary measurements in DUT1 for temperatures below 500K. At relatively low temperature, a FN dominance is observed for $V_{AA'}$>20V. Despite the current resolution limit of the B1505 curve tracer (~$1 \cdot 10^{-11}$A), it can be observed that both DT simulations and analytical formulas are able to predict the right order of I_G magnitude. As shown in Fig. 3, NLT simulations exhibit four orders of magnitude larger I_A, thus being less accurate than DT in conditions with predominant FN.

2D Power MOSFET Analysis

This section reports the results from SC test in MM simulations with DT model. Aside from the DT model, the rest of the TCAD models related to electrical properties and the test setup parasitics were calibrated in preliminary works for DUT1 [1, 9, 10]. To properly account for the self-heating effect, reported SiC thermal models are used [3]. It is worth to point out that prior works never included TCAD tunneling models to replicate i_G in this specific scenario. As a closest reference, a circuit model for i_G was developed for electro-thermal macro-modelling in [21]. Other works using TCAD tools to reproduce SC in power MOSFETs show an i_G increase at the instant where i_D rises due to thermal runaway [20]. Under these circumstances, i_G is essentially constituted by displacement current generated from the fast potential decay under the gate, as described in [8].

Fig. 6 compares simulated and measured waveforms for i_D, v_{DS}, v_{GS} and i_G extracted with the following set of conditions: $V_{DC\text{-}LINK}$=800V, $R_{G\text{-}ON/OFF}$=10Ω, T_{SC}=2.5µs, V_{DR}=-5V/+20V and room temperature. Fig. 7 extends the i_G comparison to different $V_{DC\text{-}LINK}$ values (500V, 600V, 700V and 800V). Both Figs. 6 and 7 exhibit a reasonably good match between measurement and simulation. Some discrepancies in i_D are most probably causing slightly larger values simulated i_G. A deeper analysis of T_1, T_2 and T_3, plotted in Fig. 8, shows that during the i_G ramp-time (<100mA), T_1 and T_2 remain under the metal fusion point (933K) and the intrinsic temperature (~1700K), respectively. This is in accordance with the fact that DUT1 does not fail or degrade during a single SC test.

Furthermore, under the same SC test conditions, a sequence of ten SC tests are conducted on the same DUT1, with cooling intervals of 30s between consecutive SC tests. This sequenced test does not show a variation in the measured waveforms, nor the main electrical parameters, including I_G. Fig. 9 exhibits the SiC surface electron tunnelling current density (J_{DT}), perpendicular electric field ($E_\perp$) and lattice temperature (T) profiles at times t_0-t_8 indicated in Fig. 8. As expected, the maximum J_{DT} is found in the area with highest $E_\perp$ under the overlap between N^+ source and PolySi gate. However, Fig. 9 reveals that the channel region along the Pbody is also significantly contributing to i_G as well. This relevant contribution in the channel area obeys to a combination of high $E_\perp$ and high T, where the latter is approximately 100K higher than the T in the area with N+/PolySi overlap. Aside from these two areas, J_{DT} is negligible in the rest of the gate interface. As a final remark, from the 2D nature of the thermionic effect along the gate, it can be concluded that 2D TCAD simulations are expected to offer an improved prediction of i_G current during the SC test compared to 1D TCAD simulations or analytical formulas.

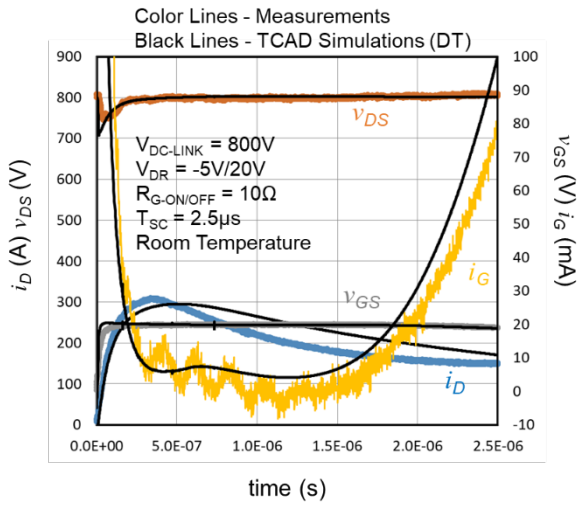

Fig. 6. Measured vs. TCAD simulated waveforms for i_D, v_{DS}, v_{GS} and i_G ($V_{DC-LINK}$=800V) in a 1200V-80mΩ SiC MOSFET. TCAD model includes DT with Φ_B=1.92eV.

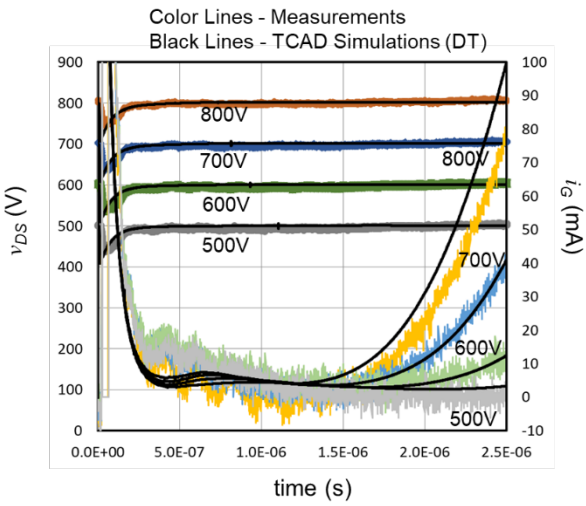

Fig. 7. Measured vs. TCAD simulated waveforms for v_{DS} and i_G ($V_{DC-LINK}$=500, 600, 700, 800V) in a 1200V-80mΩ SiC MOSFET. TCAD model includes DT with Φ_B=1.92eV.

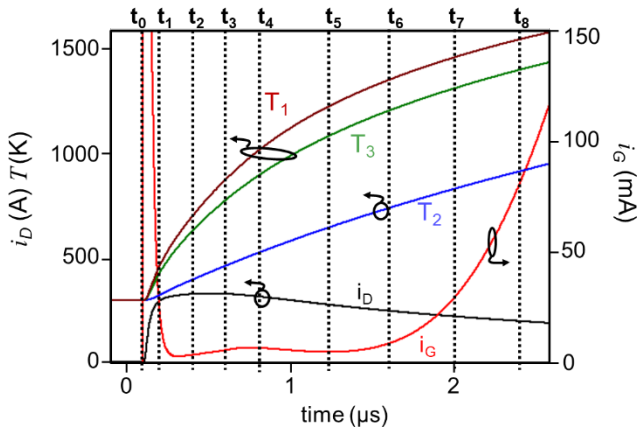

Fig. 8. TCAD simulated waveforms for i_D, i_G, T_1, T_2 and T_3 ($V_{DC-LINK}$=800V). t_0-t_8 times selected for inspection of physical magnitudes are indicated.

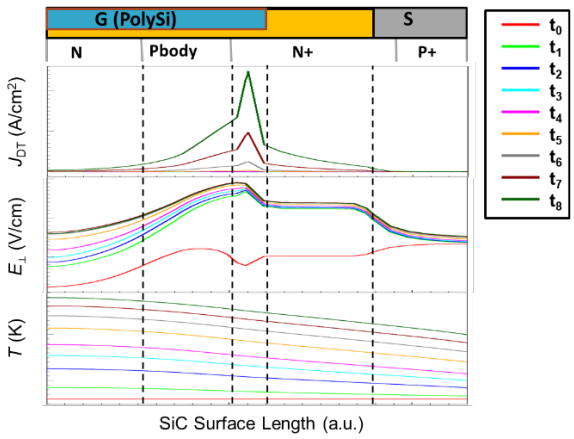

Fig. 9. SiC surface profiles for J_{DT}, $E_\perp$ and T at times t_0-t_8 indicated in Fig. 8. Top cross section of half basic cell shows the surface position with respect to the gate structure.

Summary

This work addresses the use of TCAD models to replicate the thermionic effect through the gate in SiC power MOSFETs, which is one of the most intricate phenomena appearing during the SC test. The NLT and DT models, normally recommended for nanoscale devices, have been evaluated in 1D MOS and 2D power MOSFET structures. By comparing TCAD simulations to experimental results and analytical calculations it is concluded that the DT model exhibits the best TCAD simulation trade-off in terms of accuracy and time consumption. Once the DT model with an averaged and constant Φ_B is established, a deep physical analysis of the dynamic gate current during the SC test is carried out. This analysis reveals that in SiC power MOSFETs there are two main device areas contributing to the i_G by means of the thermionic effect: the N^+/PolySi overlap and channel areas. Finally, the good fit between experiment and simulations invites to the usage of TCAD tools as a preferred tool for a more comprehensive understanding of SC-related effects and for a reliable optimization of SiC power MOSFETs with enhanced SC ruggedness.

Acknowledgements

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