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Investigation of Threshold Voltage Instability and Bipolar Degradation in 3.3 kV Conventional Body Diode and Embedded SBD SiC MOSFET

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Abstract. The 3.3 kV SiC MOSFETs are essential for traction applications, so it is important to investigate the reliability of the recently developed high voltage MOSFETs and power modules as they are believed to be more susceptible to the effects of basal plane dislocations (BPDs). This paper presents measurement results and analysis of bipolar degradation and threshold voltage instability in 3.3 kV SiC MOSFETs having two distinct kinds of integrated diode, conventional body diode and embedded Schottky Barrier Diode (SBD). No bipolar degradation was observed both in MOSFET with conventional body diode and with embedded SBD after accumulated test with 100 hours each of 200%, 400% and 600% rated current stress in the 3rd quadrant of operation. However, the output characteristics show 1% (~0.2 mΩ) and 2% (~0.4 mΩ) increase in on resistance ($R_{DS(on)}$) and 11% (0.23 V) and 5% (0.1 V) increase in threshold voltage (V_{TH}), respectively, after total bipolar degradation test in the case of the MOSFET with conventional body diode and up to 74 hrs of 600% rated current stress in the case of the MOSFET with embedded SBD at 70°C. A rapid large negative V_{TH} shift was obse rved in the MOSFETs with embedded SBD after ~ 74 hrs of 600% rated current stress. After accumulated Bias Temperature Instability (BTI) test at 150°C, the V_{TH} value at 25°C has increased by 9.7% (0.14 V) and 14.5% (0.2 V) for the MOSFET with conventional body diode and with embedded SBD, respectively, while $R_{DS(on)}$ increased by 1mΩ at 25°C and by 5mΩ at 150°C, for both types of MOSFETs.

Introduction

Currently, SiC MOSFETs are used for electric motor drives in applications such as automotive and rail traction where reliability is of paramount importance. While SiC MOSFETs offer several advantages, they are also prone to reliability issues due to increased density of interface traps and BPD defects, reflecting poorer quality of bulk material and SiO_2/SiC interface [1,2,3]. Compared to the 1.2 kV MOSFETs, the 3.3 kV SiC MOSFETs are more prone to the effects of BPDs triggered by recombination energy during body diode conduction due to the three times thicker drift region [4,5]. These primary material issues lead to threshold voltage shift in MOSFETs under gate voltage stress and degradation in body diode conduction characteristics.

The interface states between SiO_2 /SiC acts as charge traps that can capture or release charge carriers. The interfacial states are positively charged when holes are captured which lowers the threshold voltage of the MOSFET and increases the parasitic turn on. Lower threshold voltage leads to reduction of the on-resistance while releasing the electrons from the traps increases the threshold voltage and leads to the increase of the on-resistance. The threshold voltage stability and charge occupation state of the near-interface traps can be studied by a time-dependent high temperature constant bias stress measurement [6,7]. A more than one order of magnitude higher trap density as compared to the silicon devices has been confirmed on the device samples in this investigation by a method of extraction of interface trap density from subthreshold characteristics [8].

The body diode acts as a free-wheeling diode at no additional cost in the MOSFETs. However, it incurs reverse recovery losses, resulting in higher power dissipation and lower switching efficiency. Unlike a conventional body diode, the Schottky Barrier Diode (SBD) has almost no reverse recovery losses, which drastically reduces switching losses and increases efficiency. In addition, MOSFETs

with embedded SBD have lower cut-off voltage due to lower built-in voltage and are free from bipolar degradation due to unipolar conduction [9]. In the previous paper we presented results and analysis of bipolar degradation in 3.3 kV MOSFETs with conventional body diode and embedded SBD applying 50% and 80% of rated current stress with duty cycle 80%, under total time of 100 hrs at constant case temperature of 54°C [9]. This paper presents measurement results and analysis of bipolar degradation in 3.3 kV MOSFETs with conventional body diode and embedded SBD diode at diode current values from 200% to 600% of rated current stress at constant case temperature of 70°C and MOSFET threshold voltage shift at DC gate bias stress of -15 V and +20 V for 48 hours at 150°C. Asymmetrical stress voltage is selected due to the larger vulnerability to oxide failure under negative bias [10].

Experiment and Results

Both in the present and previous study engineering samples of power modules from Mitsubishi with current and voltage rating of 45 A and 3.3 kV were used [9]. Each module contains one SiC MOSFET chip.

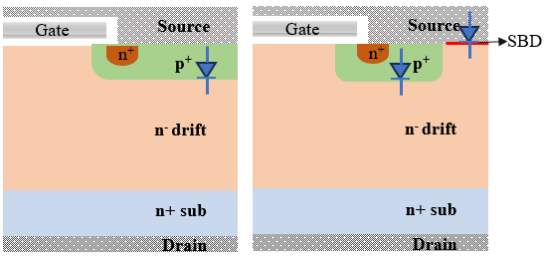

Fig. 1 Schematic SiC MOSFETs with (a) conventional body diode (b) embedded SBD.

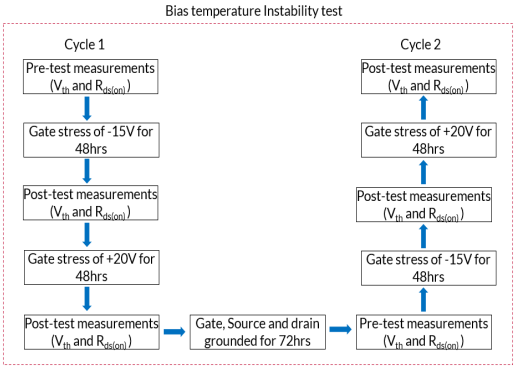

Fig. 2 Process flow of BTI test for V_{TH} instability.

Threshold Voltage Instability Test

Bias Temperature Instability (BTI) tests, V_{TH} instability tests, were performed on 3.3 kV/45 A SiC MOSFETs with two kinds of integrated antiparallel diode (see Fig. 1) using IWATSU CS-5200 curve tracer. The main objective of the BTI test is to monitor changes in V_{TH} caused by sustained positive and negative constant gate bias stress under prolonged time. The datasheet states that the Device Under Test (DUT) can withstand a maximum V_{GS} of ±20 V. To evaluate the negative shift in the transfer curve, a DC voltage of -15 V was first applied to the gate terminal for 48 hours at 150°C. After 48 hours, the voltage was increased in one step to +20 V for the next 48 hours to check for a positive change in the curve at the same temperature. This was the first cycle. The DUT was then grounded for 72 hours, and a pretest was conducted before the start of the second cycle. The transfer and output characteristics were evaluated before and after stressing the gate with different voltages. Figure 2 shows the test procedure that was used throughout the test, and Table 1 contains the test conditions.

Table 1. Stress and measurement conditions for BTI

Condition	Conventional body diode	Embedded SBD
Temperature [°C]	150	150
Gate bias [V]	-15, +20	-15, +20
Output [V]	V_{GS} = 11, 13, 15, 17	V_{GS} = 11, 13, 15, 17
Transfer (before and after stress)	V_{DS} = 10 [V], I_D = 5 [mA]	V_{DS} = 10 [V], I_D = 5 [mA]
Transfer (during stress)	V_{DS} = 10 [V], I_D = 0.5 [mA]	V_{DS} = 10 [V], I_D = 0.5 [mA]

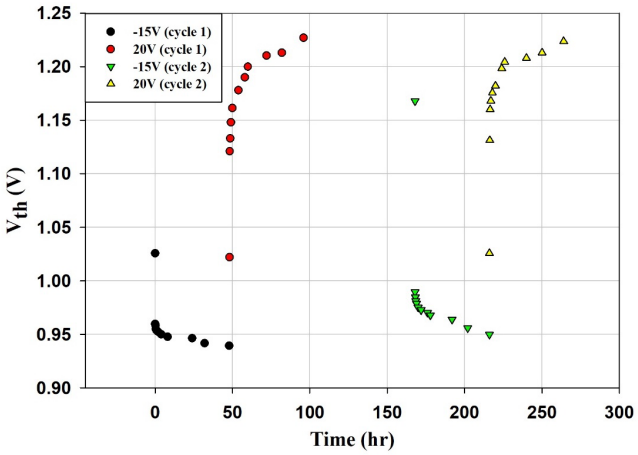

Fig. 3. BTI test process cycle at 150°C (MOSFET with embedded SBD)

Figure 3 shows the BTI test cycle in the case of the MOSFET with embedded SBD and Figure 4 shows results of the BTI measurements for both types of MOSFET on the logarithmic time scale. During a back-and-forth stress- and-measure cycle, the V_{TH} value typically increases linearly with logarithm of the stress-time. The V_{TH} has increased by 0.14 V, or 9.7%, for the MOSFET with conventional body diode and by 0.2 V, or 14.5%, for the MOSFET with embedded SBD. The V_{TH} shift values are lower compared to 0.25 to 0.50 V values for older lower voltage SiC MOSFETs [6]. Also, on-resistance ($R_{DS(on)}$) of the device has increased by 1 mΩ after both cycles at room temperature and by 5 mΩ at 150°C, for both MOSFET with conventional body diode and embedded SBD. The V_{TH} shift is controlled by electron trapping at the near-interface, N_{IT}, (border) traps. The traps are populated by tunnelling process with traps closest to the interface being filled first which results in the logarithmic time dependence. According to studies, traps that are positioned deeper into the oxide from the SiC interface do not change their charge state during either positive or negative bias stress performed in the back-and- forth manner [5]. Hence, suitable test method is required to access traps further away from the interface.

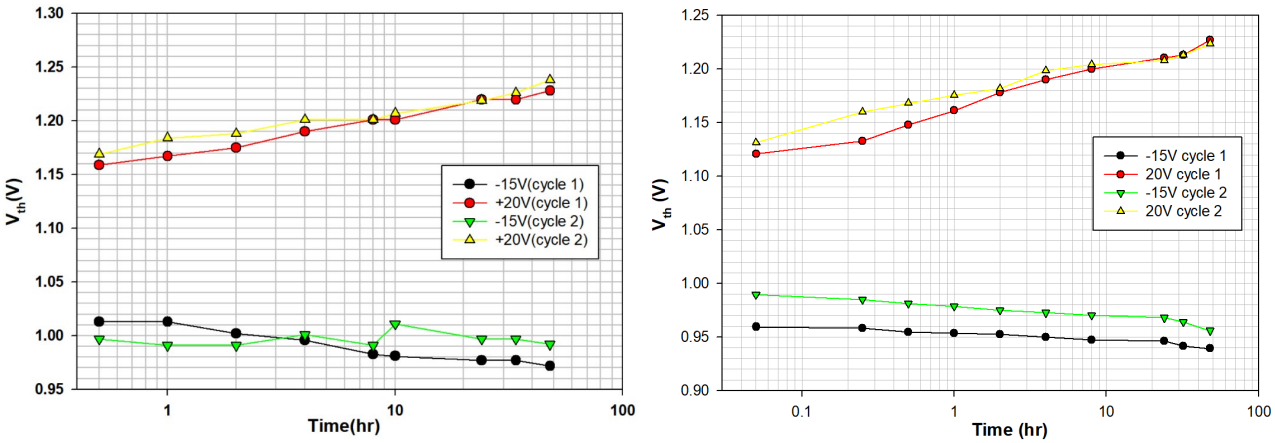

Fig. 4. Threshold voltage variation throughout the process at 150°C in (a) MOSFET with conventional body diode (b) MOSFET with embedded SBD.

Bipolar Degradation Test

In the bipolar degradation test, the SiC MOSFET is subjected to high current stress condition in the 3rd quadrant of operation, while its electrical properties are tracked over an extended time at constant temperature. Bipolar degradation measurements were conducted by applying current stress with 200%, 400%, and 600% of the rated current value and a 40% duty cycle with pulse length of 200 µs over the period of 100 hours at a constant case temperature of 70°C on the same module. The conditions were selected such as to avoid self-heating effects and to be able to maintain constant

temperature during test with forced air cooling. The third quadrant performance of the MOSFET was evaluated before stress using gate bias of -10 V, 0 V, and +17 V at 25°C and 70°C. To assess the bipolar degradation, the MOSFET output and transfer characteristics at 25°C and 70°C before and after stressing were recorded, as well as the diode conduction characteristics over multiple stressing times by switching off the channel completely. Both types of MOSFETs were tested.

Table 2. Stress and measurement conditioned for bipolar degradation test.

Condition	Conventional body diode	Schottky Barrier diode
Temperature [°C]	70	70
Duty cycle [%]	40	40
Rated current [%]	200, 400, 600	200, 400, 600
Body diode	V_G = -10 [V]	V_G = -10 [V]
Output	V_{GS} = 11, 13, 15, 17 [V]	V_{GS} = 11, 13, 15, 17 [V]
Transfer	V_{DS} = 10 [V], I_D = 5 [mA]	V_{DS} = 10 [V], I_D = 5 [mA]

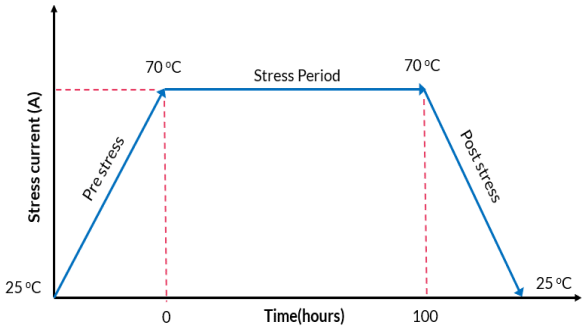

Fig. 5. Process flow for bipolar degradation test

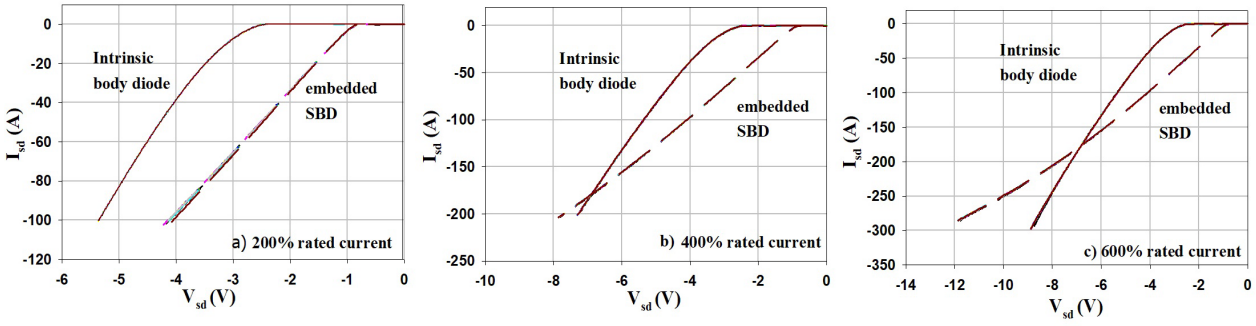

Fig.6. Third quadrant characteristics for MOSFET with conventional body diode and embedded SBD at 70°C a) 200% rated current stress, b) 400% rated current stress, c) 600% rated current stress.

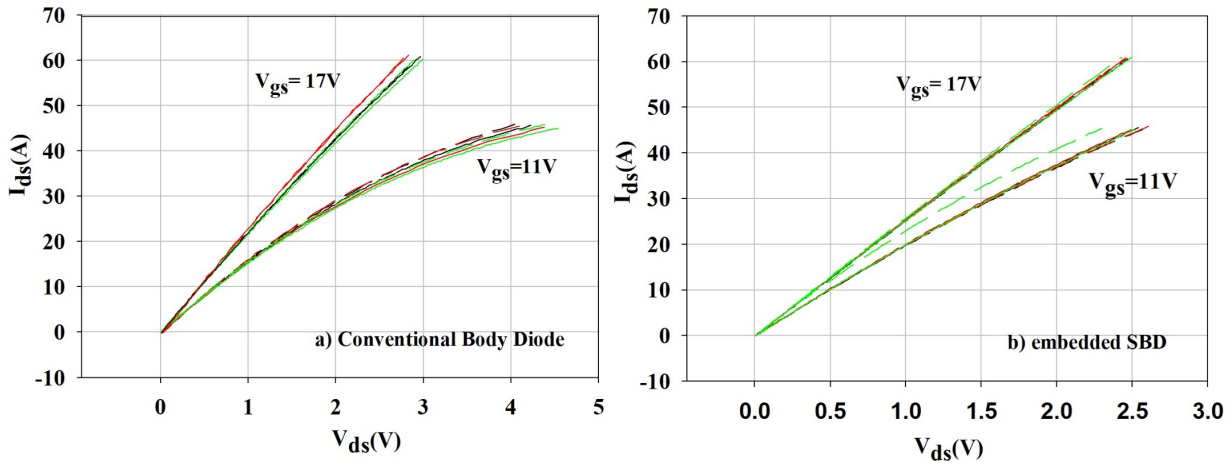

Fig.7. Output characteristics of a MOSFET subjected to current stress of 200%, 400% and 600% rated current for a MOSFET at 70°C with a) conventional body diode and b) embedded SBD.

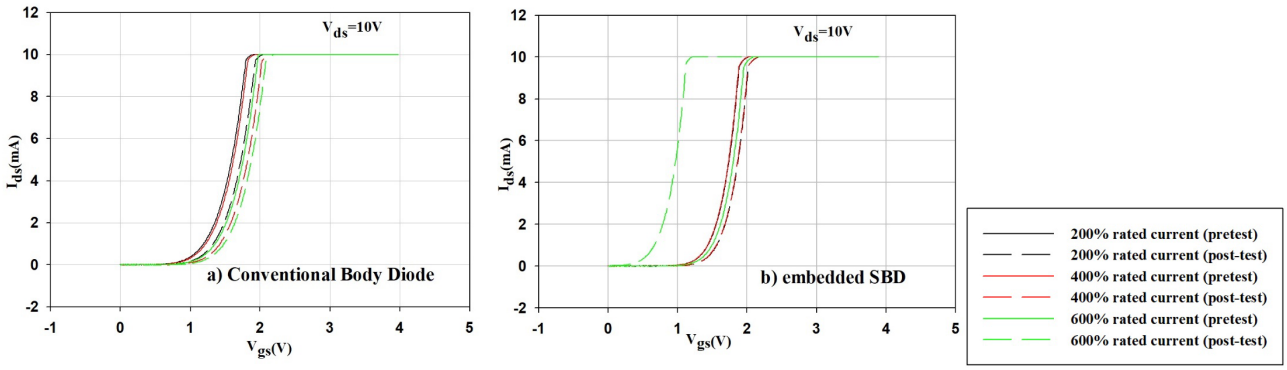

Fig.8. Transfer characteristics of a MOSFET subjected to current stress of 200%, 400% and 600% rated current for a MOSFET at 70°C with a) conventional body diode and b) embedded SBD.

Table 2 gives test conditions for body diode measurements at 8-hour intervals during 100 hours stress time. Figure 6 shows no degradation after 100 hours of current stress of the conventional body diode and embedded SBD. The voltage drop for embedded SBD is higher than for the conventional body diode. The lower voltage drop is due to the bipolar nature of the conventional body diode, which injects both majority and minority carriers during the process. This is observed at more than 200% of rated current stress. The output characteristics demonstrate the $R_{DS(on)}$ increase of around 1% (0.2 mΩ) and the V_{TH} increase by 11% (0.23 V) after 600% of the rated current stress for the MOSFET with conventional body diode. For the MOSFET with embedded SBD, the $R_{DS(on)}$ is increased by 2% (0.4 mΩ) and the V_{TH} increases by 5% (0.1 V) after stress with 600% of rated current until 74 hours of measurement. A large negative shift was observed after 74 hours of stress (see Fig.8.b). The negative shift in V_{TH} was confirmed by measuring another module under the same conditions.

Conclusions

The study of bipolar degradation and threshold voltage instability has been demonstrated in this paper. The bipolar degradation test shows no sign of degradation at current stress of up to 600% rated current in the third quadrant of MOSFET operation. The impact of high current density stress on $R_{DS(on)}$ and V_{TH} differs from the bipolar degradation test results at moderate current densities corresponding to the 50% and 80% of the rated current values [9]. The $R_{DS(on)}$ values increase slightly in both types of MOSFET while the V_{TH} shows an increase of 11% in the MOSFET with conventional body diode after 100 hrs and an increase of 5% in the MOSFET with embedded SBD until 74 hrs under current stress with 600% of rated current. The effects on $R_{DS(on)}$ and V_{TH} may be influenced by the mobile ions present in the oxide [11]. However, a rapid large negative shift in V_{TH} is observed in the devices with embedded SBD after about 74 hrs of current stress with 600% of rated current. The total value of V_{TH} shift observed in the studied devices during BTI test corresponds to a trap density of about 1.4E11 cm^{-2}. This is the trap density that is accessible under applied measurement conditions.

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