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Dynamic On-State Resistance and Threshold-Voltage Instability in SiC MOSFETs

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Abstract. Dynamic on-state resistance has been experimentally observed in all commercially-available SiC MOSFETs studied on the time scale of normal device operation, and can be explained by the presence of dynamic threshold-voltage instability. The magnitude of this dynamic on-state resistance varies from vendor to vendor, but in every case this magnitude generally corresponds to the magnitude of that device's threshold-voltage instability, as described by standard textbook equations—especially in the case of large threshold-voltage instabilities.

Introduction

This work presents very recent results investigating the direct relationship between the well-known dynamic instability of the threshold voltage (V_T) [1, 2], and the newly-revealed dynamic on-state resistance ($R_{DS\text{-}ON}$) [2, 3] in commercially-available SiC MOSFETs. Both planar-channel (Vendor M) and trench-geometry (Vendor T)—as defined in [2-4]—SiC power MOSFETs were characterized in terms of both dynamic $R_{DS\text{-}ON}$ and, independently, V_T instability under similar gate-switching conditions comparable to standard power-switching operations, details of which are given elsewhere [2, 3]. The V_T instability data was then applied to standard semiconductor device equations relating V_T to the channel resistance, and the channel resistance in turn to the total resistance, resulting in a calculated expected change in $R_{DS\text{-}ON}$ due to a change in V_T, which was then compared to the actual in-situ measured change in $R_{DS\text{-}ON}$.

The specific channel resistance is given as

$$R_{CH} \cong \frac{L_{CH} \cdot Pitch}{\mu_{ch} \cdot C_{OX} \cdot (V_{GS} - V_T)}. \quad (1)$$

wherein this specific channel resistance is a function of the channel length, cell pitch, inversion channel mobility (μ_{ch}), gate-oxide capacitance, and the difference between the applied gate-to-source voltage, V_{GS}, and V_T. The specific on-state resistance is the sum of all component resistances, normalized by the active area of the device.

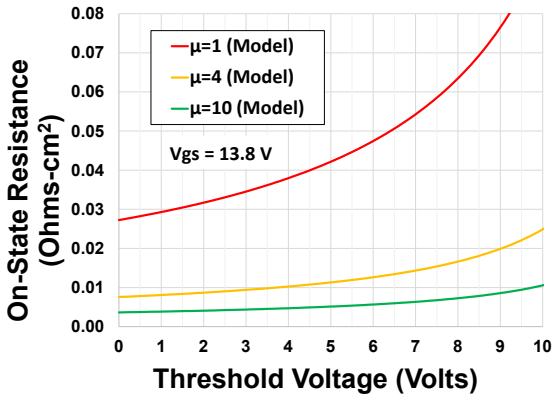

Fig. 1. Theoretical curve for $R_{DS\text{-}ON}$ versus V_T for a SiC MOSFET, as a function of channel mobility.

Fig. 1 shows the theoretical curve for $R_{DS\text{-}ON}$ versus threshold voltage for a generic SiC MOSFET, as a function of μ_{ch}, for the same V_{GS} that was applied when measuring $R_{DS\text{-}ON}$ directly. Lower channel mobilities result in larger channel resistances, thus affecting the total resistance to a greater degree. In addition, Fig.1 shows that not only does total $R_{DS\text{-}ON}$ increase with decreasing channel mobility, but more importantly, the slopes of the curves increase as well, resulting in larger changes in $R_{DS\text{-}ON}$ for the same change in V_T —and these slopes increase even more for larger values of V_T.

Results and Discussion

V_T hysteresis is a fundamental phenomenon occurring in all SiC MOSFETs. When subject to an alternating gate bias, near-interfacial oxide traps are alternately charged and neutralized, resulting in non-permanent drifts of V_T [1]. Although such dynamic V_T does not represent device degradation, if large enough, it may affect device (and therefore circuit) performance.

The magnitude of this dynamic variation in V_T depends on several factors, in particular the magnitude and polarity of the applied gate bias, and perhaps most importantly the duration in time that such bias is applied [1]. Naturally, the longer the applied bias, the greater the effect, although even gate biases applied on the time scales of normal device operation can result in noticeable V_T instabilities—but only if measured on a similar or faster time scale. Faster V_T measurements reveal more of the V_T instability that is present, but even the fastest measurements do not show the full extent of the V_T drift experienced by the device—although the effect of such drift is likely captured more readily by in-situ measurements of changes in the $R_{DS\text{-}ON}$ [2, 3].

Fig. 2 shows the measured V_T instability of a previously unstressed DMOSFET from Vendor M, both at 25 and 125 °C. Both the low side (measured following the application of a negative gate bias for the indicated hysteresis stress interval time) and high side (measured following the application of a positive gate bias) of each V_T hysteresis envelope is plotted. As is commonly observed, V_T decreases with increasing temperature, and its V_T hysteresis also decreases [1]. Nonetheless, significant V_T instabilities are observed on the time scale of normal device operation. For example, at room temperature, the Vendor M device shows a V_T instability of 2.9 V for a hysteresis stress interval time of 50 μs, which corresponds to an operating frequency of 10 kHz with a 50% duty cycle. At 125 °C, the V_T instability decreases to 1.7 V under the same bias-switching conditions.

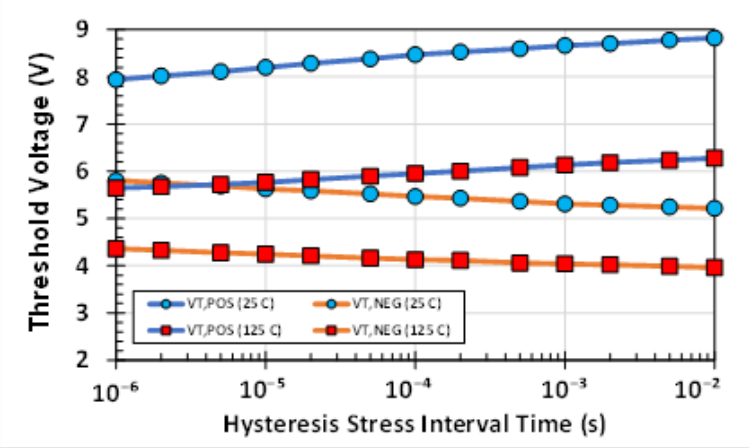

Fig. 2. V_T hysteresis data of a Vendor M planar SiC DMOSFET, for temperatures of 25 and 125 °C. Similar line colors indicate the same bias polarity of the hysteresis stress, and similar symbol shapes and colors indicate the same stress-and-measurement temperature.

Dynamic $R_{DS\text{-}ON}$ was characterized (independently of V_T instability) for both planar and trench SiC MOSFETs, up to 100 kHz and up to 125 °C, under conditions comparable to standard power-switching operations. A standard gate driver with V_{GS} of +15 and −5 V was used to supply the on-state and off-state voltages of the MOSFETs, respectively. The change in on-state resistance, $\Delta R_{DS\text{-}ON}$, is defined as the difference between $R_{DS\text{-}ON}$ measured at the beginning of each on-state interval and $R_{DS\text{-}ON}$ measured at the end of the on-state interval immediately before the turn-off transition. The V_T instability data, such as that from Fig. 2, was then applied to (1) relating V_T to the channel resistance,

and the channel resistance in turn to the total resistance, resulting in a calculated expected change in $R_{DS\text{-}ON}$ due to a change in V_T — which was then compared to the actual in-situ measured change in $R_{DS\text{-}ON}$.

This is seen in Figs. 3 and 4, which compare the calculated change in on-state resistance ($\Delta R_{DS\text{-}ON}$) —for different assumed values of μ_{ch} —based on the V_T instabilities (ΔV_T) shown in Fig. 2, with the actual in-situ measured values of $\Delta R_{DS\text{-}ON}$ (labeled "Experiment")—at 25 °C and 125 °C, respectively. The magnitude of the dynamic $R_{DS\text{-}ON}$ varies between 56% (at 10 kHz) and 42% (at 100 kHz) for the 25 °C case, whereas it is much smaller for the 125 °C case, varying between just 18% and 14%. This is unsurprising, given that the curves in Fig. 1 are much flatter for lower values of V_T (and which naturally vary less with smaller changes in V_T). Even so, a good fit to the data also requires that μ_{ch} increase with increasing temperature (μ_{ch} = 1 cm^2/V·s at 25 °C; μ_{ch} = 10 cm^2/V·s at 125 °C), consistent with what is reported on its data sheet.

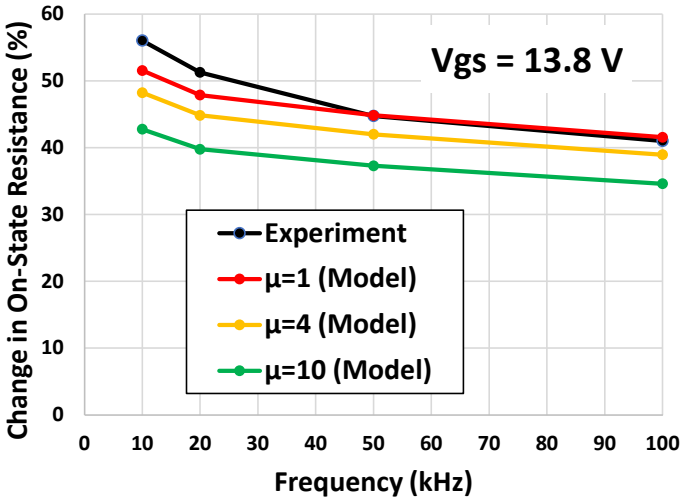

Fig. 3. Results for Vendor M planar SiC DMOSFET at 25 °C. Comparison of experimentally measured change in $R_{DS\text{-}ON}$, as a function of switching frequency, with calculated changes in $R_{DS\text{-}ON}$ —applying measured values of V_T instability (for V_T hysteresis measurements with hysteresis stress interval times corresponding to the switching frequency) to the theoretical curves from Fig. 1, as a function of assumed channel mobility.

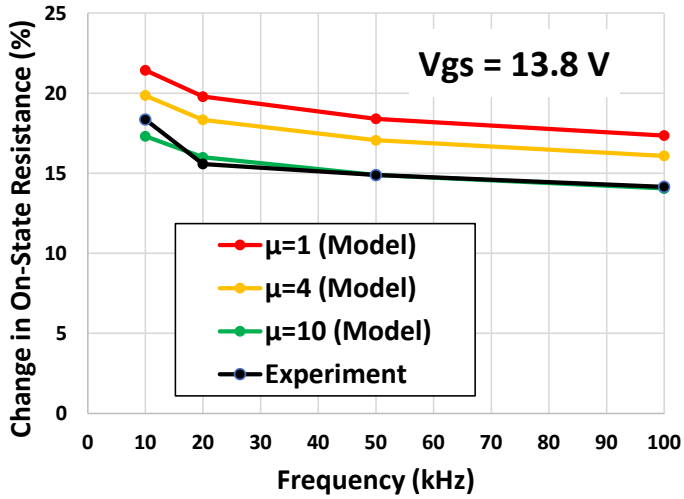

Fig. 4. Results for Vendor M planar SiC DMOSFET at 125 °C. Comparison of experimentally measured change in $R_{DS\text{-}ON}$ with calculated changes in $R_{DS\text{-}ON}$ —again applying the theoretical curves from Fig. 1 as a function of assumed channel mobility.

Fig. 5 compares the V_T instability of the same Vendor M device from Fig. 2 with a trench-geometry Vendor T device—both at 25 °C. The Vendor T device has a much, much smaller V_T instability. Fig. 6 plots the dynamic $R_{DS\text{-}ON}$ of a Vendor T device as a function of gate- switching stress (GSS) cycles [3, 4], again comparing actual in-situ results ("Experiment") with calculated values based on measured V_T instability—all at a switching frequency of 10 kHZ (the GSS frequency was about 1 MHz). It is interesting to observe that before any increase in V_T instability due to GSS-induced degradation (due to negative bias overstress effects [2, 4]), there is a poor match between the measured $\Delta R_{DS\text{-}ON}$ of about 22% and a calculated value well below 5%. As degradation occurs and ΔV_T increases, the experimental and calculated values of $\Delta R_{DS\text{-}ON}$ converge. For the very large V_T instabilities measured when GSS cycles exceed 3×10^{12}, the calculated $\Delta R_{DS\text{-}ON}$ exceeds 160%.

In general, the standard textbook equations relating $R_{DS\text{-}ON}$ and V_T were found to be consistent with our experimental results. The main difficulties appeared when measuring dynamic $R_{DS\text{-}ON}$ with small V_T instabilities. In these cases, the measured values of dynamic $R_{DS\text{-}ON}$ were much larger than what might reasonably be expected based on the V_T hysteresis measurements. One possible explanation is that even the fastest *I-V* measurements do not observe all the V_T instability that actually occurs [1, 3], yet is present and contributes to the dynamic $R_{DS\text{-}ON}$ that is measured in-situ. On the other hand, large V_T instabilities, which would predict large variations in $R_{DS\text{-}ON}$, were confirmed by experiment. Expected variations in $R_{DS\text{-}ON}$ with temperature were generally confirmed as well. Regardless of the cause of the large dynamic variability in V_T, a large V_T instability of more than a few volts can result in the presence of a significant dynamic variability of $R_{DS\text{-}ON}$. If such dynamic $R_{DS\text{-}ON}$ effects are large enough, they may result in reduced device reliability due to an unanticipated increase in power dissipation [2, 3].

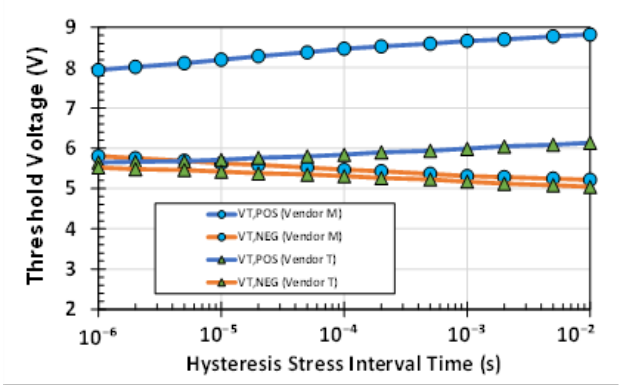

Fig. 5. V_T hysteresis data at 25 °C for a Vendor M planar SiC DMOSFET, and for a Vendor T trench-geometry SiC MOSFET. Similar line colors indicate the same bias polarity of the hysteresis stress, and in this case similar symbol shapes and colors indicate the same device.

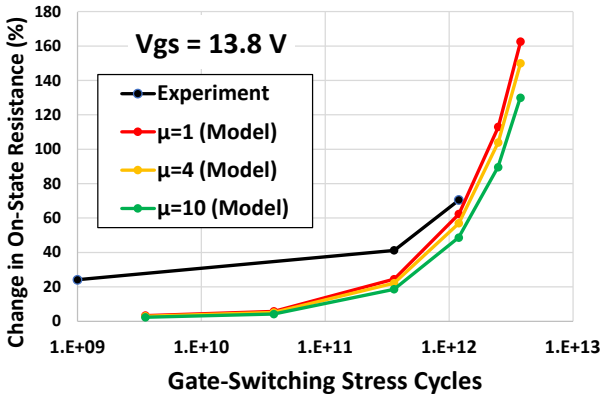

Fig. 6. Results for Vendor T trench-geometry SiC MOSFET at 25 °C. Comparison of experimentally measured change in $R_{DS\text{-}ON}$, as a function of total GSS cycles (with constant switching frequency of 10 kHz), with calculated changes in $R_{DS\text{-}ON}$ —applying measured values of V_T instability (as a function of total GSS cycles with a fixed hysteresis interval time of 100 μs) to the theoretical curves from Fig. 1, as a function of assumed channel mobility.

Summary

We have observed dynamic $R_{DS,ON}$ effects in power SiC MOSFETs with large threshold-voltage instabilities under normal gate-switching conditions, thus confirming the theoretical relationship between $R_{DS,ON}$ and V_T. However, in cases where the measured V_T hysteresis was small (e.g., the unstressed Vendor T trench-geometry MOSFET at room temperature), the measured dynamic $R_{DS,ON}$ was much larger than the theoretical value based on the measured dynamic V_T. One explanation for this discrepancy could be that even the fastest *I-V* measurements were still not able to capture all the V_T instability that occurred—in contrast to the in-situ dynamic $R_{DS,ON}$ measurements.

Regardless of the cause of the large dynamic variability in V_T, a large V_T instability of more than a few volts (when measured using fast *I-V*) can result in the presence of a significant dynamic variability of $R_{DS,ON}$.

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