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Study of the Bias Driven Threshold Voltage Drift of 1.2 kV SiC MOSFETs in Power Cycling and High Temperature Gate Bias Tests

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Abstract. Threshold voltage instability remains a challenging aspect for metal-oxide semiconductor-field-effect-transistors (MOSFETs) made from silicon carbide (SiC). SiC MOSFETs from two manufacturers, with planar and trench gate structure respectively, have been tested under different test procedures, including power cycling and high temperature gate bias tests. The standard power cycling test setup has been modified to enable an in situ threshold voltage read-out procedure with the hysteresis method. The recorded threshold voltage drift has been compared with results from high temperature gate bias tests applying a simple power law fit, with the intention to predict the drift in power cycling tests. For the group with trench MOSFETs comparable results between power cycling and gate stress tests have been achieved.

Introduction

Although SiC MOSFETs successfully entered the market of semiconductor power devices, there are still aspects related to reliability and robustness which must be addressed. One of those topics is the threshold voltage instability [1], resulting from a wider band gap of SiC compared to Si and a high density of trap states at the SiC/SiO_2 interface (D_{it}). Both aspects lead to phenomena such as more pronounced bias-temperature instability (BTI) and threshold voltage hysteresis ($V_{GS(Th)Hyst}$) [2]. Whereas the $V_{GS(Th)}$-hysteresis itself is referred to be harmless [3] for the switching behavior and the application, the BTI might have a significant impact on the on-state resistance ($R_{DS(on)}$) especially for lower voltage class devices.

The BTI-driven threshold voltage drift can be addressed with a high temperature gate bias (HTGB) test. During a power cycling test (PCT) a longer lasting positive and/or negative gate voltage with application levels is applied to the device - similar as for a HTGB. Depending on the selected test procedure in the PCT, either a constant negative gate bias or a very low frequency AC gate voltage can be applied to the specimens [4]. A typical end-of-life (EOL) criterion in power cycling tests is an increase of the forward voltage drop by more than $5\,\%$, which might be affected by a potential $V_{GS(Th)}$-drift during the test. Hence, the lifetime in PCTs might be distorted by this drift.

Test Procedure and Specimens

To analyze the $V_{GS(Th)}$-drift during the power cycling test, a standard setup has been modified, to enable an in situ threshold voltage measurement, without removing specimens from the test bench. The PCT setup for one single specimen is shown in Fig. 1 together with the read-out procedure for the virtual junction temperature (T_{vj}) and the threshold voltage according to the hysteresis method in alignment to the JEDEC standard JEP 184 and [2]. A detailed description of the setup can be found in [5]. Commercially available off-the-shelf $1.2\,\mathrm{kV}$ SiC MOSFETs in TO-247-3 package from two manufacturers have been tested under similar test conditions, which are summarized in Table 1. The rated on-state resistance $R_{DS(on)}$ is $75\,\mathrm{m\Omega}$ for the devices with a planar gate structure (PGM group)

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Table 1: Test conditions of the PCT in MOSFET-mode [9] for 1.2 kV SiC MOSFETs

Test group	I_{Load} [A]	ΔT_{vj} [K]	$T_{vj(min)}$ [K] ([°C])	T_{inlet} [K] ([°C])	t_{on} [s]	t_{off} [s]	$V_{GS(on)}$ [V]	$V_{GS(off)}$ [V]
PGM (planar gate)	21.8	55-68	~358 (85)	353 (80)	2.0	4.0	20	-10*
TGM (trench gate)	19.2	55-62	~358 (85)	353 (80)				

* applied to suppress the MOS-channel completely

and 80 mΩ for the trench MOSFETs (TGM group), which enables comparable test conditions in the power cycling test. Both groups contained 15 specimens.

MOSFET-mode [9] is the recommended procedure for power cycling tests on SiC MOSFETs. Devices under test switch between on-state (t_{on}) where a DC load current I_{Load} is driven through the specimens and off-state (t_{off}) where T_{vj} is being measured at low sense current. During the on-state, a high positive V_{GS} is being applied across the devices under test whereas a negative gate voltage is required in the off-state to apply the $V_{SD}(T)$-method [4, 10]. To ensure a precise T_{vj} calculation, the MOS-channel must be suppressed completely with a sufficiently low negative gate bias. For some manufacturers this can be even below $V_{GS} = -10$ V [12] exceeding the data sheet limits. Although there is a sufficient gap to the dielectric breakdown, the low negative gate voltage will have a significant impact on the interface states [7], the $V_{GS(Th)}$-drift due to the BTI effect and might have a significant influence on the $R_{DS(on)}$, which is an important EOL-criterion in power cycling tests. Separated from each other, both gate bias polarities can provoke the BTI effect in different directions but they might result in a superimposed drift after the PCT, containing a share of positive (PBTI) and negative BTI (NBTI). Due to low number of switching cycles, the AC-driven $V_{GS(Th)}$-drift [6] was not considered.

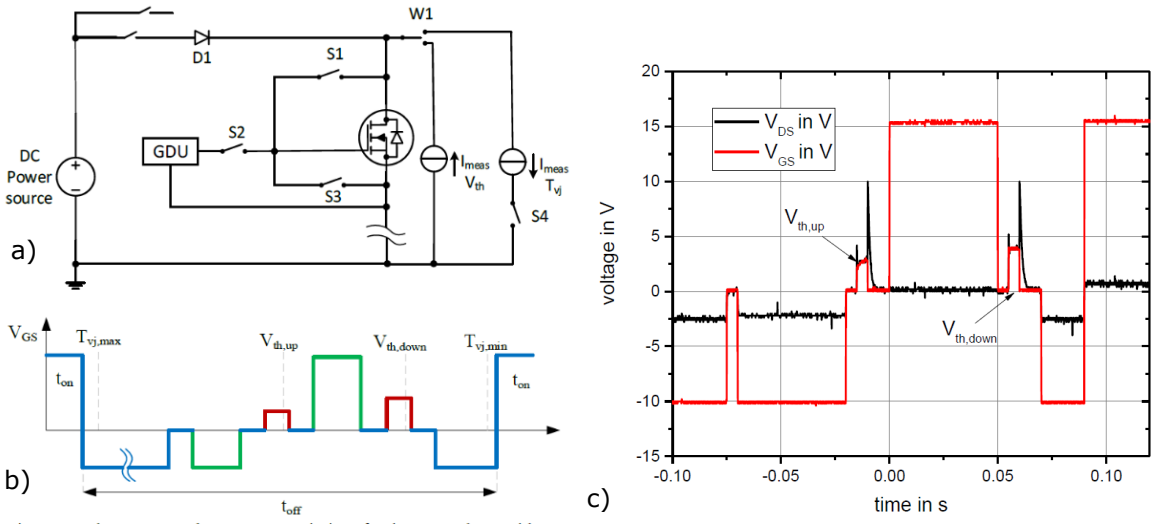

Fig. 1: a) Simplified circuit diagram for the determination of $V_{GS(Th)}$ and T_{vj} in the PCT; b) pulse pattern of gate voltage and measurement timings of T_{vj} and $V_{GS(Th)}$; $V_{GS(Th)}$ read-out in alignment to the hysteresis method from the JEDEC standard JEP 184 and [2] shortly before $T_{vj(min)}$ measurement; c) sample measurement on a SiC MOSFET during the PCT; delay between load-current turn-off event and $T_{vj(max)}$ measurement was 200 µs; detailed description of the test setup in [5].

In parallel to the power cycling tests, three gate stress tests with positive, negative, and periodically alternating stress voltage have been performed, including an in situ $V_{GS(Th)}$ read-out according to the triple sense method in alignment to the JEDEC standard JEP 184 and [2], with the intention to predict the $V_{GS(Th)}$-drift and to separate BTI effects from thermomechanical wear induced V_{DS}-drift

in PCTs. In every HTGB test 6 pristine specimens for each manufacturer have been stressed at high case temperature ($T_C = 150\,°\text{C}$) under DC gate bias. To ensure comparability between power cycling and gate stress tests, the same gate voltage levels have been selected as in the PCT, including $V_{GS} = 20\,\text{V}$ for the PBTI and $V_{GS} = -10\,\text{V}$ for the NBTI test. $V_{GS(Th)}$ has been recorded in situ with a logarithmically increasing time intervals for a total stress time of $t_{stress} = 500\,\text{h}$ at high temperature to avoid recovery effects during cooling phases [7]. In the third HTGB test (Alt-BTI) the stress bias has been alternated periodically between positive and negative gate voltage to investigate the interaction of PBTI and NBTI effects on the same devices under test. Therefore, the gate voltage has not been switched with an AC signal but basing on a logarithmically increasing stress time, containing a $V_{GS(Th)}$ read-out after every stress period. The total test time was set to $t_{stress} = 1000\,\text{h}$ containing $500\,\text{h}$ PBTI and $500\,\text{h}$ NBTI stress. With this procedure it was possible to investigate potential recovery effects, which are related to the opposite gate bias and compare the results of the separated PBTI and NBTI portions with the continuous DC tests. For a reasonable comparison of the test results the threshold voltage drift ($\Delta V_{GS(Th)}$) was fit with a power law according to Eq. 1:

$$\Delta V_{GS(Th)} = A_0 * t_{test}^{b} \tag{1}$$

with the scale factor A_0, the power law exponent b and the test time t_{test}.

Threshold Voltage Drift Driven by Different Test Conditions

Temperature Dependency of the Threshold Voltage. Prior to the reliability tests, the temperature dependency of the threshold voltage has been recorded for both manufacturers. As shown in Fig. 2, not only the slopes of the Up and Down values are different, but they vary between both groups as well. Within the recorded temperature range $V_{GS(Th)}$ shows a linear dependency. Although the slope of $V_{GS(Th)Down}$ has a satisfying resolution for both groups, this parameter is not suitable for the junction temperature calculation due to the threshold voltage instability and hysteresis phenomena [2, 7].

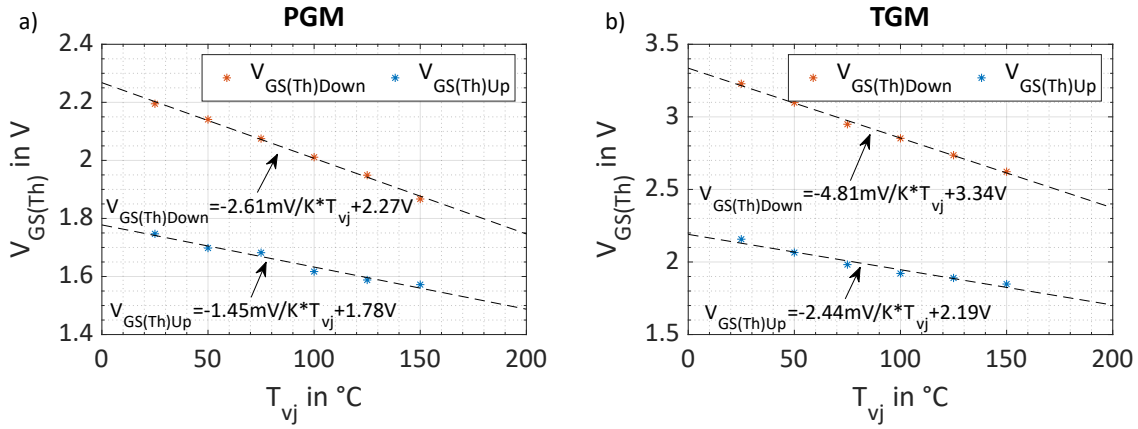

Fig. 2: $V_{GS(Th)}$ vs. T_{vj} for a) planar and b) trench MOSFET; $V_{GS(Th)}$ measured with the triple sense method according to the JEP 184 standard, including records of the $V_{GS(Th)Up}$ and $V_{GS(Th)Down}$ in the gated-diode configuration ($V_{GS} = V_{DS}$, $I_D = 1\,\text{mA}$); the acquisition delay time set to $t_{aq(del)} = 1s$; a preconditioning prior to every $V_{GS(Th)}$ measurement has been applied to specimens with a gate voltage of $V_{GS} = \pm 20\,\text{V}$ for a fixed pulse time of $t_{precon} = 100\,\text{ms}$

Threshold Voltage Drift in the PCT. Representative PCT results from each group are shown in Fig. 3, including trends of forward voltage drop (V_{DS}), thermal resistance ($R_{th(jhs)}$) and junction temperature swing (ΔT_{vj}) in a) and b). For the PGM group only 6 out of 15 specimens reached the EOL condition due to a V_{DS}-increase by more than $5\,\%$ from the steady state value and 9 devices did not fail until the test end after $450,000$ cycles. V_{DS}-increase is a typical EOL-criterion for semiconductor power devices in TO-packages in power cycling tests and indicates either bond-wire lift-off or heel crack as failure

mechanism. The shown planar SiC MOSFET reached end-of-life after more than $367,000$ cycles, whereas the first failure occurred after approximately $240,000$ cycles (not shown). This deviation results from different individual temperature swing in the test, as shown in Table 1. In contrast to the PGM group, all trench SiC MOSFETs reached the end-of-life in the PCT. As expected, the EOL-condition remained the same and all specimens from the TGM group failed due to a V_{DS}-increase.

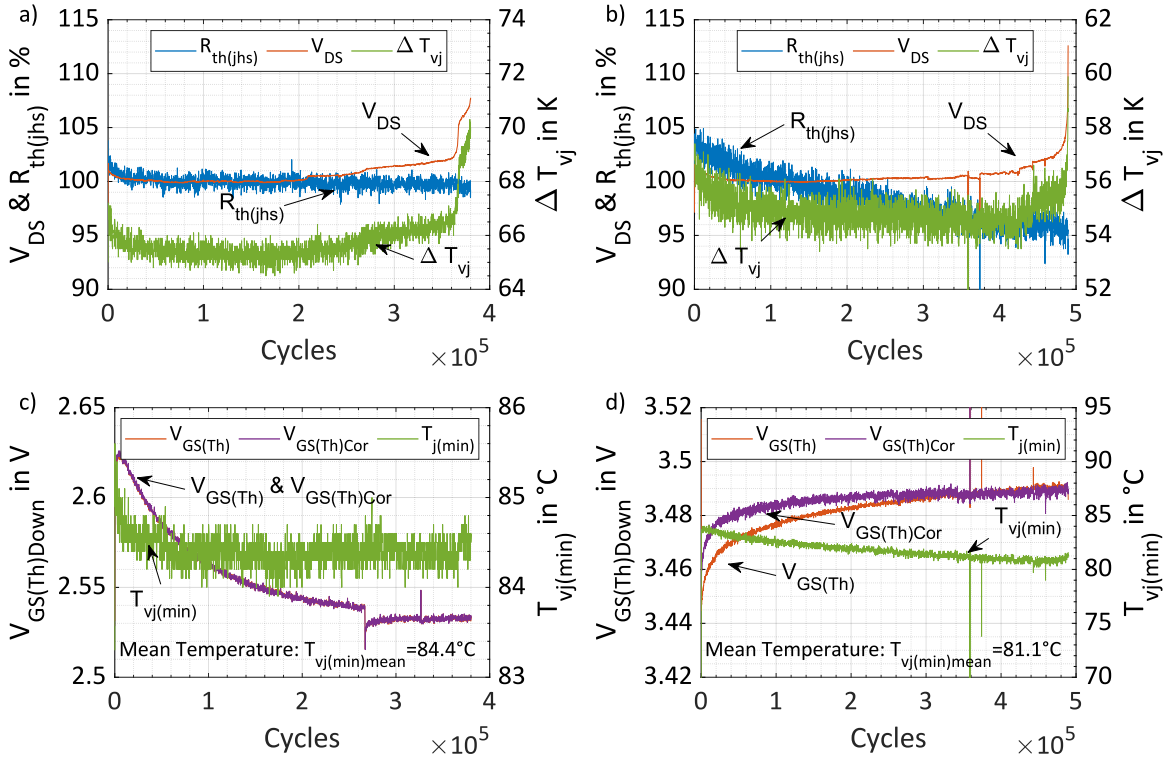

Fig. 3: $R_{th(jhs)}$, V_{DS} and ΔT_{vj} in a) planar and b) trench MOSFET together with $V_{GS(Th)Down}$ and $T_{vj(min)}$ in c) and d); planar MOSFET reached EOL after approx. $373,000$ cycles as shown in a); trench MOSFET reached EOL after approx. $487,000$ cycles as shown in b); slight decrease of $T_{vj(min)}$ for the trench device in d) affecting $V_{GS(Th)Down}$ read-out; measured and temperature-corrected $V_{GS(Th)Down}$ value shown in c) and d); test of planar device restarted around $267,000$ cycles in c)

An opposing trend has been found for these two groups regarding the threshold voltage, as shown in Fig. 3 c) and d). The planar MOSFET showed a small $V_{GS(Th)}$ increase within the first $20,000$ cycles, partly resulting from the slight decline of the lower junction temperature ($T_{vj(min)}$), which was recorded shortly after the $V_{GS(Th)Down}$ measurement as shown in Fig. 1 b). After this peak the threshold voltage dropped for the specimen of the PGM group as depicted in Fig. 3 c). An interruption of the test occurred at approximately $267,000$ cycles, where the devices under test remained biased with a negative gate voltage ($V_{GS} = -10\,\mathrm{V}$) for approximately $27.3\,\mathrm{h}$, leading to an additional $V_{GS(Th)}$ drop due to the NBTI effect and finally reaching a saturation of the drift. The $V_{GS(Th)}$-curve for the trench specimen was affected by a more pronounced decrease of $T_{vj(min)}$, beginning from test start almost until test end. Therefore, the measured $V_{GS(Th)Down}$ values have been temperature corrected with the extracted slope ($-4.8\,\mathrm{mV\,K^{-1}}$) from Fig. 2 b) and drawn together with the raw data in Fig. 3 d). A mean temperature of $T_{vj(min)} = 81.1\,^{\circ}\mathrm{C}$ was calculated from roughly $425,000$ cycles until test end and was applied as targeted temperature for the data correction, because in this period T_{vj} reached the static value. Especially within the first half of the test a significant deviation between measured and corrected $V_{GS(Th)}$-values is clearly visible. The data correction was applied to the specimens from the PGM group as well, but the deviation remained negligible due to the minor decrease of $T_{vj(min)}$ (below $2\,\mathrm{K}$) within the first $100,000$ cycles and the lower slope ($-2.6\,\mathrm{mV\,K^{-1}}$). Therefore, both $V_{GS(Th)}$ curves are almost on top of each other in Fig. 3 c).

To identify a general $V_{GS(Th)}$ trend in the power cycling test, the $V_{GS(Th)Down}$-drift was extracted and is shown in Fig. 4 for both groups. The measured threshold voltage has been temperature-corrected for all devices under test due to the non-stable $T_{vj(min)}$ during the PCT with the parameters shown in Fig. 2. Instead of the switching cycles, the $V_{GS(Th)Down}$-drift was plotted vs. the test time in PCT, calculated according to the test period of $T_{PCT} = 6\,\mathrm{s}$. The ratio between on- and off-state was $1:2$. This condition led to a two times longer time, when negative gate voltage ($V_{GS(off)} = -10\,\mathrm{V}$) was applied to the devices under test, then positive gate voltage ($V_{GS(on)} = 20\,\mathrm{V}$). Occasional interruptions of the $V_{GS(Th)}$ read-out occurred during the test but this had no influence on the results.

Obviously, the specimens with planar gate structure had a non-uniform behavior during the test. Three out of fifteen specimens showed a significant drop between $2\,\mathrm{h}$ and $200\,\mathrm{h}$, whereas $V_{GS(Th)}$ decreased with varying intensity beginning from $30\,\mathrm{h}$ until EOL for the remaining specimens after an initial growth. However, no correlation has been found between these devices, in terms of common test parameters such as temperature swing, virtual junction temperature or position in the setup (graphs not shown here). A contrary behavior has been observed for the TGM group where the threshold voltage increased for all fifteen devices under test in the same manner, as shown in Fig. 4 b). Therefore, it was possible to extrapolate the fit parameters for the MOSFETs with trench gate structure. For the extrapolation only values after $2\,\mathrm{h}$ have been considered.

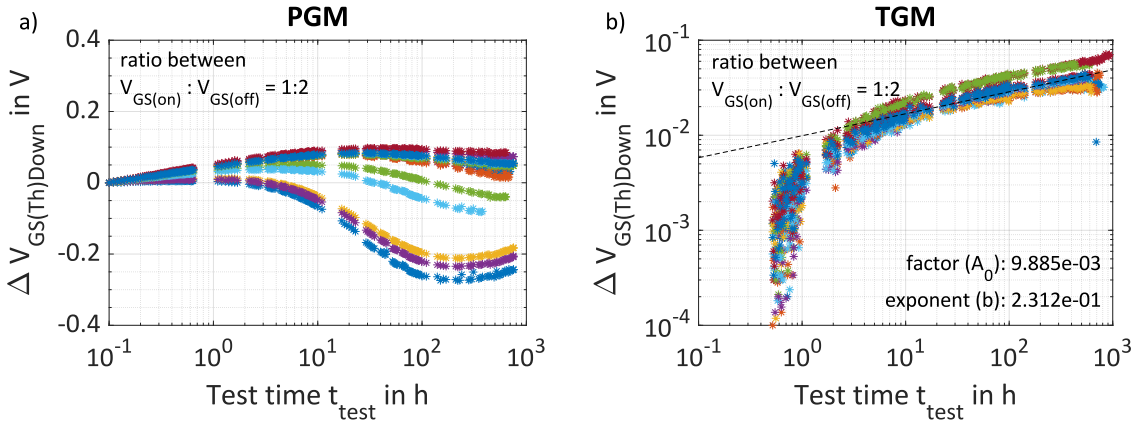

Fig. 4: $V_{GS(Th)}$ drift for a) planar and b) trench MOSFETs during the PCT in MOSFET-mode with a AC gate signal corresponding to the t_{on}/t_{off} time; $V_{GS(on)} = 20\,\mathrm{V}$ and $V_{GS(off)} = -10\,\mathrm{V}$ with a ratio of $1:2$; $V_{GS(Th)}$ read-out in situ at $T_{vj(min)}$ (approx. $85\,^{\circ}\mathrm{C}$) with the hysteresis method; preconditioning for $100\,\mathrm{ms}$ at operating gate voltage; fit with power law as dashed line with factor A_0 and power law exponent b; temperature corrected data with slopes from Fig. 2

Threshold Voltage Drift in the HTGB. The results of DC HTGB tests are shown in Fig. 5 and Fig. 6 containing both groups, for positive and negative gate voltage respectively. Based on previously published results an increasing $V_{GS(Th)}$ was expected in the test with positive gate voltage ($V_{GS} = 20\,\mathrm{V}$) [2, 8, 11]. However, this behavior was observed for the TGM group only, whereas $V_{GS(Th)}$ dropped significantly for the specimens with planar gate structure. Increasing $V_{GS(Th)}$ is typically caused by charging effects of interface traps and/or oxide charges due to positive gate bias [1]. Decreasing $V_{GS(Th)}$ is a typical indicator for mobile oxide charges, such as sodium or potassium ions, which is significantly enhanced by high temperature [2].

The drift in the NBTI test was less pronounced than in the PBTI test for both groups, potentially resulting from the lower absolute stress voltage level and opposite polarity. All specimens of the TGM-group showed a slight $V_{GS(Th)}$ decrease in the NBTI test and the drift remained below $50\,\mathrm{mV}$ after $500\,\mathrm{h}$. An opposing trend has been found for the MOSFETs with planar gate structure. Within the first $10\,\mathrm{h}$ the threshold voltage remained almost stable, below the initial value, but started to increase subsequently with test time. This behavior was probably caused by the same mobile charges, which

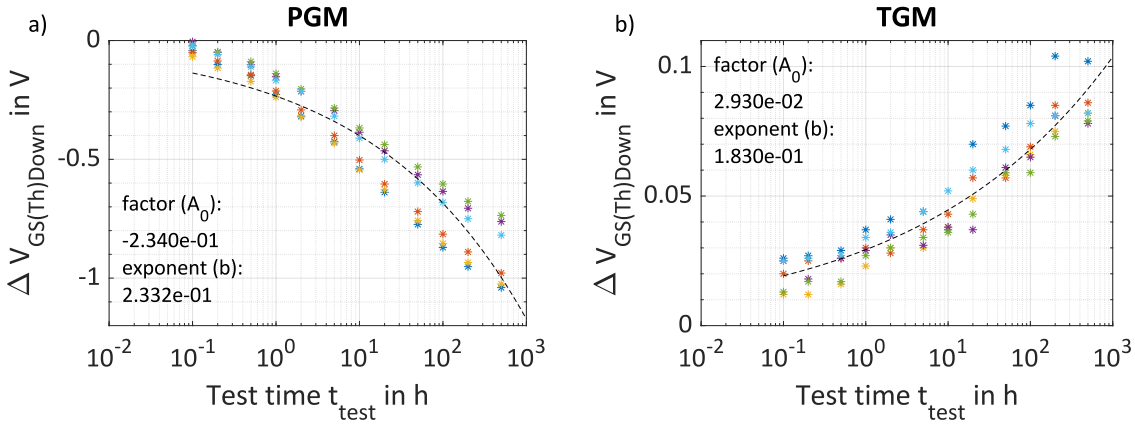

Fig. 5: $V_{GS(Th)}$ drift for a) planar MOSFETs and b) trench MOSFETs during the PBTI test at $V_{GS} = 20\,\text{V}$ and $T_C = 150\,°\text{C}$ for a test duration of $t_{test} = 500\,\text{h}$; in situ read-out of $V_{GS(Th)Down}$ at high case temperature with the gated-diode configuration at $I_D = 1\,\text{mA}$ and an acquisition delay time of $t_{aq(del)} = 1\,\mu\text{s}$; fit with power law as dashed line with factor A_0 and power law exponent b

led to a $V_{GS(Th)}$ decrease in the PBTI test. Negative gate bias attracted mobile ions, such as Na^+ and K^+, in the oxide close to the gate metallization. Consequently, a higher gate voltage was necessary to create an inversion channel at the SiC/SiO_2-interface.

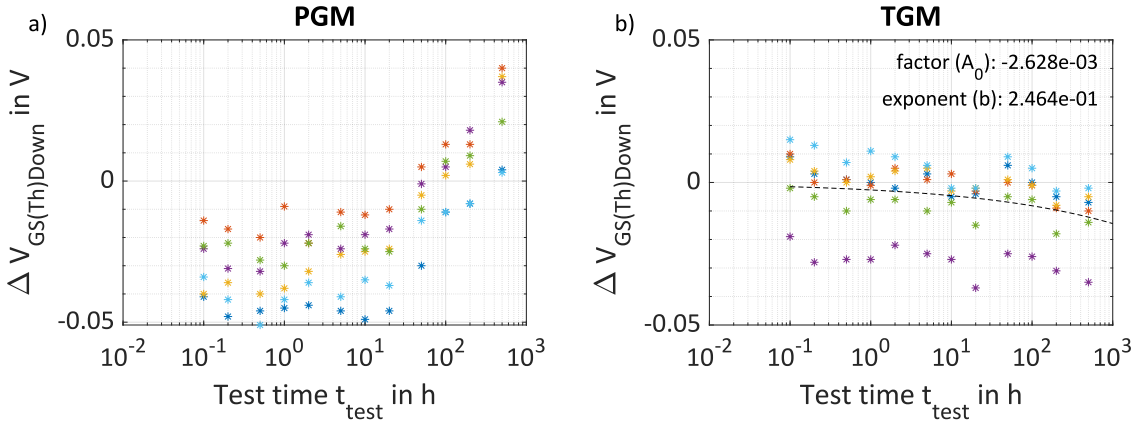

Fig. 6: $V_{GS(Th)}$ drift for a) planar and b) trench MOSFETs during the NBTI test at $V_{GS} = -10\,\text{V}$ and $T_C = 150\,°\text{C}$ for a test duration of $t_{test} = 500\,\text{h}$; in situ read-out of $V_{GS(Th)Down}$ at high case temperature with the gated-diode configuration at $I_D = 1\,\text{mA}$ and an acquisition delay time of $t_{aq(del)} = 1\,\mu\text{s}$; fit with power law as dashed line with factor A_0 and power law exponent b

To model the bipolar gate switching of the PCT, SiC MOSFETs have been examined to a periodically alternated gate stress test. The impact of positive and negative gate bias is clearly visible in Fig. 7, with circles and asterisks representing the $V_{GS(Th)}$ drift after stress with positive and negative gate bias, respectively. Resulting from the initial stress period of $0.1\,\text{h}$ with positive gate voltage, $V_{GS(Th)Down}$ decreased for the PGM group, shown in Fig. 7 a). After the subsequent stress with negative gate bias for $0.1\,\text{h}$ $V_{GS(Th)Down}$ decreased further. With logarithmically increasing time in every stress period for the PBTI and NBTI part the gap between the $V_{GS(Th)}$ drift became more significant. Comparing these results with Fig. 5 a) and Fig. 6 a), several relations become evident. Stress with opposite gate bias counteracts the previous trend and inhibits the resulting drift. Although the impact on the threshold voltage from both stress portions is clearly visible, the resulting drift is reduced, at least for the PBTI part. Despite the higher absolute stress voltage in the PBTI test ($|V_{GS}| = 20\,\text{V}$) than

in the NBTI test ($|V_{GS}| = 10\,\mathrm{V}$), the final $V_{GS(Th)}$ drift after the terminating NBTI part is in the range of the results from negative gate stress in Fig. 6 a) leading to a $V_{GS(Th)}$ increase.

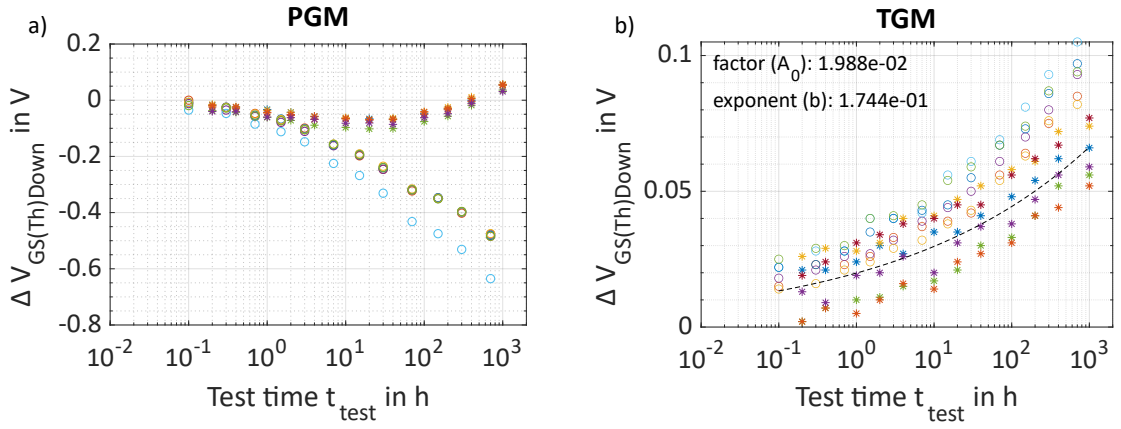

Fig. 7: $V_{GS(Th)}$ drift for a) planar and b) trench MOSFETs during the Alt-BTI test at $V_{GS(on)} = 20\,\mathrm{V}$, $V_{GS(off)} = -10\,\mathrm{V}$ and $T_C = 150\,°\mathrm{C}$ for a total test duration of $t_{test} = 1000\,\mathrm{h}$, including $500\,\mathrm{h}$ PBTI and NBTI stress with equal share; in situ read-out of $V_{GS(Th)Down}$ at high case temperature with the gated-diode configuration at $I_D = 1\,\mathrm{mA}$ and an acquisition delay time of $t_{aq(del)} = 1\,\mu\mathrm{s}$; fit with power law basing on the drift after the NBTI part

Due to different behavior in the DC gate stress tests of the SiC MOEFETs with trench gate structure, the results from the Alt-BTI test deviated significantly from the test of the PGM group. However, the $V_{GS(Th)}$ drift correlates to the results shown in Fig. 5 b) and Fig. 6 b). Positive gate bias led to a $V_{GS(Th)}$ increase, whereas the negative gate bias counteracts the drift. This behavior became more pronounced with increasing test time. Like the results from the PGM group, the final threshold voltage after $1000\,\mathrm{h}$ was between $50\,\mathrm{mV}$ and $100\,\mathrm{mV}$ higher than the initial value. To ensure a justified comparison between the $V_{GS(Th)}$-drift in the PCT and the Alt-BTI test, only the values recorded after the NBTI part have been considered for the fit parameters extraction.

Discussion and Conclusion

Returning to the motivation of this paper, the experimental attempt to model the PCT-driven $V_{GS(Th)}$ drift with different gate stress tests, it becomes evident that no general approach has been found. Especially, due to the complicated and non-uniform drift behavior of the PGM group in the PCT, it was hardly possible to extract reliable fit parameters. Taking the gate stress tests into account, the SiC MOSFETs with planar gate structure indicate the presence and interaction of different mechanisms, affecting the $V_{GS(Th)}$ drift, including interface states and oxide charges. In contrast to the PGM group, the SiC MOSFETs with trench gate structure showed a homogeneous and predictable $V_{GS(Th)}$ drift in the PCT, remaining below $100\,\mathrm{mV}$. In this case, the fit results from PBTI and Alt-BTI test came close to the parameters extracted from the PCT. Especially, the power law exponent b is in the same range for all three tests, whereas the lowest factor A_0 has been extracted from the PCT. This behavior results most likely from the typical temperature swing in the PCT, leading to a slightly lower $V_{GS(Th)}$ drift.

Summary

Threshold voltage instability remains a challenging aspect of SiC MOSFETs. Beside the standard approaches to analyze the $V_{GS(Th)}$ drift in gate stress tests, the impact on power cycling tests became evident as well. Depending on manufacturer or rather manufacturing process and/or MOS structure, the drift intensity and polarity might vary significantly. Only for one out of two test groups, the extracted power law fit parameters were in a comparable range between power cycling and gate stress

tests. Therefore, it is highly recommended to implement the $V_{GS(Th)}$ read-out procedure in power cycling tests of SiC MOSFETs.

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