*Solid State Phenomena*
*ISSN: 1662-9779, Vol. 361, pp 33-38*
*doi:10.4028/p-S31g4f*

*Submitted: 2023-09-05*
*Accepted: 2024-03-05*
*Online: 2024-08-26*

# Early-Stage Reliability Evaluation of Passivation Stack and Termination Designs in SiC MPS Diodes

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**Keywords:** Silicon carbide MPS diode, Accelerated wafer-level BVR reliability test, Ionic-mobile charges, single-zone junction termination extension, protection overcoat design

**Abstract.** We present an early-stage reliability evaluation approach to assess the impact of surface charges in the passivation overcoat (PO) film layers. This is obtained by applying a so-called accelerated wafer-level reverse breakdown voltage stability test in combination with wafer-level static and Van der Pauw measurements. Here, we applied this approach on 4H-SiC merged PiN Schottky diodes with a single-zone junction termination extension fabricated by using different border doses and PO stacks. Accordingly, the correlation between design parameters and the influence of surface charges can be quickly identified, leading to reduced cycle time and enhanced product reliability by optimizing the design of the JTE parameters already in the development phase. This study supports diodes and MOSFETs product manufacturing with an efficient optimization approach to address design and process impacts toward acquiring long-term lifetime demanded in automotive and industrial applications.

## Introduction

Silicon Carbide Merged PiN Schottky (MPS) diodes exhibit great potential for switching power supply applications. An MPS diode consists of interdigitated Schottky and P+-implanted areas (Fig. 1) and combines the best features of both Schottky and PiN diodes to obtain low on-state voltage drop, extremely low leakage in the off-state, fast switching, and superb high-temperature characteristics. In high-voltage devices, avoiding premature breakdown is a key element. A junction termination extension (JTE-) terminated device on n-type material employs a moderately p-doped ring, which surrounds the metal contact and is electrically connected to it. This region spreads the intersections of equipotential lines with the surface away from the active area to more distant points along the surface up to the termination periphery [1].

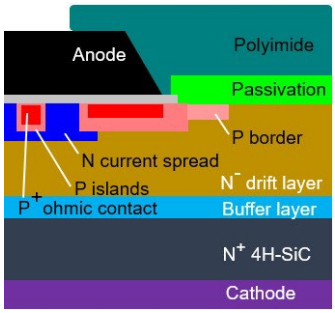


**Fig.1.** Schematic of 4H-SiC MPS rectifiers with a single-zone junction termination extension architecture.

A challenge with JTE design optimization is concerning the surface charge states induced by passivation dielectric layers, which change the electric field distribution at the JTE region [1]. The major advantage of a single-zone JTE design is a straightforward fabrication process, however, it is more susceptible to surface charges compared to other JTE architectures [2]–[6]. Therefore, devices with a single-zone JTE must be carefully evaluated, e.g., in high-temperature reverse bias (HTRB) test [2], [7]–[9]. Furthermore, the impact of surface charges highly depends on their concentration, location, and mobile or static nature.

Given that such surface charge states inevitably exist in the PO layers, it is hence vital to understand their influence in the early product design phase. To this aim, we apply accelerated wafer-level breakdown voltage (BVR) stability tests in association with the wafer-level electrical data analyses to evaluate the performance of different passivation stack designs and single-zone JTE architecture to safeguard the long-term reliability of the SiC MPS diodes.

## Experimental

650V voltage class 4H-SiC MPS test diodes with single-zone JTE architecture were fabricated by using 4H-SiC (0001) with a miscut angle of ~4° towards [11 $\bar{2}$ 0]. In the design of experiments (DoEs) three different PO stack designs, i.e., (i) USG/Si3N4, (ii) TEOS/Si3N4, (iii) SiONx/Si3N4 were used and compared together with devices without PO stack/only polyimide (PI). Each set of experiments was evaluated on three different wafers to provide sufficient statistical results. In addition, the DoEs include two different dose levels (100% and 250%) for the p-border termination to study the impact of termination and stacks design correlation in the reliability. A thick polyimide (PI) layer was deposited on the top of the PO stack to passivate the termination region. Details are shown in Table 1.

The accelerated BVR stability test was carried out at wafer-level at high current (8mA) and temperature (175 °C) and as well as packaged level at at high current (7mA) and room temperature (~30 °C). These results were ultimately verified on packaged devices in reliability tests, i.e, high-temperature reverse bias (HTRB) and high-temperature-pressure-humidity reverse bias (H3TRB). Samples on the wafer were coated with a polymer to prevent arc occurrence during high-voltage wafer-level measurements. The leakage characterization is conducted before and after the stress using a Keysight B1505A power device analyzer.

**Table 1.** The design of experiments including three different passivation overcoat structures with 100% and 250% p-border doses. Additionally, devices with only polyimide (without PO) are investigated as a reference.

| Stack design | p-border dose (%) | p-border dose (cm-2) | BVR (V) |
|---|---|---|---|
| USG/Si3N4/PI | 100 | 2,0E+13 | 824 |
| TEOS/Si3N4/PI | 100 | 2,0E+13 | 829 |
| SiONx/Si3N4/PI | 100 | 2,0E+13 | 819 |
| No PO_ Only PI | 100 | 2,0E+13 | 824 |
| USG/Si3N4/PI | 250 | 5,0E+13 | 452 |
| TEOS/Si3N4/PI | 250 | 5,0E+13 | 445 |
| SiONx/Si3N4/PI | 250 | 5,0E+13 | 786 |
| No PO_ Only PI | 250 | 5,0E+13 | 455 |

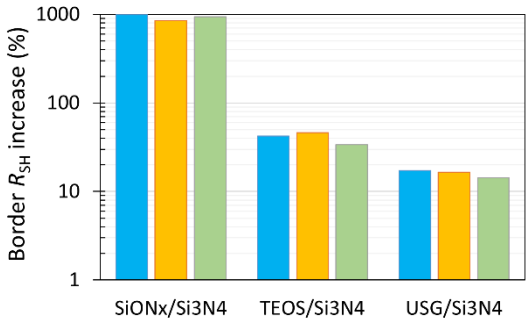


**Fig. 2.** p-border sheet resistance ($R_{Sh}$) variation before and after different PO depositions (not available for only PI option) on the samples with 100% p-border dose. Each stack design is fabricated in three different processed wafers marked with three colors underlying the reproducibility of the results.

## Results and Discussion

The first implication towards device optimization can be conceived from the wafer-level static electrical tests (WLT) evaluation in Table 1, in which for the 250% p-border dose, all PO versions except the SiONx/Si3N4 exhibit low BVR (<<650V) values below the voltage class of the devices, and thus those can be prudently excluded for further investigation. For this reason, further electrical measurements were carried out on the wafers with 100% p-border dose and all the PO variants investigated in this study as well as on the wafers with 250% p-border dose with only the SiONx/Si3N4 PO stack option.

Another point for refining device performance optimization emerges as we consider the border sheet resistance ($R_{Sh}$) before and after PO deposition, which importantly reflects the impact of surface charges in different PO stacks. This parameter is shown in Fig.2 as relative $R_{Sh}$ variation (%), assuming as reference to the values measured before PO deposition. The $R_{Sh}$ is measured on Van der Pauw (VdP) structures in the wafers test pattern. The $R_{Sh}$ variation is remarkably higher with SiONx/Si3N4 (~900%), compared to TEOS/Si3N4 (~40%), or USG/Si3N4 (~20%) PO stacks. This result can be reasonably attributed to the e-field modification induced in the JTE by the positive surface charges in the PO films [1], evidently higher for the SiONx/Si3N4 stack. Given the quite high BVR values measured with SiONx/Si3N4 PO stack at both 100% and 250% border dose, it has to be argued that the substantial $R_{Sh}$ variation induced by this PO stack does not affect the device characteristics at time zero. However, this would not exclude the impact of high surface charge density on the devices' lifetime. For this reason, we carried an accelerated wafer-level BVR stability test on all the PO stack/border dose combinations passing WLT tests and listed in Table 1 which are discussed in the following.

For a proper wafer-level BVR stability test, it is necessary first to prepare the samples. This is due to an arcing issue that can occur at high-voltage measurement between the top metal and uncovered areas at the saw lane leading to an unwanted measurement-related device hard failure. We tackled this problem by preparing the sample with a polymer coverage to increase the dielectric strength. The inset in Fig. 3a shows an exemplary device under test covered with a polymer leaving a small area in the middle for contacting a needle on the topside (anode). Fig. 3a shows the wafer-level BVR stability test results revealing significantly lower stability of devices with 250% p-border dose (with SiONx/Si3N4 PO stack) compared to 100% dose in all the PO stack versions investigated in this study. In fact, diodes with 250% p-border dose and SiONx/Si3N4 PO stack exhibit a consistent degradation of their electrical characteristics after a maximum of ~15 min of stress at 8 mA and 175°C. The effect is clearly visible in Fig.3b where after stress a BVR of about 450V is measured, accompanied by a consistent increase of the leakage current. The BVR stability becomes worse going from the center to the wafer edge showing severe degradation at a much shorter time of only a few seconds. This also implies a low stability of the 250% p-border dose associated with the wafer physical parameters variation at the edge regions.

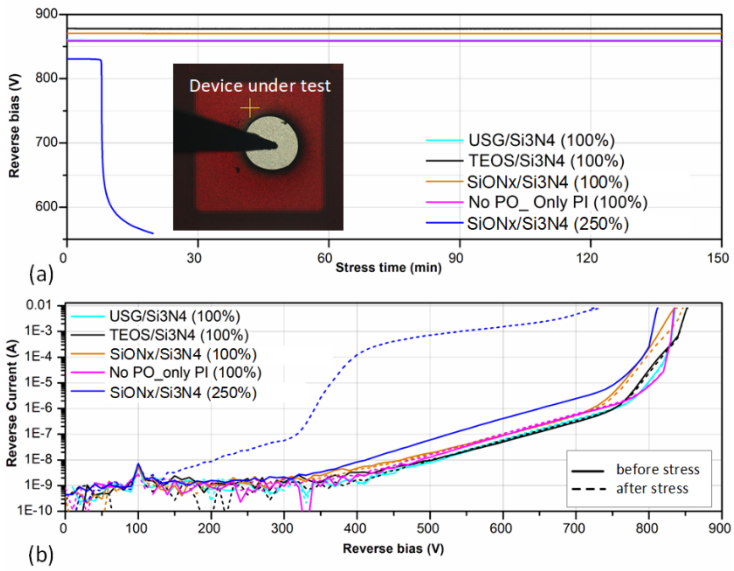


**Fig. 3.** a) BVR stability test results indicating the samples with 250% p-border dose (with SiONx/Si3N4 PO stack) degrade severely ~15 min after starting the test, while no change was measured on 100% border dose regardless of the PO stack design. Inset shows an exemplary device under measurement with a polymer coating for arcing prevention at high voltages. (b) Reverse characteristic before (solid line) and after (dashed line) BVR test shows no change for 100% border dose and a significant leakage current increase for 250% border dose.

In contrast, all devices with lower p-border dose (100%) exhibit robust characteristics after 2.5 hours (Fig. 3a), regardless of the different PO stack used on the JTE. The extended BVR stability testing on these devices shows no degradation, even up to 8 hours under such intensive stress. Moreover, devices behave uniformly, irrespective of their position on the wafer. The reverse characteristic before and after stress (Fig. 3b) revealed no changes at the maximum rated voltages underlying a successful control over the surface charges.

To elucidate this, we conducted TCAD simulation, as shown in Fig.4. Fig. 4a showcases the dependence of breakdown voltage on the interface charges for 250% p-border and the SiONx/Si3N4 PO stack. Accordingly, while in the presence of induced positive charges, the VBR well fits the device BVR specification, it significantly decreases upon reduction in the charge density. Fig. 4b displays the condition without any surface charges at which the field crowding occurs at the edge of JTE and devices show a low BVR of ~450V. This is consistent with the outcomes of the wafer-level stability test in which following failure, devices with a 250% p-border and SiONx/Si3N4 PO stack exhibit a BVR value of approximately 450V, suggesting the dissipation of the charge effects. Fig. 4c depicts the impact of high positive charges induced by the SiONx/Si3N4 PO stack leading to a modification in the electric field distribution at the JTE area. Consequently, a quasi-JTE elongation forms, allowing devices to initially function within their specified breakdown voltage rating. However, under conditions of high temperature and high reverse voltage, the accumulated charges compensate or migrate within the PO layer over time. This results in an imbalance in potential at the JTE, leading to a decrease in BVR and eventually device failure.

Also, the TCAD simulation results are consistent with the VdP and WLT results previously shown, indicating that the high amount of positive surface charges induced by the SiONx/Si3N4 PO stack drastically increases the sheet resistance after the PO deposition. On the other hand, all the PO stacks with 100% p-border dose are robust, confirming that this border dose value is evidently in the middle of the tight BVR stability window versus border dose, typical of single zone JTEs, and for this reason less sensitive to surface charges impact [1].

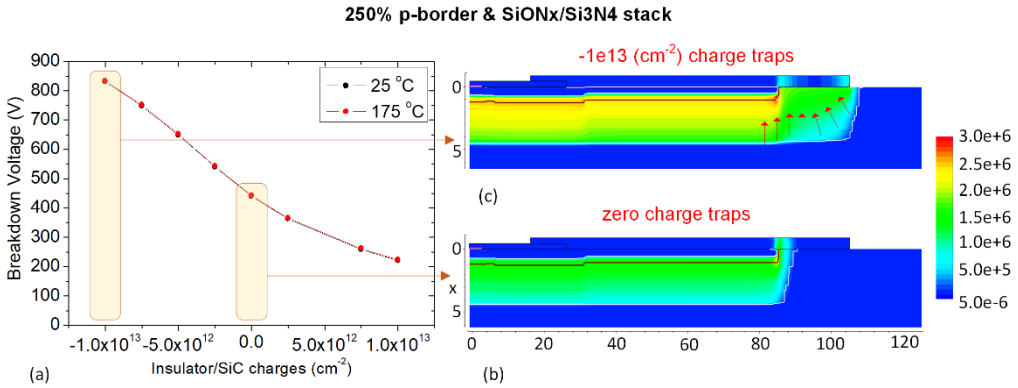


**Fig 4.** TCAD simulation of devices with 250% p-border dose and SiONx/Si3N4 stack. a) Dependence of breakdown voltage dependence charge densities interface layer demonstrating typical BVR range about 850V for high positive charges while it drops as the positive charge density decreases. Electric field distribution at the JTE region in absence (b) and presence (c) of interface charge states. The induced positive interface charges result in a quasi-JTE extension, allowing the devices to operate within the initial BVR specification. However, subjecting the devices to elevated temperatures and high reverse voltage causes the positive charges' impact (c) to diminish, leading to a transition back to a lower BVR range as shown in (b).

This evidences that the termination behavior is mainly governed by the accurate control of the border dose. That said, additional investigations were performed to determine which of the remaining PO stacks inducing low surface charge density enables delivering a longer lifetime with 100% p-border dose. To this purpose, additional BVR stability (see Table 2.) and reliability tests (see Table 3.) were carried out at the packaged level on a number of diodes with 100% and 250% p-border dose and different PO stack options. For BVR stability test, the devices were soldered on PCBs and stressed under an avalanche condition of 7 mA at room temperature. These parameters were selected to facilitate accelerated testing while maintaining Tj<200°C, thereby preventing the initiation of irrelevant failure modes. The findings unequivocally indicate premature failure in samples with 250% p-border dose, whereas the remaining two designs with 100% p-border dose and USG/Si3N4 PO stack and only PI options exhibit robust performance even after two weeks of continuous intense stress.

**Table 2.** Packaged level BVR stability test. Early failure (~32 hours) for the diode with 250% p-border dose and SiONx/Si3N4/PI stack while other samples exhibit robust behavior even after 2 weeks.

| Sample | Test Condition | #Fail_Duration |
|---|---|---|
| USG /Si3N4/PI (100%) | $I_{ava}$ = 7mA<br>Ta = 30°C<br>Tj < 200°C | 2 weeks |
| No PO_Only PI (100%) | | 2 weeks |
| SiONx/Si3N4/PI (250%) | | 32 hours |

**Table 3.** Packaged level qualification results. Each test was performed on 80 samples. All stack designs passed H3TRB test after 4000h. Only SiONx/Si3N4/PI stack with 250% p-border dose failed in HTRB as expected from the BVR stability test on wafer & package level.

| Sample | **HV-HTRB**<br>(T=175°C; Vr=650V) | **HV-H3TRB**<br>(T=85°C; 85% RH; Vr=650V) |
|---|---|---|
| USG /Si3N4/PI (100%) | 0/80 _ 4000h | 0/80 _ 4000h |
| No PO_ Only PI (100%) | 0/80 _ 4000h | 0/80 _ 4000h |
| SiONx/Si3N4/PI (250%) | 16/80 _ 168h | 0/80 _ 4000h |

Furthermore, the results of the HTRB and H3TRB tests further verify the short-loop BVR stability results. Once again, the samples with 250% p-border dose and SiONx/Si3N4 PO stack demonstrate a pronounced failure mode during the HTRB test, whereas all the other samples with 100% p-border dose successfully pass the 4000 hours of both HTRB and H3TRB tests. These results significantly surpass the automotive qualification standard, underscoring the effectiveness of the introduced approach and design optimization.

Overall, USG /Si3N4 and SiONx/Si3N4 with 100% p-border dose exhibit extremely robust and quite similar performances under high voltage, temperature, and humidity stress. The samples without PO layer were included to gain insights into surface charges when compared to other stack designs. While these samples exhibit strong performance at the package level, they are susceptible to vulnerabilities under harsh conditions, such as in applications as bare die in modules, which offer less hermeticity compared to mold compound encapsulation. Consequently, it is advisable to opt for designs that incorporate the PO layer for an enhanced lifetime.

## Conclusions

We presented a short-loop reliability evaluation approach using an accelerated wafer-level BVR stability test in combination with wafer-level electrical data analyses. By utilizing this approach, we showed that the passivation PO/PI stacks and single-zone JTE in SiC MPS diodes could be designed and optimized to control the impact of induced surface charge states to achieve products with extended lifetime. This is verified by packaged level BVR stability test along with HTRB and H3TRB results which showcase the robust products performance of the optimized designs beyond 4000h without any sign of degradation. The presented method enables a time- and cost-efficient approach to address the process and design flaws and issues in the early stages without requiring undergoing the assembly process of diode and MOSFET products.

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