Solid State Phenomena
ISSN: 1662-9779, Vol. 361, pp 39-45
doi:10.4028/p-CB1KRz

Submitted: 2023-08-31
Revised: 2024-03-25
Accepted: 2024-04-05
Online: 2024-08-26

A Unique Failure Mode of SiC MOSFETs under Accelerated HTRB

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Keywords: SiC MOSFET, ALT-HTRB, Lifetime Model, Gate Oxide Degradation

Introduction

Device lifetime under reverse bias conditions is an important reliability concern for SiC devices. Provided that the termination structure is well designed, device failure in the active cell is driven by gate oxide breakdown due to the high field in the semiconductor and gate dielectric. For planar MOSFETs, the largest field occurs in the JFET region [1,2]. Standard HTRB testing is insufficient to estimate failure rates under operating conditions and hence testing under accelerated off-state conditions (ALT-HTRB) is required. This paper provides data, statistical analysis, failure analysis and finally a Weibull statistics-based temperature, V_d and stress time dependent model.

Devices and Experimental Data

The devices used in this study are 16mΩ, 750V rated planar gate MOSFETs, packaged in TO-247. Devices are stressed in parallel under different V_d and temperature conditions as listed in Table 1. It takes ~2s to reach the desired V_d,. An additional 2s stabilization is used before any device measurement is performed. Sample size is 48 devices per stress condition. Although the voltage rating is 750V, the transistors are stressed at V_d ranging from 875V up to 950V, with V_g=0V. In agreement with [1], stress conditions are in the V_d range of 0.875 to 0.95% of the avalanche voltage.

Table 1. Experimental matrix for the ALT-HTRB stress tests (V_g=0V).

T (ºC)	V_{ds} [V]	Stress time [Hrs]	Failures [%]
25	875	1166	0
25	920	888	45
25	935	556	44
25	950	472	87
175	875	1166	0
175	900	920	12
175	920	416	27
175	950	556	37

Fig. 1 shows typical off-state I_d-V_d characteristics for two different temperatures. As from V_d~920V, I_d at RT is larger than I_d at T=175ºC. The breakdown of the devices (measured at 10mA) is ~1kV. Fig. 2 shows I_g and I_d at the stress condition at the start of the stress. For each group, the devices with the highest I_d fail first, indicating that I_d is a good proxy for the probability of a device to fail under ALT-HTRB. For I_g, there is no distinction between failed and non-failed devices.

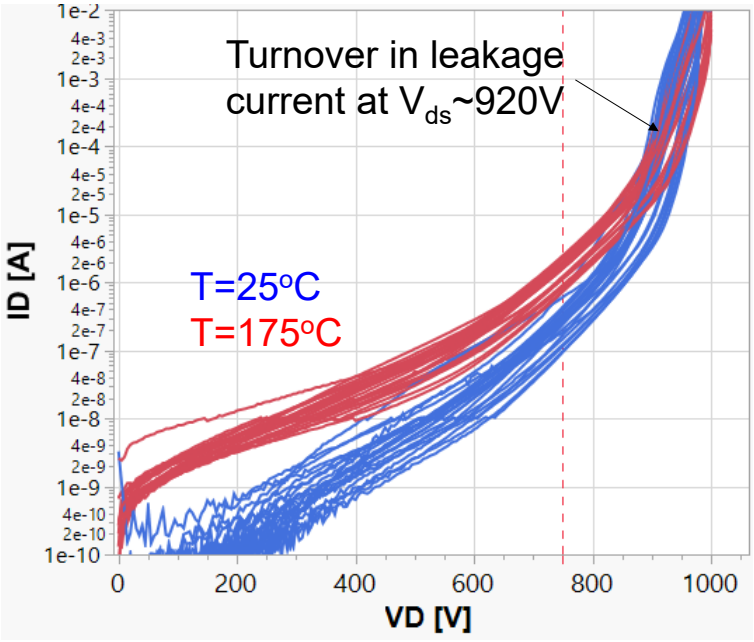

Fig. 1. I_d-V_d characteristics of SiC parts at V_g=0V, at T=25°C and 175°C. V_{rating}=750V, V_{bd}~1kV. The vertical red dashed line denotes the voltage rating of the devices.

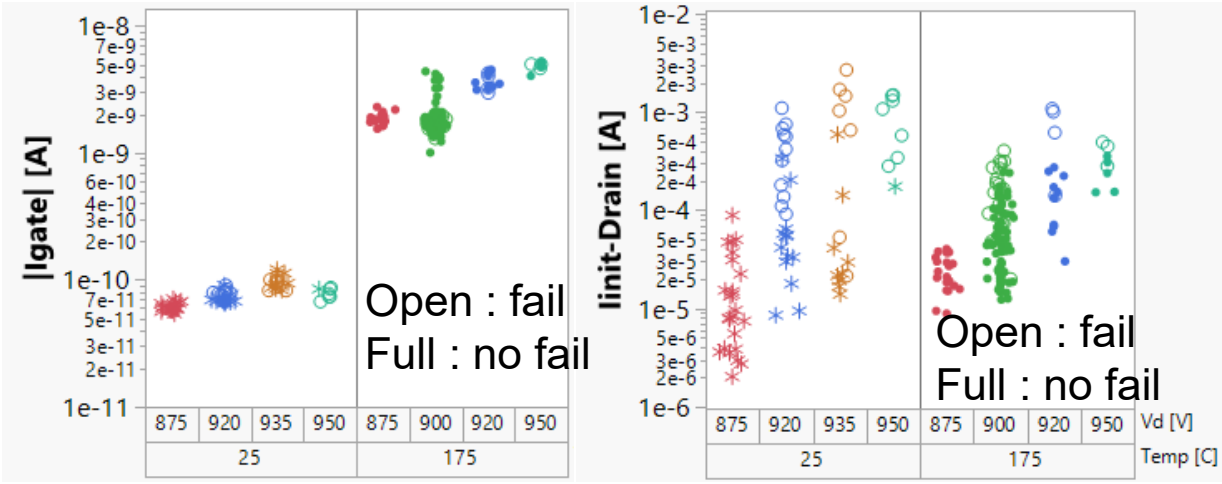

Fig. 2. Initial I_g and I_d at the stress condition for the devices under ALT-HTRB. Open symbols are the devices that fail during the test (see Table 1).

Fig. 3 plots the $t_{63\%}$ derived from the Weibull statistics for all experiments using censoring for the non-failing devices and using the E-model for field acceleration [1]. In line with the expectation from the drain leakage current (Fig. 1) and the observation that the failure mode is current driven (Fig.2), there is a cross-over in t_{fail} at V_d~920V. Using the field acceleration model of Fig. 3 (E-model) and assuming an Arrhenius temperature dependency, a lifetime contour map can be constructed for any given desired ppm level using the t63% failure times and an experimental Weibull slope of β=1.5. As an example, Fig. 4 shows the lifetime contour map at 100ppm.

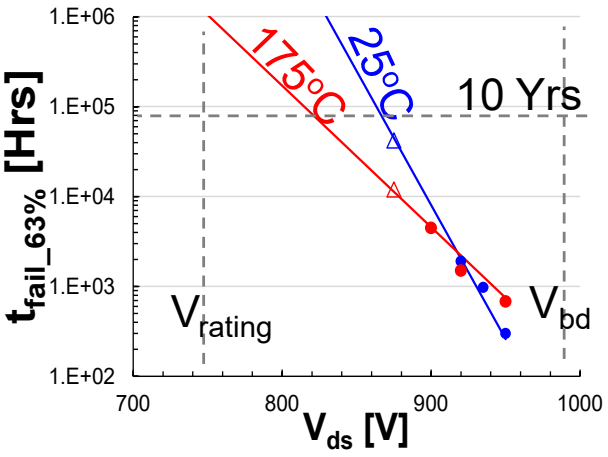

Fig. 3. $t_{63\%}$ derived from the Weibull statistics of the t_{fail} data, using the E-model. For V_d>920V, the t_{fail} is lower at T=25ºC compared to T=175ºC, see also Figs 1 and 2.

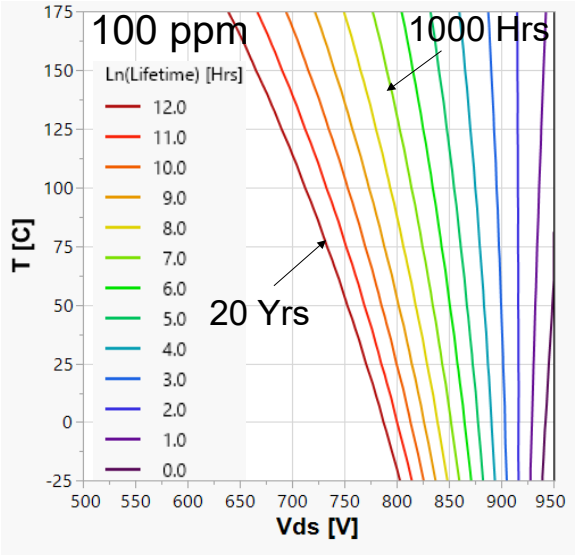

Fig. 4. Lifetime Contour map at 100ppm failure rate, from the $t_{63\%}$ failure data (Fig. 3) and Weibull slope β=1.5. Above V_d=920V lifetime improves with increasing temperature, see also Figs 1, 2 and 3.

Failure Analysis

Failure analysis is performed on 20 devices, from all groups of the experimental matrix. In all cases, the failure spot is in the active area, in the center of the hex cell of the JFET region, see Fig. 5. More specifically, the devices all fail as shown in Fig. 6 i.e. at one side of the hex cell only (red dots). If only the electric field in the SiC and/or SiO_2 would be the driving factor, half of the population is expected to fail at the location of the green spots of Fig. 6. This unexpected anomaly can be explained by the anisotropy of the avalanche plasma, which moves faster along the c-plane [2] and the fact that the crystal has a 4º offcut angle. Therefore, avalanche carriers generated at the p-body/n-epi junction at the location of the green arrows and dots in Fig.6 will move under the p-body contact region where there is no gate oxide. In contrast, avalanche carriers generated at the location of the red arrows and dots will encounter the higher field in the JFET region and create electron/hole pairs. These hot holes can then cause SiO_2 degradation and wear-out, ultimately leading to failure. This is another argument that the degradation of transistors under ALT-HTRB is driven by avalanche in the semiconductor and is dissimilar to gate oxide degradation during TDDB. Hence care should be taken on which field acceleration model to use. On two samples TEM was done, but no crystal defects were revealed in either sample, in agreement with [1] but in contrast to [3,4,5].

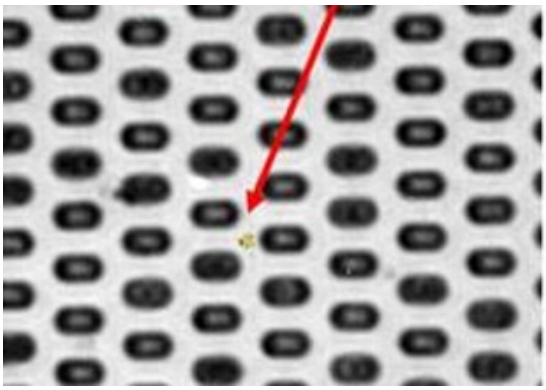

Fig. 5. Typical example of the failure location during ALT-HTRB (OBIRCH). The devices always fail in the center of the hex cell of the JFET region.

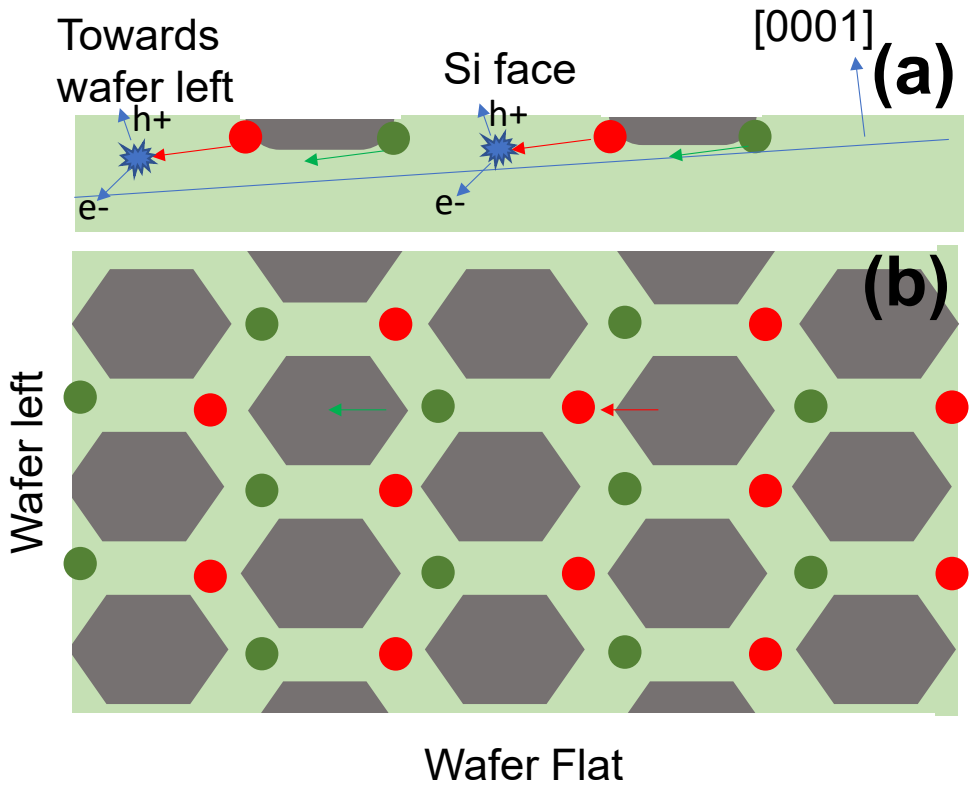

Fig. 6. (a) cross section of the SiC crystal from the wafer flat. The grey regions denote the p-body areas, green is the n-epi/JFET region. The 4° off-axis angle is towards the left side of the wafer when the flat is at the wafer bottom. (b) top view of the cell layout, with the wafer flat at the bottom. Impact ionization occurs at the curvature of the p-body/n-epi (both at the red and green dots). The *red dots* represent the locations where the devices *always fail* (see Fig. 5). The *green dots* represent the locations where the devices *never fail*. Only for the red dots, avalanche carriers (generated at the pbody/n-epi junction) can reach the high field region in the JFET. This is because the impact ionization plasma preferentially moves along the c-plane, i.e. to the left of the wafer because of the 4° offcut angle [3]. Secondary hot holes are only generated if the plasma reaches the JFET high field area (red dots).

During stress, I_g and I_d for each individual device is monitored. When either I_g or the I_d reaches compliance at 100nA or 1mA, the device is reported as a "soft" or "hard" failure respectively. Figs. 7 and 8 show the on-state and off-state characteristics of two typical "soft" and "hard" failed devices. Irrespective of "soft" or "hard" failure mode, the emmi spot is always in the center of the hex cell (as in Fig. 5).

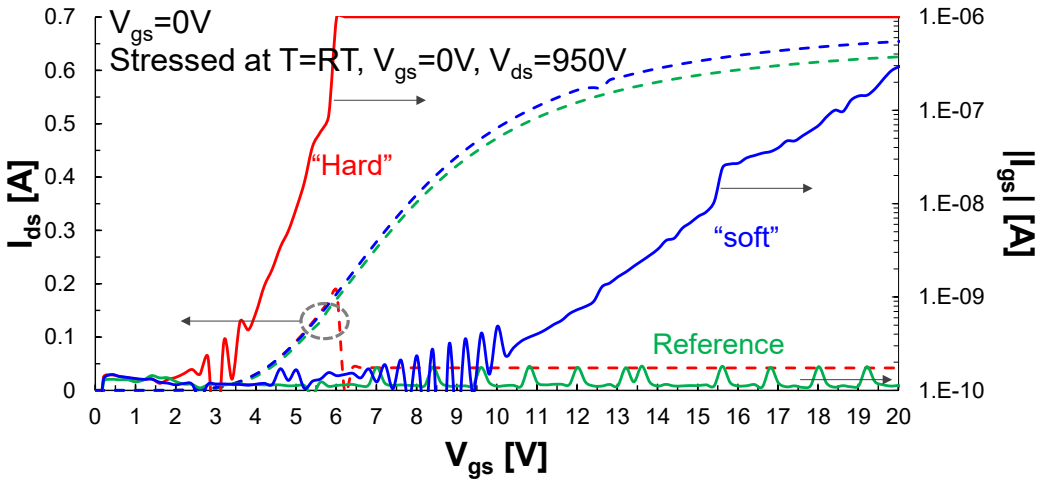

Fig. 7. On-state characteristics of "failed" devices (stress condition T=RT, V_d=950V). "soft" failure when I_{g_off} reaches compliance (100nA), "hard" failure when I_{d_off} reaches compliance (1mA). For the "soft" failing device the transistor is still working properly, with good on-state and off-state behavior (see also Fig. 8). For the "hard" failing device, transistor action is lost.

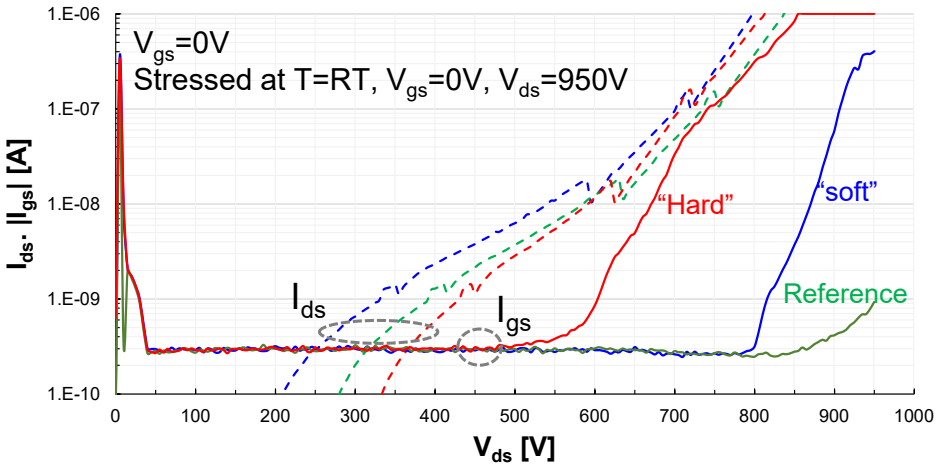

Fig. 8. Off-state characteristics of "failed" devices (stress condition T=RT, V_d=950V). Same devices as in Fig. 7. "soft" failure when I_{g_off} (at stress condition) reaches compliance (100nA), "hard" failure when I_{d_off} (at stress condition) reaches compliance (1mA). For the "soft" failing device, the transistor is still working properly.

Parametric Degradation During Stress

During stress device parameters are measured in-situ. Up till failure, all prime device characteristics remain unchanged (V_{th}, R_{on}, I_{g_on}, I_{d_off}, etc), except for I_{g_off} (measured at the stress condition) see Fig. 9. I_{g_off} drops due to the build-up of positive charge in the dielectric in the JFET region. The fact that the prime device parameters do not change with stress indicates that the degradation is not in the channel area of the transistor, but in the JFET area, in agreement with the model of Fig. 6.

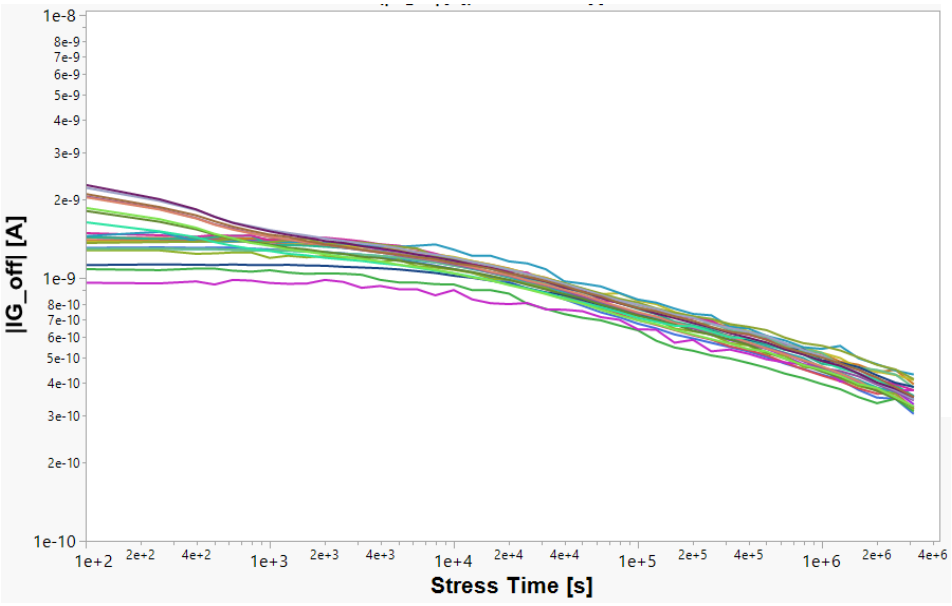

Fig. 9. Parametric degradation of $|I_{g\_off}|$ during ALT-HTRB stress at V_g=0V, V_d=900V, T=25ºC. I_{g_off} measured at the stress condition of V_d=900V. I_{g_off} drops due to the build-up of positive charge in the gate dielectric during stress.

ALT-HTRB versus Single Event Burn-out (SEB)

It is instructive to compare the magnitude of the failure rate of ALT-HTRB against other failure mechanisms that occur under reverse bias, more specifically single event burn-out (SEB) due to cosmic rays. Fig. 10 shows the extracted FIT rates for ALT-HTRB (calculated from the MTTF of the Weibull data), compared to SEB FIT rates (from neutron irradiation experiments).

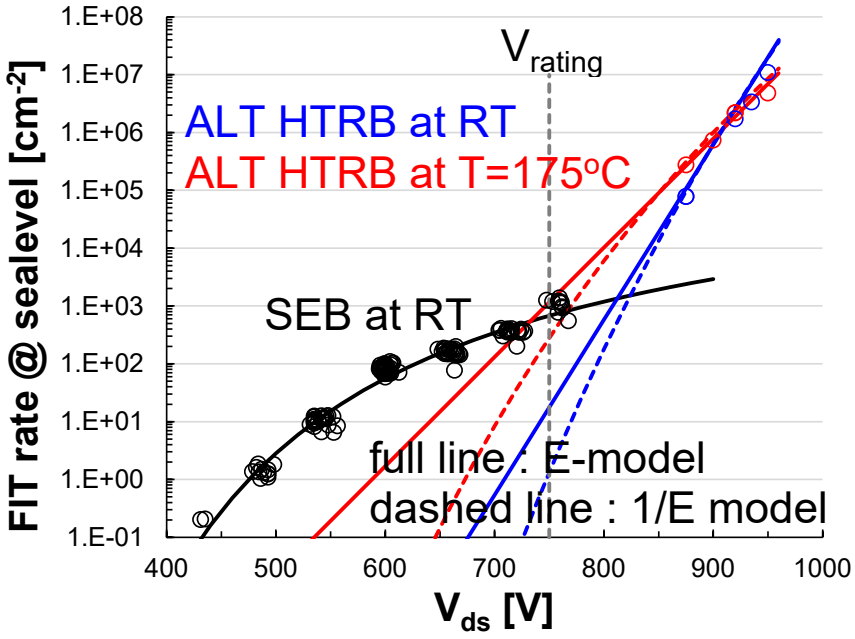

Fig. 10. SEB and ALT-HTRB FIT rates. For ALT-HTRB, the full lines correspond to the E-model (as per JEDEC JC70.2), whereas the dashed lines correspond to the 1/E model (which is in line with an avalanche model, since $t_{fail} \sim J_{aval}^{-1} \sim J_d^{-1}.\exp(1/E)$. Up to V_{rating}, the FIT rate is determined by SEB, not ALT-HTRB.

Although throughout the paper the E-model is used for field acceleration for ALT-HTRB (as per JEDEC JC70.2), it is instructive to also calculate the extrapolation for the 1/E model (dashed lines in Fig. 10). The 1/E model is more in line with an avalanche driven failure mode, since

$t_{fail} \sim J_{aval}^{-1} \sim J_d^{-1}.\exp(1/E)$

Up to V_{rating}, the FIT rate is determined by SEB and not by ALT-HTRB.

Conclusion

This paper provides evidence that the failure mode during ALT-HTRB is driven by avalanche driven hot holes, which is different from standard TDDB gate oxide degradation. Model extrapolation shows that below V_{rating} SEB dominates the FIT rate. In all of the failing devices that were submitted for failure analysis, no crystal defects were found to be the root cause of the failure. This finding is in agreement with [1] but in contrast to the findings of [3,4,5].

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