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Design Optimization and Reliability Evaluation in 1.2 kV SiC Trench MOSFET with Deep P Structure

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Abstract In this paper, 1.2 kV SiC trench MOSFET with deep P structure has been proposed to effectively shield the trench bottom oxide. The various design splits, such as N concentration between deep P and deep P to trench distance, were experimentally evaluated and TCAD simulations were performed to extract maximum oxide electric field at trench bottom. Based on trade off results, critical design parameters were optimized to obtain low Rdson and stable breakdown voltage with acceptable oxide electric field. To evaluate trench gate oxide reliability in wafer level, gate oxide integrity (GOI/Vramp), charge to breakdown (QBD), and time dependent dielectric breakdown (TDDB) tests were conducted. Also, high temperature gate bias (HTGB) and high temperature reverse bias (HTRB) stress tests were carried out for assembled samples to compare device reliability depending on different designs. For the target design, the promising reliability results were confirmed in both wafer level and assembled samples.

Introduction

SiC trench MOSFET have drawn attention as one of the promising candidates in high voltage application because of low on-state resistance and high switching performance, compared to the conventional planar MOSFET. While the superior trench channel mobility and high active cell density made it attractive [1], there have been concerns for trench gate oxide reliability, derived from high electric field in high voltage condition [2]. Various concepts to protect trench bottom oxide have been proposed [3], but there are still design requirements to effectively control the maximum oxide electric field without losing inherent advantages in the trench MOSFET. In this study, 1.2 kV SiC trench MOSFET with deep P structure was suggested and critical design parameters were optimized for Ron and maximum oxide electric field. Also, trench gate oxide reliability was investigated for both dies in wafers and assembled samples.

Experimental Details

1200 V trench channel SiC MOSFETs were fabricated on 4H-SiC wafers. Fig. 1 shows cross sectional view of the proposed trench MOSFET with deep P structure. The MOSFET channel was formed on trench sidewall to increase cell density with higher channel mobility and high N concentration regions were fabricated around the trench to decrease on-state resistance. The deep P structures were formed close to trench to relieve electric field on trench bottom oxide. As critical parameters, the deep P to trench distance was varied in one mask shot and N implant doses under the trench were controlled in different wafers. Also, P implant doses for trench channel were adjusted to evaluate the amount of Ron increase depending on threshold voltage.

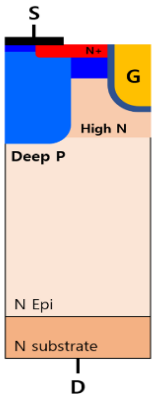

Fig. 1. Schematic of SiC trench MOSFET with deep P structure.

To assess trench gate oxide reliability in wafer level, gate oxide integrity (GOI/Vramp), charge to breakdown (QBD), and time dependent dielectric breakdown (TDDB) tests were conducted. The GOI/Vramp and QBD tests were performed for dies, which were randomly selected in a wafer after DC test. The gate oxide breakdown voltage in GOI/Vramp test and time to breakdown in 20 mA/cm^2 stress condition were recorded respectively. In TDDB tests, 51.5, 53.0, 54.5, 56.0 V gate bias stresses were applied until devices were failed at 175 ºC.

Furthermore, target N concentration wafers were assembled in TO247-4L package with splits of deep P to trench distance to compare reliability depending on oxide electric field at reverse bias. In high temperature reverse bias (HTRB) stress tests, 1.2 kV bias was applied to target and wide distance design samples at 175 ºC for 1000 hrs and fail samples were screened by interim DC tests. In addition, high temperature gate bias (HTGB) stress tests were conducted in target design with 22V bias at 175 ºC to confirm trench gate oxide integrity in assembled samples.

Results and Discussion

Device characteristics and TCAD simulation analysis Fig. 2, Fig. 3, and Fig. 4 present measured VTH, Ron, and BV characteristics depending on deep P to trench distance and N concentration splits in 9 mm^2 die. The DC characteristics were measured for over 100 dies in each design splits and average values were calculated to investigate the trend for critical parameters.

In Fig. 2, the threshold voltage shows increasing trend, as narrowing deep P to trench space in target and low N concentration, which means the aluminum dopants used to form deep P structure can affect channel dose because of lateral straggle. This effect is more significant when deep P is close to trench and there is little change in VTH for high N concentration condition.

Fig. 3 depicts the Ron sensitivity depending on N concentration and deep P to trench distance. In case of low N concentration, sharp Ron increase can be shown near the target deep P to trench distance, which can result in unstable Ron even in small process variation. Whereas, for target and high N concentration conditions, even though they also show increasing trend, as decreasing deep P to trench distance, robust Ron can be expected in possible process variation for target deep P to trench distance.

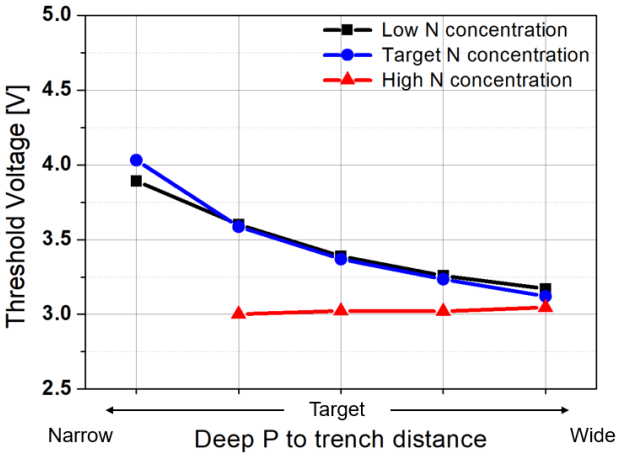

Fig. 2. Threshold voltage trend depending on N concentration and deep P to trench distance. (Measurement)

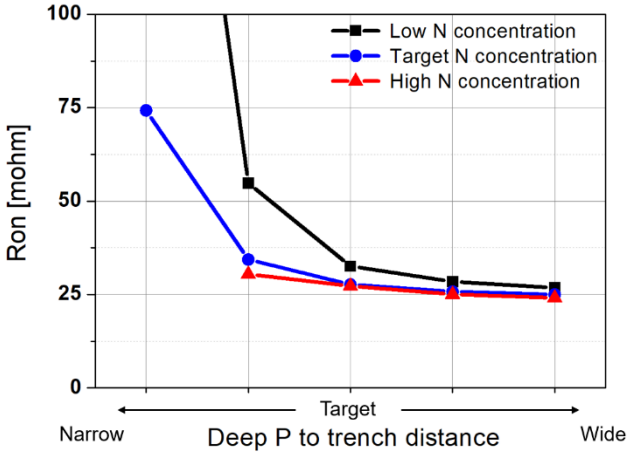

Fig. 3. Rdson trend with 18V gate bias depending on N concentration and deep P to trench distance. (Measurement)

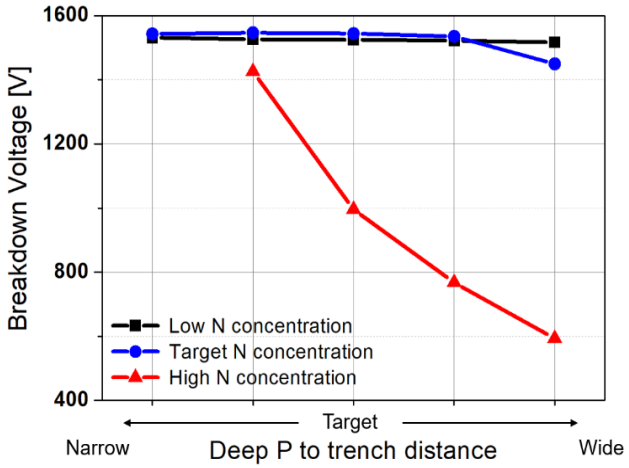

Fig. 4. Breakdown voltage trend depending on N concentration and deep P to trench distance. (Measurement)

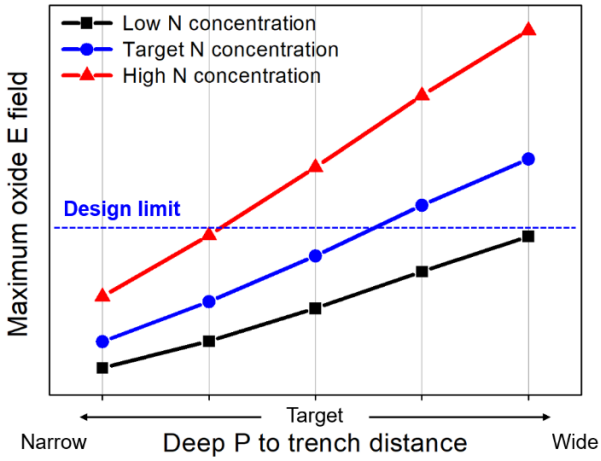

Fig. 5. Maximum oxide electric field at 1200V trend depending on N concentration and deep P to trench distance. (Simulation)

Meanwhile, clear BV reduction was observed, as increasing deep P to trench distance for high N concentration in Fig. 4. It can be explained by channel punch through phenomenon caused by high electric field at the end of the channel, which is prominent in high N concentration and wide deep P to trench distance. Based on these experimental results, it is concluded that the N concentration cannot be increased too much in target deep P to trench distance to obtain stable BV.

Also, TCAD simulations were performed to investigate the risk of trench gate oxide according to critical parameters and the maximum oxide electric field values in each design were extracted in Fig. 5. The maximum oxide electric field is increased as deep P to trench distance or N concentration are increased, which is matched well with the BV trend. In assumption of allowable maximum oxide electric field for stable operation of the device, it can be seen that N concentration cannot exceed a specific value in target deep P to trench distance.

In summary, the high N concentration condition has advantages of low Ron, but it shows low BV and oxide breakdown risk at reverse bias due to the high oxide electric field. On the other hand, the low N concentration wafer is beneficial to stable BV and low oxide electric field, however steep Ron increase is observed in narrow deep P to trench distance. According to this trade-off between Ron and oxide electric field, target N concentration and deep P to trench distance were determined to secure stable Ron variation and BV with acceptable maximum oxide electric field.

Fig. 6 represents VTH and Ron trend with variation of channel P dose. In order to evaluate the increase of Ron depending on VTH rise in the trench channel, the channel P dose was varied in a wide range. While VTH shows a large change from 2.2 V to 4.3 V in experimental splits, Ron change is marginal from 27 mohm to 30 mohm. It indicates that the rise of VTH makes a limited effect on Ron degradation, which results from low channel resistance in trench MOSFET.

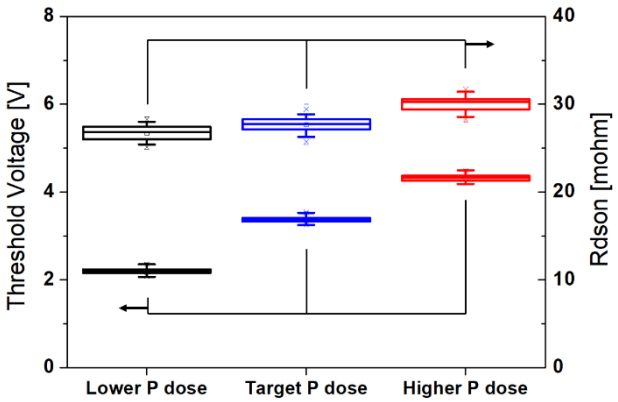

Fig. 6. VTH and Ron trade-off in trench channel P dose splits.

Wafer level reliability test To evaluate trench gate oxide integrity and reliability in wafer level, GOI/Vramp, QBD, and TDDB tests were performed. In GOI/Vramp test, 100 dies were randomly selected from target design wafer after pre-sorting test and the gate voltage was increased until the gate leakage current reached 100 mA. (Inset of Fig. 7) For each die, the gate

voltage that makes the leakage current of 10 mA was recorded as the gate oxide breakdown voltage and sorted in increasing order in Fig. 7. As a results, promising trench gate oxide integrity was verified with extrinsic failure rate less than 1 defect/cm^2. In QBD assessment, a constant current stress of 20 mA/cm^2 was applied to each die until it failed due to gate oxide breakdown. During the stress, the gate voltage for constant current and stress time were recorded as shown in inset of Fig. 8. The stress time to gate oxide breakdown was converted into charge to breakdown divided by gate area and sorted in ascending order in Fig. 8. Consequently, the charge to breakdown values exceeding 1 C/cm^2 were confirmed for all dies.

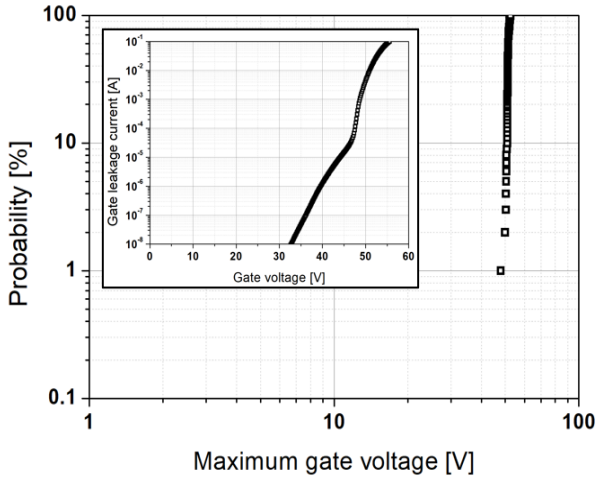

Fig. 7. Gate oxide integrity (GOI) in wafer level

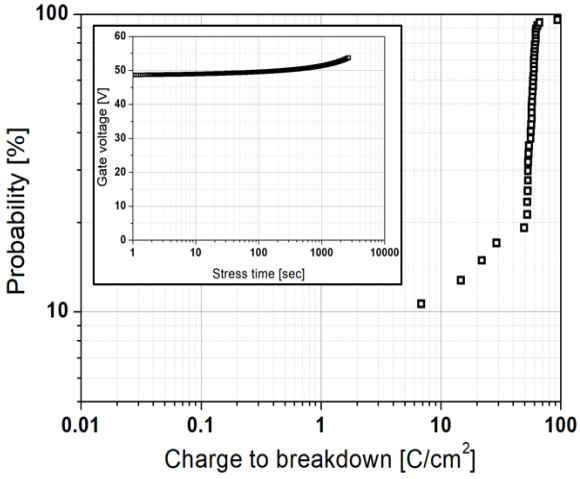

Fig. 8. Charge to breakdown (QBD) in wafer level

In addition, constant voltage stresses of 51.5 V, 53.0 V, 54.5 V, and 56.0 V were applied to each die at 175 ºC until gate oxide breakdown occurred in TDDB test. The lifetime of each die was arranged in increasing order and presented in Fig. 9 for lifetime prediction at each gate voltage stress. Based on these results, lifetime estimation at the max operation voltage was investigated and gate oxide lifetime over 20 years with cumulative failures less than 5 ppm was guaranteed in 22 V max operation bias.

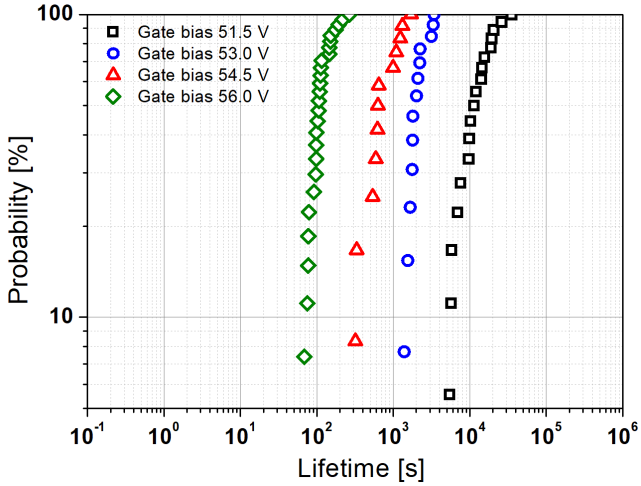

Fig. 9. Time dependent dielectric breakdown (TDDB) in wafer level

Package level reliability test In target N concentration condition, target deep P to trench and wide deep P to trench dies were assembled in TO247-4L package to compare package level reliability depending on maximum oxide electric field. In HTRB stress test, over 400 samples were randomly selected from each design and 1.2 kV drain bias was applied for 1000 hrs at 175 ºC with interim readout at 168 hrs and 500 hrs. While no device failure was observed in target design until 1000 hrs,

5 samples and 1 sample failures were detected in wide deep P to trench design at 168 hrs and 500 hrs respectively in Table I. The die failures in HTRB test for wide deep P to trench design can be explained by trench gate oxide damage or increased channel leakage current due to higher electric field. It demonstrates that the maximum electric field at trench bottom oxide is one of the key factors for reliability at reverse bias.

To verify trench gate oxide reliability, HTGB stress test was performed on target design samples. The 480 target design samples assembled with TO247-4L were randomly selected and 22 V max operation gate bias was applied at 175 ºC for 1000 hrs. For all samples, there were no failures until 1000 hrs, which corresponds to robust trench gate oxide integrity results in wafer level. (Table II)

Table I. High temperature reverse bias stress (HTRB) results.

Condition	+1.2 kV HTRB reliability fail rate		
	168h	500h	1000h
Target design	0/480	0/480	0/480
Wide deep P to trench distance	5/432	1/427	-

Table II. High temperature positive gate bias stress (HTGB) results.

Condition	+18V HTGB reliability fail rate		
	168h	500h	1000h
Target design	0/480	0/480	0/480

Summary

In this work, 1.2 kV SiC trench MOSFET with deep P structure was fabricated to relieve maximum oxide electric field at trench bottom. As critical design parameters, N concentration and deep P to trench distance were experimentally varied and VTH, Ron, and BV trends were investigated according to various design splits. Also, the maximum electric field values were extracted by TCAD simulation. In case of high N concentration and wide deep P to trench distance design, there are advantages of low Ron, but it has low BV and oxide breakdown risk due to high oxide electric field. Whereas low N concentration and narrow deep P to trench distance design are beneficial to stable BV and low electric field, however Ron variation was a major concern. Based on this trade-off, target N concentration and deep P to trench distance are carefully determined to obtain stable Ron and BV with acceptable maximum oxide electric field. In addition, the VTH and Ron trend with variation of channel P dose was evaluated and marginal Ron increase was confirmed with significant rise of VTH.

To investigate trench gate oxide reliability in wafer level, GOI/Vramp, QBD, and TDDB tests were performed. As a result, extrinsic failure rate less than 1 defect/cm^2 was verified in GOI/Vramp test and charge to breakdown values over 1 C/cm^2 were confirmed for all dies in QBD assessment. Moreover, gate oxide lifetime over 20 years with cumulative failures less than 5 ppm was guaranteed in TDDB test for 22 V max operation bias. Meanwhile, HTRB and HTGB reliability tests were conducted for TO247-4L package samples, and no failures were detected for 1000 hrs in target design.

In summary, key design parameters were optimized to effectively protect trench bottom oxide in the proposed trench MOSFET with deep P structure and the promising reliability results were confirmed in both wafer level and assembled samples for target design.

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