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UIS Ruggedness of Parallel 4H-SiC MOSFETs

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Abstract. We have studied the UIS (Unclamped Inductive Switching) ruggedness of SiC MOSFETs in parallel. We show that UIS ruggedness of parallel MOSFETs is a function of the difference in their breakdown voltage (Δ-BVDSS). As expected, for large Δ-BVDSS UIS, ruggedness is dominated by the lower BVDSS transistor. Somewhat unexpectedly, for small enough Δ-BVDSS, UIS ruggedness is better than the sum of its two transistors. Specifically, the energy that parallel transistors of low Δ-BVDSS can sustain depends on the peak current and is 10%-20% higher than the sum of the energies of the individual transistors. We explain the physical mechanism of this effect and extend the concept to the case of more than 2 parallel transistors. These findings are important for the efficient design of power circuits with multiple die in parallel.

UIS Ruggedness of a Pair of Parallel MOSFETs

We performed ramp to breakdown UIS stress tests by means of a successive increase of the inductance L (L-ramp) for given peak currents. Fig. 1 shows the UIS ruggedness of Wolfspeed's C3M0075120 (1200V, 20A) MOSFETs [1] as a function of Δ-BVDSS for five different peak currents through parallel pairs of FETs: 40A (magenta), 20A (blue), 10A (green), 8A (orange) and 7A(red). On the y-axis the failure energy per transistor is plotted. Solid lines show the fit to the data to actual measured failure energies (per FET, i.e. divided by 2). The dotted lines on the left show the failure energies for a single FET at half current of the pair, which is the expected value if both FETs dissipate energy equally. The dotted lines on the right show failure energies for a single FET at full current of the pair divided by 2, which is the expected value, if a single FET must dissipate the entire energy.

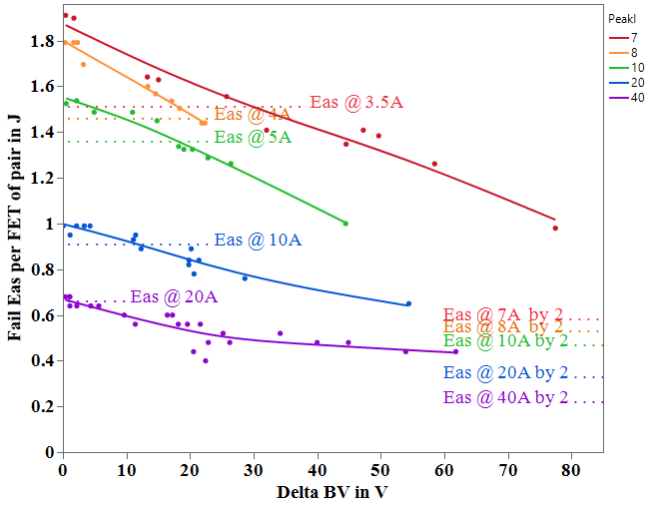

Fig.1. Failure energy per FET of pairs of FETs as a function of Δ-BVDSS for 5 peak (pair-) currents (magenta =40A, blue=20A, green=10A, orange=8A, red=7A). Dotted lines left show failure energies for single FET at half currents, dotted lines right show failure energies for single FET at full current (divided by 2).

We observe, that:

1.) The breakdown energy E depends on the peak current I_p and the difference between $\Delta V_{av}$of the individual FETs: E_{as} decreases with $I_p^{-0.6}$ and decreases with ΔV_{av} with a rate of approx. **10 mJ/V**
2.) For small Δ-BVDSS the solid lines exceed the dotted lines, i.e. the pair of parallel FETs can withstand an energy larger than the sum of two individual FETs.
3.) As $\Delta V_{av} \gg 0$ and E_{as} of the pair tapers off, the theoretical minimum is not reached by ΔV_{av}=60V

Before discussing these results of UIS ruggedness of a pair of parallel MOSFETs it is helpful to recapitulate the theory of UIS ruggedness of a single MOSFET as presented in [2]. The main failure mechanism is due to the thermal runaway and melting in the metallization (Aluminum) caused itself by the self-heating from the power dissipation in the MOSFET in avalanche. In [2] it was shown that this, together with a power law of $z_{th}(t)=t^q/\hat{c}$ for the transient thermal impedance z_{th}, leads to a relationship

$$E = \frac{(\Delta T_{crit}\tilde{c}(1+q))^{1/q}}{2q} V_{av}^{\,1-\frac{1}{q}} I_p^{\,1-\frac{1}{q}}, \quad (1)$$

whereby ΔT_{crit} is a critical junction temperature [3]. Figure 2 plots the relationship $E \sim I_p^{\kappa}$, whereby $\kappa=1-1/q$ for single FETs from C3M0075120. This plot explains the $E \leftrightarrow I_p$ observation listed above.

In order to explain the observed $E \leftrightarrow \Delta V_{av}$ relationship it is helpful to compare the waveforms of the individual FETs with waveforms of the pair for two cases: large and small ΔV_{av}.

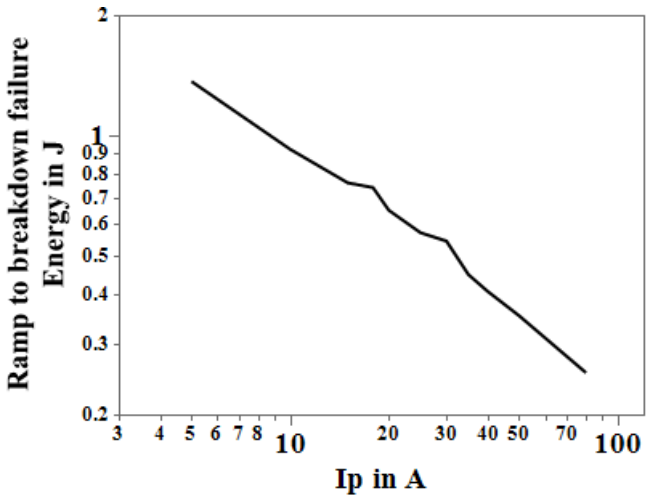

Fig. 2. Failure energies as a function of peak current I_p for C3M0075120.

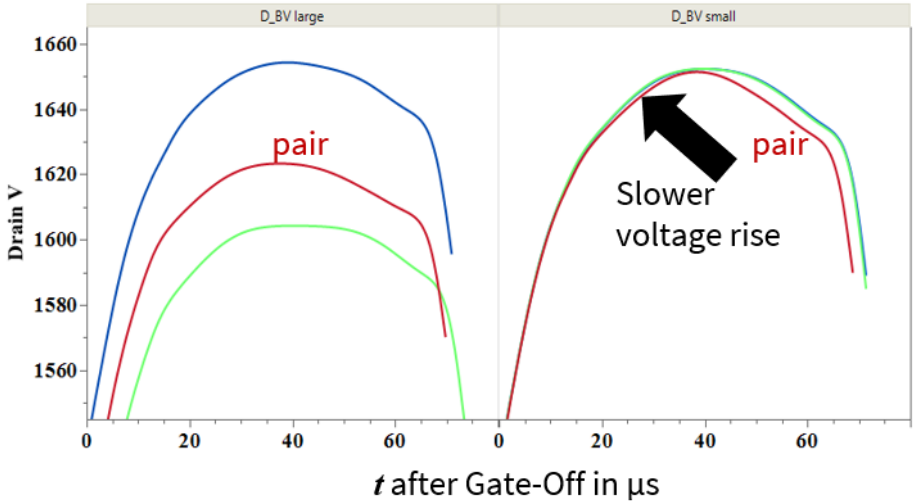

Fig. 3. Left: UIS waveforms of FET pairs with large Δ-BVDSS. Right: UIS waveforms of FET pair with small Δ-BVDSS; Blue: high BVDSS-FET, Green: Low BVDSS-FET, Red: FET pair.

Figure 3 plots these waveforms for the two cases of large and small ΔV_{av}: in blue the high BVDSS-FET, in green the low BVDSS-FET and in red the waveform of the FET pair. The waveform of the pair for small ΔV_{av} is almost identical to the waveforms of the single FETs indicating an almost equal share in dissipation of energy. The waveform of the pair for large ΔV_{av} is in the middle between the single FET waveforms indicating that both FETs are in avalanche with the lower BVDSS FET dissipating more. This explains the expected decrease of E with ΔV_{av}.

Unexpectedly, the UIS ruggedness of a pair exceeds the sum of the two individual FETs. We refer again to the waveforms presented in figure 3. On close observation, it can be seen, that the waveform of the pair rises slightly slower and has a slightly lower peak voltage and earlier finish. The root cause lies in the positive avalanche temperature coefficient [4], which leads to a thermal balancing: As one FET heats up, its ΔV_{av} increases and it thus offloads current to the other FET.

This result can also be discussed in the framework of the above-mentioned model for UIS ruggedness [2]. According to the link established between the transient thermal impedance $z_{th}(t)=t^{q}/\hat{c}$ and the energy versus peak current relationship $E \sim I_p^{\kappa}$ with $\kappa=1-1/q$, a smaller q comes along with a steeper slope in the $E \leftrightarrow I_p$ relationship. Figure 4 illustrates this. The data from figure 1 is replotted as a function of I_p, parameterized by ΔV_{av} with different colors It can be seen, that the slope of the pairs is steeper than the slope of the single FET (black curve as in figure 2).

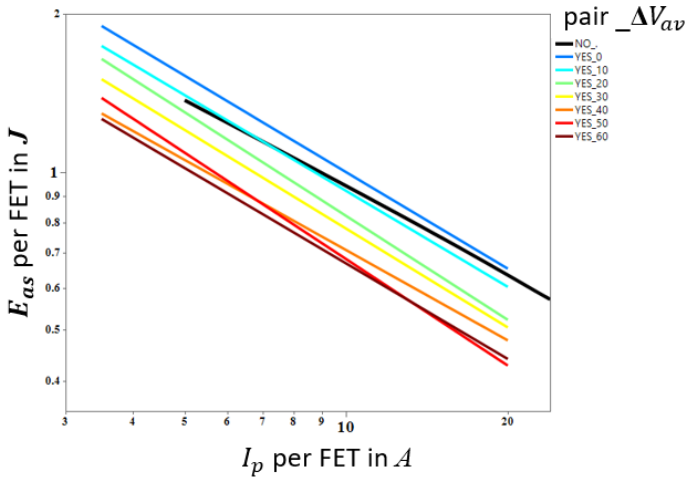

Fig. 4. $\mathbf{E \leftrightarrow I_p}$ curves for different $\mathbf{\Delta V_{av}}$, extracted from figure 1.

This result can be illustrated in yet a different manner. As shown in [2], it is possible to extract z_{th} and subsequently q directly from the waveform $V(t)$:

$$z_{th}(t) = \frac{1}{TC_{BV} V_{av} I_p}\left(\frac{V(t)-V(0)}{V(0)} + \left(\frac{\bar{V}-V(0)}{V(0)} + \frac{R_s I_p}{\bar{V}}\right)\left(e^{\frac{\bar{V}}{\tau_{av} V(0)} t} - 1\right)\right) \quad (2)$$

where TC_{BV} is the temperature coefficient of the avalanche voltage, R_s is the series resistance of the current path (extracted alongside with q) and τ_{av} is the time in avalanche. Figure 5 plots on the left the relationship $\kappa=1-1/q$ and illustrates that a smaller q leads to a more negative κ and thus a steeper $E \sim I_p^{\kappa}$ relationship. On the right the q-exponents of the individual FETs vs. the q-exponents of the pairs extracted according to the formula above (Green: 10A on the pair, Blue: 20A; Pluses and Dots refer to the 1st and 2nd FET). For most devices the individual q-s are larger than the q-s of the pair. According to (1) E scales inversely with q-s.

UIS Ruggedness of Four Parallel MOSFETs

Finally, we present data for four FETs in parallel. Figure 6 shows the data arranged in a similar fashion as in figure 1. The conclusions for the 4 FETs case are the same as for the 2 FETs case.

Conclusions

In conclusion, we present data for UIS ruggedness of 4H-SiC MOSFETs in parallel. We show its dependency on peak current and the difference in breakdown voltage of the single FETs. We show and explain that for sufficiently small Δ-BVDSS the UIS ruggedness of a pair of parallel pairs of FETs surpasses the sum of the ruggedness of the individual transistors. Effective binning of FETs by BVDSS can be chosen very generously or is unnecessary when designing for UIS robustness.

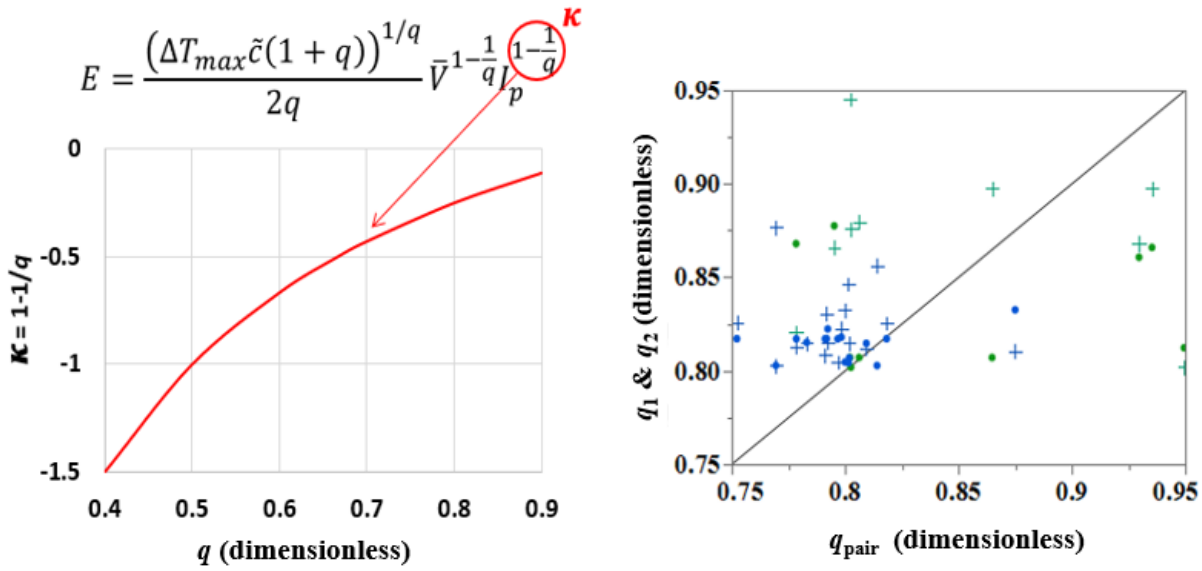

Fig. 5. Relationship between the exponent κ from E(Ip) and the exponent q of zth(t)=t q/ĉ as described in [2] Right: q of the individual FETs vs. q of the pair. Green: 10A on the pair, Blue: 20A; Pluses, Dots refer to the 1st and 2nd FET.

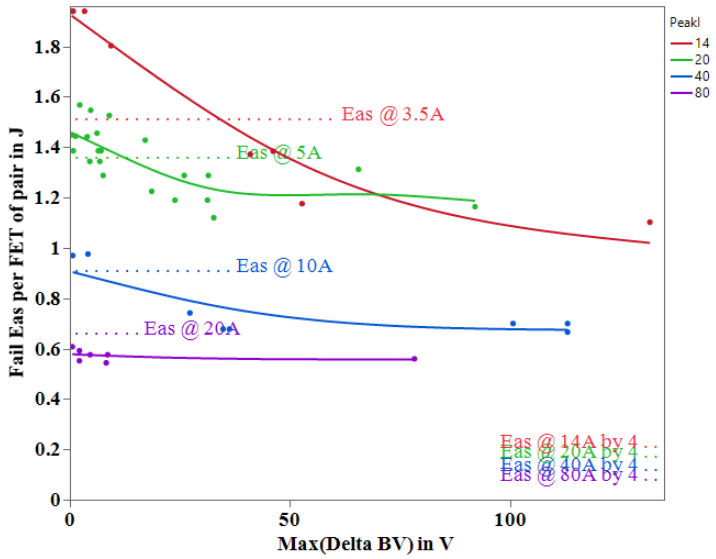

Fig. 6. Failure energy per FET of quads of FETs as a function of Δ-BVDSS for 4 peak (pair-) currents (magenta=80A, blue=40A, green=20A, red=14A). Dotted lines left show failure energies for single FET at half currents, dotted lines right show failure energies for single FET at full current (divided by 4).

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