

Reliability of SiC MOSFETs in the High Cycle Fatigue Regime under Fast Power Pulses

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Keywords: Power cycling, reliability, silicon carbide, high cycle fatigue, 3D simulation

Abstract. Device reliability is an important factor in application, especially in the field of electric mobility. In this paper high cycle fatigue power cycling results of SiC devices in baseplate free modules are presented. To minimize testing time, the devices were stressed with load pulses corresponding to a 50 Hz load. The reliability results are the first fatigue results for temperature swings below 30 K for SiC devices. The lifetime in the high cycle fatigue area is limited by solder fatigue for high virtual junction temperatures of 150 °C. In theory, the reliability should increase exponential since the elastic-plastic transition area is reached. The experiment revealed that the lifetime can still be described by the Coffin-Manson approach also in the high cycle fatigue area. It can be observed that the high junction temperatures weaken the stability of the solder layer, so no major lifetime increase can develop. The measured temperature data are additionally corrected by a three-dimensional (3D) simulation to ensure a validity of the results.

Introduction

The weaker reliability of SiC devices compared to its silicon counterparts is an often discussed topic especially for the gate oxide [1] and the power cycling capability in classical power module technologies [2], [3]. These drawbacks and the higher costs are an obstacle for a broader market share. Previous work showed that silicon devices can have a significantly increase in lifetime when tested for certain high cycle fatigue conditions [4], [5]. This effect might boost the lifetime in applications where only small temperature ripples respectively deformation rates are expected. The phenomenon could also positively influence the reliability assessment of SiC devices. Investigations in [6] also observed an increasing lifetime, when the temperature swing is below $\Delta T = 50$ K and a low $T_{vj,min}$ of 20 °C is applied. The investigation in this paper should fill a white spot in lifetime testing, presenting results in the range of $\Delta T < 35$ K.

Experimental Setup

Testing in the high cycle fatigue regime requires some modifications compared to a standardized test approach like IEC 60749-34 [7]. For a high cycle fatigue test, a large number of power cycles is expected. To minimize the test duration, the cycling time is decreased to 20 ms. To still reach high acceleration factors with standard equipment, the load current can be increased to add more conduction losses. This is disadvantageous because increasing the load current above the rated current might overstress sensible packaging structures like bond wires. Early failures caused by overstressing or to high acceleration factors would be the result, instead of wear-out failures like described in bathtub curves [8]. To circumvent this problem, the chips are not only heated by conduction but also with switching losses.

Fig. 1. shows the schematic advanced setup for the power cycling tester with switching losses. The total system contains four devices under test in two separate phases. Each phase consists of two branches. When the devices are heated, the load current is toggled with high frequency between the branches to generate switching losses by hard turn-off against the inductance L_x . A boosted active

clamping circuit (BAC) is used to limit the drain-source voltage across the DUT to stay inside the safe operation area.

A single turn of event for the device under test SiC-MOSFET type 45 mΩ/1.2 kV can be found in Fig. 2. The maximum drain-source voltage is limited to approx. 400 V for 20 A load current resulting in approx. 6.3 mJ turn off energy per single turn off event. The clamping and the gate voltage are oscillating a little bit, but do not influence the test result. The switching losses lead to a superimposed temperature ripple of approx. 2 Kelvin when calculating with an adiabatic approach for the die.

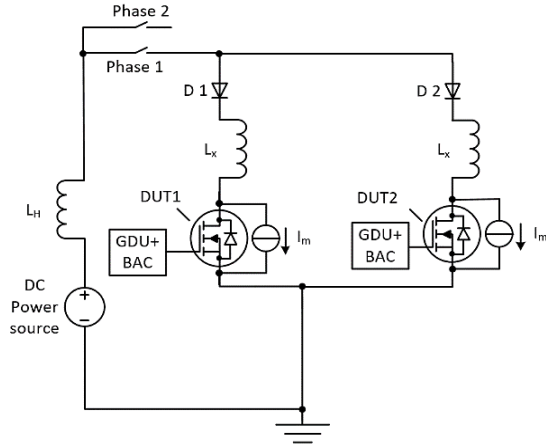


Fig. 1. Detailed switching topology for phase one of the advanced power cycling concept with switching and conduction losses.

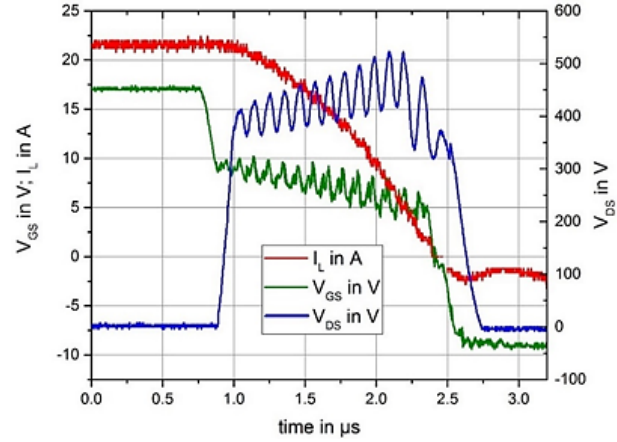


Fig. 2. Single turn-off event with gate-source and drain-source voltage and load current in red with clamping time of approx. 1.5 μs.

An exemplary simulated temperature ripple for $t_{on} = 10$ ms under thermal stable conditions is presented in Fig. 3. A total of five power cycling swings is simulated, while the system is already in a thermal stable condition. The test approach allows the applicability with the same measurement strategies and timings for determining temperature and thermal resistance like with standard power cycling test equipment. Especially, the temperature determination with the $V_{SD}(T)$ method is applied, the calibration function of V_{SD} is shown in Fig. 4, determining the temperature with the pn-junction of the inverse body diode at closed n-channel. This allows highest precision temperature determination and comparability to standard test results.

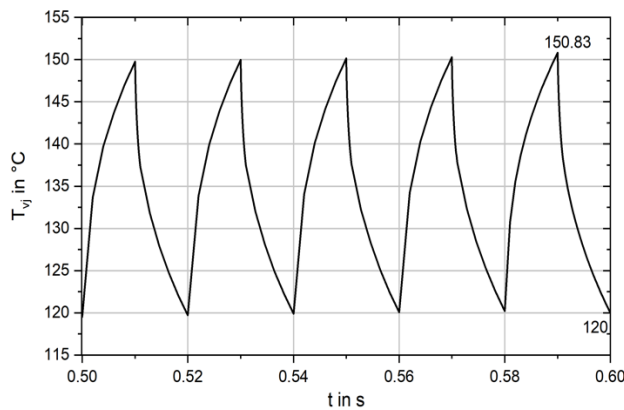


Fig. 3. Simulated temperature ripple of the junction temperature T_{vj} for the test conditions for test 1 in Table 1.

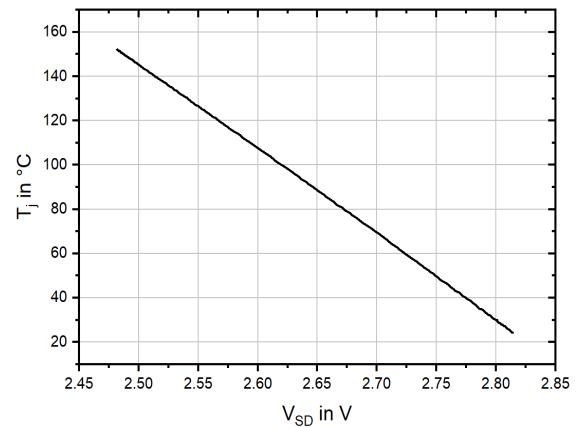


Fig. 4. $V_{SD}(T)$ calibration curve for 100 mA measurement current.

Only in the heating phase the devices under test are actively switched, adding an adjustable portion of switching losses to the device. The amount of switching losses can be adjusted with the value of the inductance L_x or with the switching frequency [9]. More detailed information about the test approach can be found in [9]. In previous testing, the test strategy showed equal results compared to a standard approach for the failure modes bond wire lift-off and solder fatigue [10].

Design of Experiments and Results

Two tests were performed with a total runtime of more than 200 days. Detailed test settings are displayed in Table 1.

Table 1. Detailed test settings for test 1 and 2.

Parameter	Test settings	
	FS45MR12W1M1 B11 Easy-pack	
	Test 1	Test 2
ΔT (raw)/ ΔT (corrected)	30 K / 34 K	22 K / 25 K
$T_{vj,max}$ (raw)/ $T_{vj,max}$ (corrected)	150 °C / 154 °C	150 °C / 153 °C
$t_{on} = t_{off}$	10 ms	10 ms
I_{load}	20.3 A	20.2 A
f_{switch}	23 kHz	16.5 kHz
Switching losses ratio	57 %	36 %

The design of experiments aimed for a first verification test with a $\Delta T = 30$ K. In this regime it is expected that still a decent amount of plastic strain will lead to fatigue. The second test targets more the expected elastic dominated zone. The cycle time, load current and the maximum junction temperature $T_{vj,max}$ were kept constant for both tests. With a different ratio of switching losses respectively the switching frequency, the temperature swing was adjusted. The power loss density is with ~ 10 W/mm² for test 1 and ~ 6 W/mm² for test 2 noticeable higher compared to application.

The main failure mode is an increase of the thermal resistance of +20 %. The development is displayed in Fig. 5 for test 1 and Fig. 6 for test 2. The failure relates to chip solder fatigue. In test 1, a not optimized dummy device was used after failure of DUT 3 (blue) which lead to oscillations for the other devices, but did not overall influence the lifetime determination.

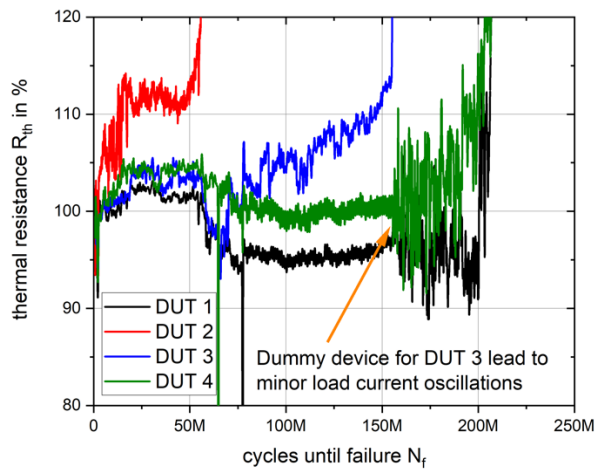


Fig. 5. Development of the thermal resistance $R_{th,junction}$ to case in % in dependency of cycles until failure N_f for test 1.

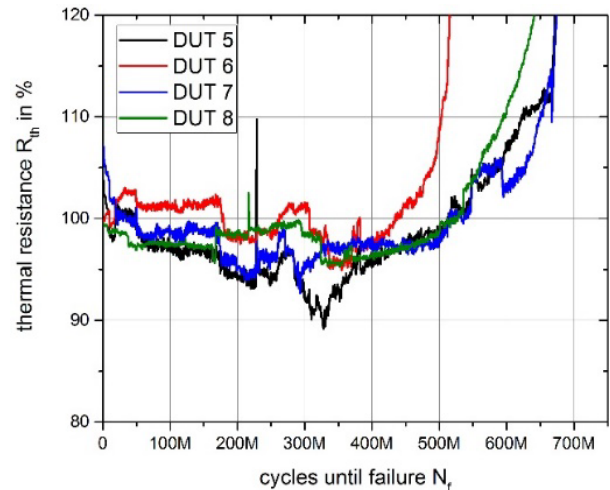


Fig. 6. Development of the thermal resistance $R_{th,junction}$ to case in % in dependency of cycles until failure N_f for test 2.

Close to end-of-life at elevated temperatures also some bond lift-offs are visible. Scanning acoustic microscopy (SAM) showed that the degradation started in the center of the solder layer, which is expected for this high power loss density (see Fig. 7 left). Fig. 7 right shows no information of the health state of the bond wires, since the damage to the solder layer is high. The signal is reflected by the cracks in the chip solder layer and can therefore not reach the bond interconnection area.

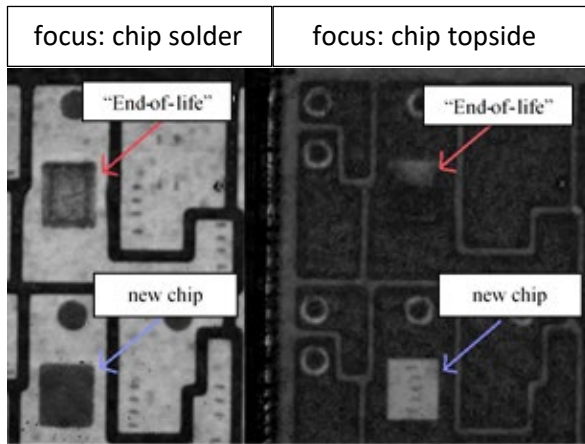


Fig. 7. SAM investigation with comparison between stressed and new system with the very strong solder degradation of the tested system.

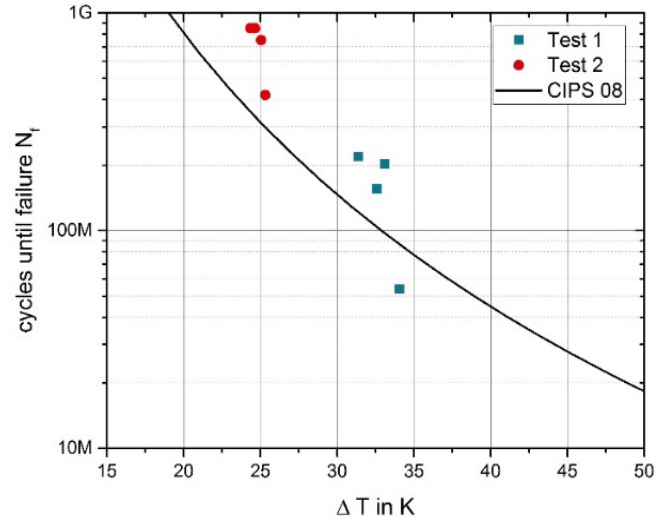


Fig. 8. Development of the thermal resistance R_{th} junction to case in % in dependency of cycles until failure N_f for test 1 and test 2 in relation to an adapted CIPS 08 model.

The lifetime results depending on the ΔT are shown in Fig. 8. As reference the CIPS 08 [11] lifetime expectation with an adjusted base lifetime to $K = 1.7 \cdot 10^{15}$ is given as guide for the eye. It can be seen that the lifetime even for test 2 shows good agreement with the trend of the standard lifetime expectation. It can therefore be stated that the reliability for the tested conditions can be described with a Coffin-Manson approach. It is expected that the relatively high junction temperature of $T_{vj,max} = 150^\circ\text{C}$ weakens the mechanical stability of the solder connection. Hence, no exponential increase of the lifetime can be observed. Similar dependencies were found for Si devices in [12].

Simulation Modelling

Since the experiment always contains a temperature measurement error due to the delay time after current turn-off, a 3D-simulation was carried out to correct the experimental data. In addition, there is further information on the temperature distribution and the physical degradation effects.

The full model is a standard baseplate-free packaging technology with the material data and layer thicknesses in Table 2.

Table 2. Material data and geometry for the simulation.

Layer	Material	Thickness
bond wire ($\varnothing 400 \mu\text{m}$)	aluminum	$\varnothing 400 \mu\text{m}$
metallization	aluminum	$4 \mu\text{m}$
chip	silicon carbide	$110 \mu\text{m}$
	epitaxy	$10 \mu\text{m}$
	substrate	$100 \mu\text{m}$
chip solder	Sn96Ag3.5Cu0.5	$50 \mu\text{m}$
DCB top	copper	$400 \mu\text{m}$
ceramic	Al_2O_3	$700 \mu\text{m}$
DCB bottom	copper	$400 \mu\text{m}$
TIM	Dow corning 340	$50 \mu\text{m}$
heat sink	copper	10 mm

The temperature dependency of the materials was included. Results of the thermal simulation are presented in Fig. 9 for $T_{vj,max}$ and Fig. 10 for $T_{vj,min}$.

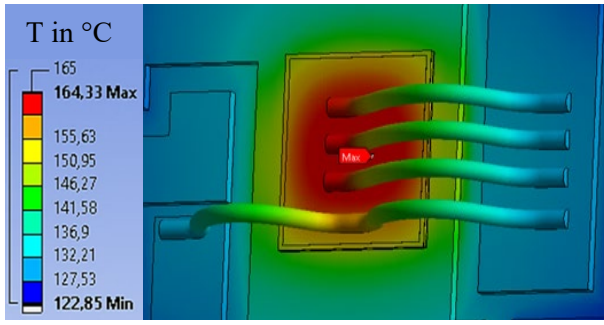


Fig. 9. Temperature distribution on the chip surface at the end of the warm-up phase ($T_{vj,max}$).

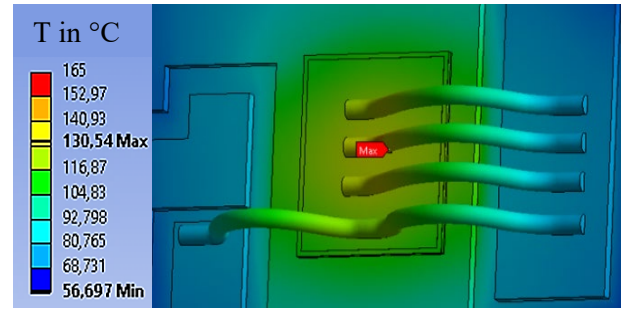


Fig. 10. Temperature distribution on the chip surface at the end of the cooling phase ($T_{vj,min}$).

Because of the high power density to reach $T_{vj,max}$ in a short on-time, a high temperature gradient of approx. 25 K can be observed between center and edge in Fig. 9, even though SiC has superior thermal conductivity (see also Fig. 11). The bond wires even allow a local reduction in temperature, even though the effect is small.

The measurement delay time to determine $T_{vj,max}$ is critical since the device will cool down already several Kelvin, which can influence the lifetime results especially for small temperature swings drastically [12]. The measured virtual junction temperature is correlating best with the area weighted average of the chip surface in the simulation [11]. In the simulation, a delay time correction of $\Delta T_{md} = 0.146 \cdot \Delta T$ was extracted. This leads to a correction of 4.4 K for the test 1 conditions at $\Delta T = 30$ K temperature swing. A second option would be a calculation with the square-root-(t) method [13]

$$\Delta T_{md} = \frac{2 \cdot P}{A \cdot \sqrt{\pi \cdot c \cdot \rho \cdot \lambda}} \cdot t^{\frac{1}{2}} \quad (1)$$

while using $P/A = 9.84$ W/mm² (test 1), $c = 750$ J/K, $\lambda = 263$ W/mK, $\rho = 3210$ kg/m³ and $t = 140$ μ s, a temperature error of $\Delta T_{md} = 5.2$ K is calculated. Both results are quite close to each other. The simulation is expected to be more precise since all surrounding layers and materials have been considered. All experimental results of the previous section are temperature corrected by the simulation values in this section, to ensure stable precision of the measurement results.

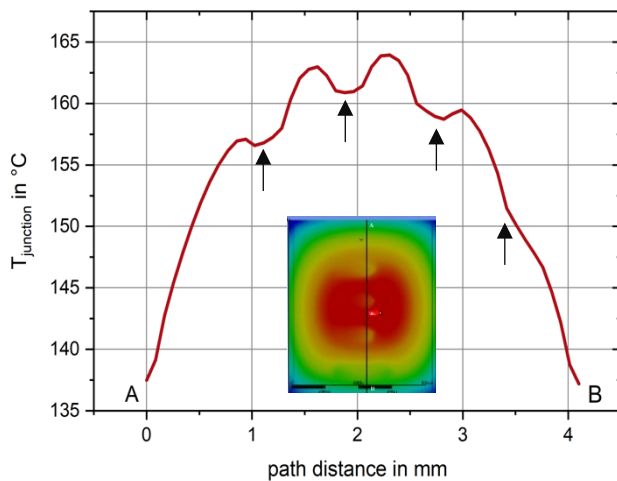


Fig. 11. Temperature distribution along a linear evaluation path for $T_{vj,max}$ on the topside of the chip crossing all four marked bond stitches.

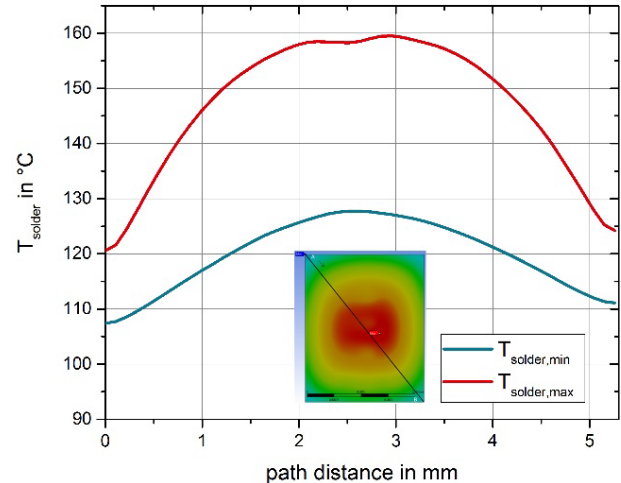


Fig. 12. Temperature distribution along an diagonal evaluation path for $T_{solder,max}$ and $T_{solder,min}$ on the topside of the solder layer.

Also the failure location was investigated. The temperature trend on the topside of the solder layer is displayed in Fig. 12. The temperature $T_{solder,max}$ after the heating phase is shown in red while the $T_{solder,min}$ after cooling is in blue. The maximum local ΔT occurs in the center of the system with approx. 32 K while on the edge the local ΔT is below 15 K. This can explain the starting fatigue in the center area because the highest strain occurs in that zone.

Conclusion

In this work an advanced power cycling strategy was applied to test the reliability of commercially available SiC MOSFETs in a baseplate-free package. For testing low temperature swings or in general at conditions in the high cycle fatigue zone, the cycle time is reduced to 20 ms. The results show a minor increase in lifetime by approaching $\Delta T \approx 25$ K, but an elastic range cannot be stated clearly when testing at high maximum junction temperatures ($T_{vj,max} = 150$ °C). The widely known Coffin-Manson approach still seems applicable. Taking the results from Silicon devices into account [12] it is expected to observe a possible transition to the elastic zone at lower $T_{vj,max}$ for a soft soldered die attach. This needs to be proven in a further study.

The thermal-electrical simulation was used for temperature correction, to avoid the measurement delay time error. It also confirms the findings from the failure analysis where the most damage occurs in the center of the solder layer for this application close testing conditions.

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