Solid State Phenomena
ISSN: 1662-9779, Vol. 361, pp 71-76
doi:10.4028/p-O7afLP

Submitted: 2023-09-22
Revised: 2024-04-24
Accepted: 2024-04-24
Online: 2024-08-26

The Impact of Gamma Irradiation on 4H-SiC Bipolar Junction Inverters under Various Biasing Conditions

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Keywords: Gamma Radiation, Co-60, Bipolar Transistor, Inverter, TTL, Enhanced Dose-Rate Sensitivity, Critical Regime

Abstract. In this study, we introduce the impact of gamma irradiation on 4H-SiC based transistor-transistor logic (TTL) inverters. These monolithic bipolar inverters have been successfully demonstrated in a broad spectrum of temperature and supply voltage conditions. In this iteration of experiments, attempts made to the processing to increase beta values. The gamma radiation tests from a ^{60}Co source were conducted under various operation conditions and measured in-situ under different biasing conditions. The Silicon Carbide Integrated circuits (SiC ICs) show excellent tolerance properties to gamma radiation up to doses of nearly 1 MRad. Comparable Si BJT-based TTL inverters show considerable degradation already at one order of magnitude lower doses, clearly demonstrating the superior radiation hardness of 4H-SiC ICs.

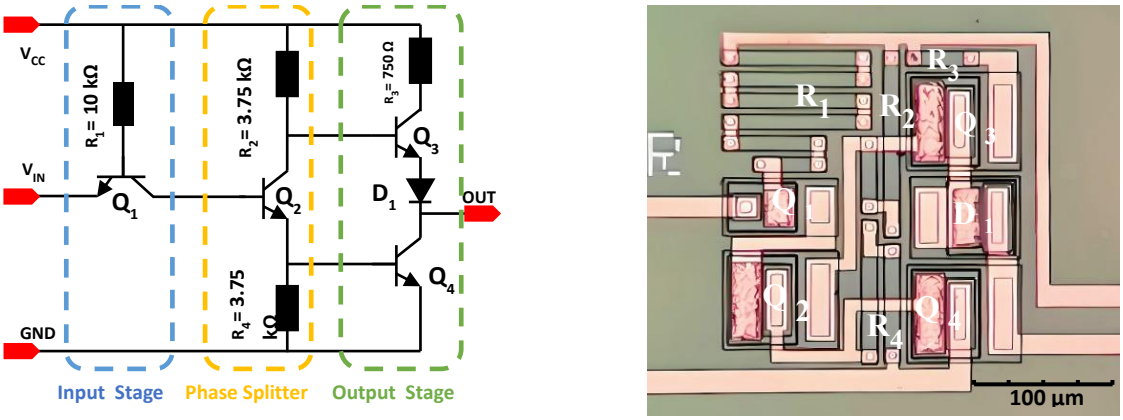
Introduction

An inverter performs a simple and essential logic operation known as a "complementary" or "NOT" operation. It takes an input signal (logic 0 or logic 1) and produces the opposite output (if the input is 0, the output is 1, and vice versa) and this operation is fundamental for building more complex logic functions. Logic circuits and ICs exposed to harsh environments, such as space, where radiation is an issue, may behave very differently than under normal conditions and, furthermore, the behavior of an inverter under radiation exposure differs significantly from that of a single transistor, hence necessitating further investigation.

A schematic for the 4H-SiC based TTL inverter used for the irradiation studies in the present work is shown in Figure 1 (a).

The inverter circuit has three distinct stages. The initial stage is referred to as the "Input Stage," which incorporates a single-emitter transistor. In a multiple input NAND gate this transistor would have multiple emitters but for these tests the simplest possible circuit was used. Subsequently, there is the "Phase splitter" stage, where a transistor functions as a switch to bifurcate the phase into binary values, namely 0 and 1. Finally, the "Output stage" encompasses two transistors, both of which operate in a mutually exclusive manner within a totem-pole configuration, alternating between the logic high and logic low states (1 = 10 V, 0 = 0 V).

In scenarios where the input combination is V_{cc}=15 V and V_{in}=0 V, the transistor Q_1 remains in the "on" state, causing Q_2 to be in the "off" state. This configuration effectively divides the phase into a logic 1 at the collector and a logic 0 at the emitter, resulting in Q_3 being in the "on" state and Q_4 being in the "off" state, ultimately yielding an output of 1. Due to two pn junction voltage drops (Q3 and D1), the output voltage is 10 V rather than the supply voltage of 15 V, but this is also the case for silicon TTL circuits.



(a) (b)

Fig. 1. The schematic diagram of the IC based on TTL logic (a). A photograph of the processed inverter (b).

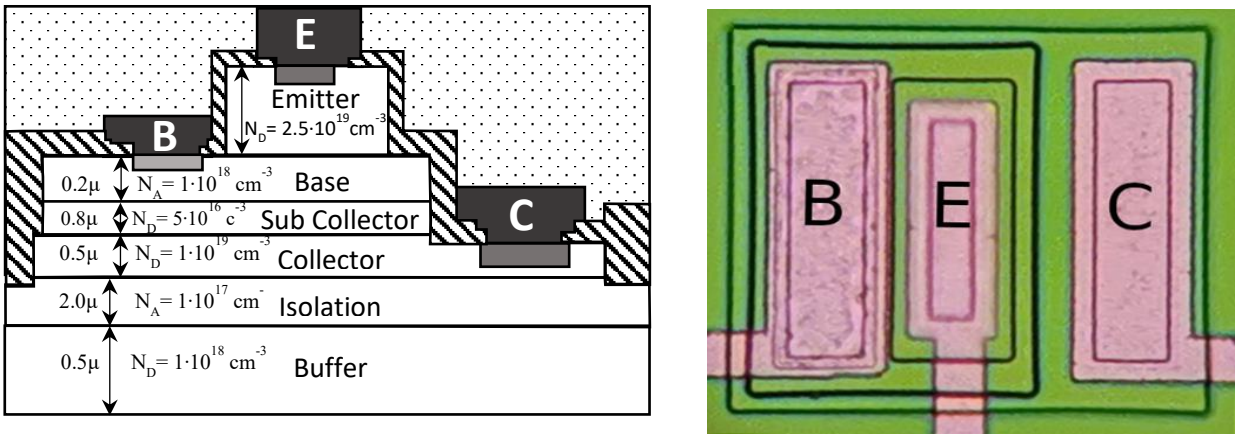
Conversely, when the input combination is V_{cc}=15V V_{in}= 15 V, the emitter-base junction of Q_1 becomes reverse-biased, causing it to operate in reverse active mode. As a result, the phase splitter Q_2 alters the collector to logic 0 and the emitter to logic 1. Consequently, transistor Q_3 switches to the "off" state, while Q_4 switches to the "on" state, resulting in the final output being at logic 0, or close to 0V.

Processing

The SiC bipolar devices and integrated circuits are produced at the MyFab Electrum Laboratory located in KTH, Kista, Sweden. The manufacturing process follows a procedure that replicates the steps outlined in the mentioned process description [1-3].

The initial material used for the processing was 100 mm 4° off-axis 4H SiC n-type conducting wafers from Cree™. These wafers feature multiple epitaxial layers by that were grown in a single sequence to reduce interface states between epitaxial layers. The cross-sectional structure of a single transistor is shown in Fig. 2.

The first epitaxial layer, known as the Buffer Layer, is used to minimize the amount of defects during epi-growth. Subsequently, the Isolation Layer, serves to effectively segregate individual devices, thanks to its substantial p-type doping concentration. The remaining layers follow a standard design for low-voltage bipolar transistors: n^+ collector for contacts, a lower doped sub-collector that blocks the voltage, a medium doped p-base, and a highly doped n^+ emitter to finish off.



(a) (b)

Fig. 2. A schematic cross-section of the transistor, with the substrate and the different epitaxial layers (a) and the view from the top (b). Not to scale.

The buried collector layers are strategically positioned to establish low-resistance ohmic contact for the lightly doped intrinsic collector layers situated above it. The doping level and thickness of the subsequent base layer play a pivotal role in determining the device's gain, while the lightly doped drift collector layers is the key factor influencing the device's breakdown voltage. The top layer is the highly doped Emitter layer. This layer significantly enhances emitter injection efficiency and simultaneously reduces contact resistance, contributing to the overall performance of the device.
The NPN transistors undergo a fabrication process involving three dry etching steps, each serving to isolate the Emitter, Base, and Collector regions, respectively. Due to the TTL logic architecture, only NPN transistors are needed.
The diode in the schematic is a NPN transistor with its collector shorted to the base, to ensure that the diode voltage drop is the same as the base-emitter voltage drop. In the context of the present research, it is important to clarify that the sacrificial thermal oxidation step is undertaken to eliminate approximately 10 nm of damaged SiC resulting from the dry etching procedure. The entire surface is passivated by an PCVD oxide layer, which is subsequently annealed in an N_2O environment.

Radiation Facility and Conditions

Gamma radiation tests were conducted at the ^{60}Co Calliope facility, situated within the ENEA Casaccia Research Center in Rome, Italy. Calliope has a pool-type irradiation plant that houses a ^{60}Co source within a spacious, shielded cell measuring 7.0 m x 6.0 m x 3.9 m. The facility's maximum authorized activity stands at 3.7 x 10^{15} Bq (100 kCi), with the current activity as to 1.4 x 10^{15} Bq (38 kCi). The plane source rack comprises 25 rods of ^{60}Co, with a total active area of 41 cm x 75 cm. The radiation emitted from these sources consists of two photons, measuring 1.17 and 1.33 MeV, with a mean energy of 1.25 MeV. Notably, the irradiated material remains non-activated, allowing for immediate handling following the conclusion of the irradiation test. Within the Calliope facility, various dosimetry systems and instruments for samples characterization and treatment are available. For these irradiation tests involving BJTs, the ESR-alanine dosimetry method was employed [4].
SiC BJTs were tested across a range of gamma-ray doses and dose rates (HRD = 124.5 Rad/s, NRD = 49.48 Rad/s, and LRD = 9.975 Rad/s). An Al/Pb filter was used in front of the samples during radiation to mimic space conditions by removing low-energy secondary photon components. During radiation the samples were biased in one of three conditions: V_{CC} = V_{in} = 15 V, V_{CC} = 15 V, V_{in} = 0 V, or V_{CC} = V_{in} = 0V.

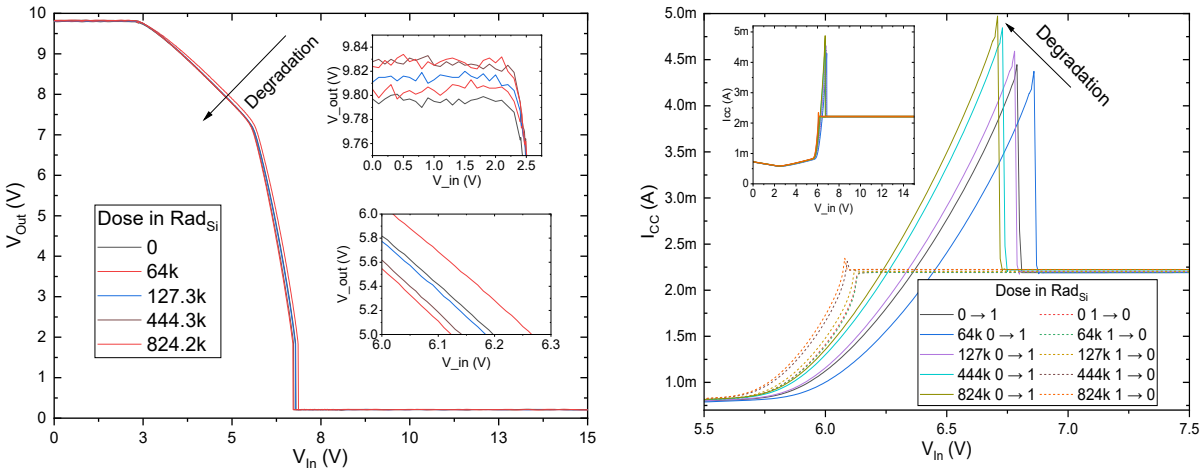
Measurement Procedure

The SiC bipolar devices underwent thorough testing in line with semiconductor device standards, including MIL-STD-883L and MIL-STD-750 (Method 1019.9) [5, 6]. To assess gamma radiation effects in real-time, a remote setup enabled device operation in different states, with immediate in-situ characterization after each exposure, offering a more accurate representation than previous studies.
National Instruments™ equipment was used for electrical tests, with remote measurements and shielding to counter radiation-induced noise. Calibration and precision measures increased the testing time but ensured accuracy.
The inverters underwent rigorous analog regime testing in a harsh environment, necessitating the use of long lines. The test program was configured to accommodate the effect of the long lines, by using the sense mode for each of the measurement units. Line calibration was conducted during each iteration between the radiation and measurement. In order to reduce the potential effect of the induced charge in the lines, the iteration timing was carefully adjusted to ensure that the exposure duration exceeded the measurement time by at least a factor of ten.
DC characteristics were measured using a common method. V_{CC} was held at 15 V, while V_{in} varied from 0 to 15 V with a “trimmed mean” [7] used for noise reduction. This method yielded satisfactory resolution even with long cables. Bidirectional sweeps were performed, from logic zero (0 V), to logic one (15 V), and then back from one to zero.

Output Signal and Experiment Results

The primary attributes of the inverter during the work are output signals levels and supply currents, which respectively encompass its efficacy in signal inversion and power efficiency. These criteria is the most important, particularly in the context of radiation testing. Figure 3 presents the transient characteristics of the 4H-SiC TTL inverter for different absorbed doses.

As evident from the graphs, there are slight fluctuations (see the insets of Fig. 3 (a)) in the output signal in the transfer characteristics as the accumulated dose increases, but the general trend is that the inverters are only slightly affected even up to doses of nearly 1 MRad. To explain, we notice that the output behavior slightly shifts towards lower values of V_{in} (see Fig.3 (a)). This shift indicates that the transition between Q_3 and Q_1 takes place at the lower voltages, which is most likely caused by the induced charge in the Base-Collector region of Q_1 transistor.



(a) (b)

Fig. 3. Measured transfer characteristics of SiC Inverter. (a) Voltage output characteristic V_{out} (V), (b) Supply Current I_{cc} (A) for input voltages between 0 and 15 V (inset) and magnified for 5.5 to 7.5 V.

We can also notice that the logic high level (1) is slightly reduced, which is unusual for similar ICs fabricated in silicon. Usually, in silicon inverters, the logic low levels (0) and the IC's power supply current are affected the most, not the transition point between 1 and 0, but we don't observe such behavior in the SiC IC.

From the perspective of ICs investigation under the radiation exposure, circuit power consumption is of greater interest (see Fig.3 (b)). In the legend for each dose level, there are two curves, representing the transition between low and high logic states (0 → 1 and 1 → 0) corresponding to different sweep directions of the input voltage. There is a distinct peak (see Fig.3(b)) for each of the doses for the sweep 0 → 1, which is a normal behavior of the circuit. Current consumption doubles temporarily, which is an effect of situation when Q_3 is still partially on while the Q1-Q2-Q4 circuit is also beginning to turn on.

The phenomena described above is similar to the "Crowbar Curren" effect [8] in CMOS inverters. It is worth discussing the dynamics of the peak shifting from logic low to high levels. The steady state current consumption when the input is at 0 or 1 is unchanged by the radiation.

Circuit simulations with SPICE (LTSpice) shows that a degradation process occurs in all transistors within the base-emitter region. This leads to an earlier onset of current flow in the Q_1 - Q_2 region and subsequent switching. A similar process explains the behavior in transistor Q_3, resulting in an increase in spike amplitude as a function of absorbed dose (those that induce interface charge).

N. 32 samples were tested for three different dose rates, and three different bias conditions and the results are summarized in Figure 4. In all operation conditions of the ICs a similar (small) degradation of parameters is observed.

Discussion

Considering the results above described, the experiment does not detect a strong radiation effect in the 4H-SiC inverter for the absorbed gamma doses and the deviation from the initial performance is small, all less than 10% and most less than 5%. It is evident that as radiation intensity decreases, the dispersion increases (Figure 4), indicating a dependency on dose rate.

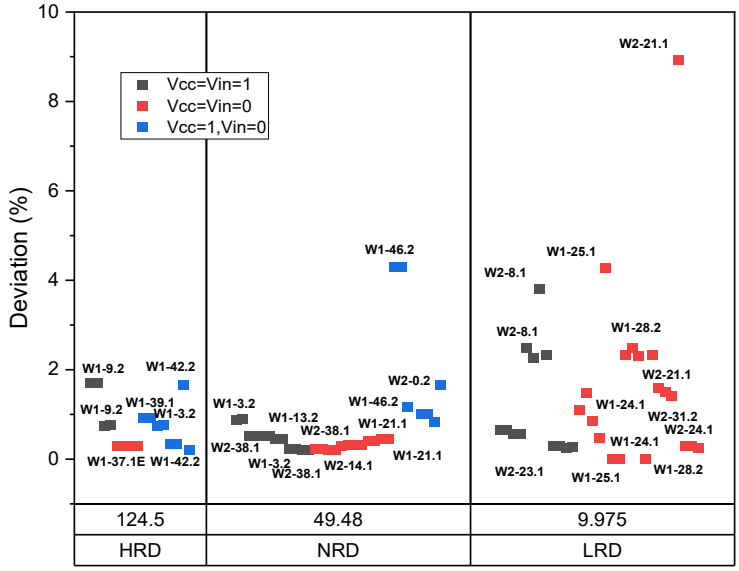


Fig. 4. Deviation of I_{cc} parameter in Relative units. Dose rates in units off Rad/s.

For comparison, Figure 5 includes some typical products from major manufacturers. It is evident that the radiation tolerance of silicon carbide ICs surpasses silicon-based ones by orders of magnitude.

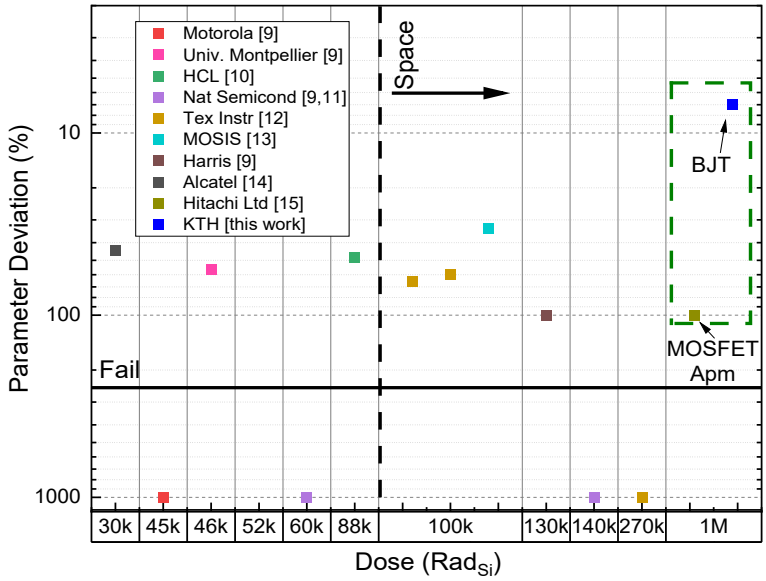


Fig. 5. Comparison of radiation resistance in Si vs. SiC inverters.

Conclusion

In this article, we have investigated the radiation tolerance of silicon carbide ICs operating on TTL logic. These circuits exhibit minimal degradation at gamma doses approaching 1 MRad (less than 10%). The critical mode of operation is the passive mode (V_{CC} = V_{in} = 0V), where the uniform accumulation of induced charge in the oxide and interface can potentially lead to premature IC triggering without a loss of logical levels. All of these findings make silicon carbide-based ICs outstanding candidates for replacing traditional silicon devices in applications involving harsh environments, such as space exploration, nuclear reactors, and medical equipment.

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