

Modelling-Augmented Failure Diagnostics in Planar SiC MOS Devices Using TDDB Measurements

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Abstract. In this study we analyzed the physical mechanisms governing time-dependent dielectric breakdown (TDDB) and we used TDDB physical model of dielectric breakdown, implemented in the defect-centric Ginestra® modeling platform, to deconvolute the intrinsic material properties effects and geometry feature impact on the gate oxide (GOx) and SiC-device breakdown.

Introduction

SiC has superior physical properties which make it an ideal material especially for power electronics applications, which require to operate at high voltages, high frequencies, and high temperatures [1]. Despite significant improvements in gate oxide reliability, the increased occurring probability of early failures in SiC devices remains one of the main challenges. For this reason, the understanding of time-dependent dielectric breakdown (TDDB) mechanisms is crucial for the reliability improvement of SiC-based power devices. As previously reported, the extrinsic breakdown leads to observation of the early failure tails in TDDB distributions which are attributed to gate oxide (GOx) fabrication and result in process-related defects [2-5]. Differently, the intrinsic (material inherent) GOx reliability depends on the physical breakdown strength of SiO₂, its preexisting electronic defects (defects that can trap and emit carriers – so called precursors defects) as well as on temperature and on the applied electric field. These defects are characterized with spatial and energetic position which is intimately connected with the dielectric strength. From intrinsic point of view, SiC based device exhibits similar intrinsic breakdown characteristics to Si equivalent [4]. In this study, we are investigating the role of the atomic defects, their entanglement with extrinsic factors of the breakdown and deconvolute their impact. To this aim, device simulations have been calibrated against experimental results. Initially, the time-zero defect constellation properties were determined by exploiting experimental current-voltage (IV) and capacitance-voltage (CV) measurements carried out on SiC capacitors. Afterwards, the intrinsic TDDB model (used in the simulations) has been calibrated and validated against experimental data. Finally, the statistical information on our experimental process variability have been used to reproduce the full (intrinsic-extrinsic) experimental TDDB distributions. The block diagram illustrating the flow of the study is reported in Fig. 1.

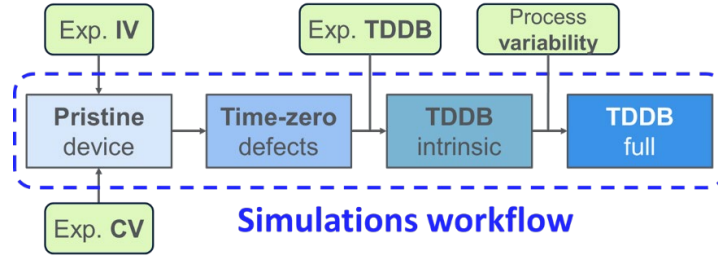


Fig. 1. Block diagram illustrating simulations workflow and its interplay with the experimental data.

Experimental Approach

Fabrication method. In this study, metal–oxide–semiconductor (MOS) capacitors of different sizes have been fabricated on 150 mm n-type 4° off-axis 4H-SiC (0001) epitaxial wafers with an epilayer thickness of 11.5 μm and an epilayer nitrogen-doping concentration of $7 \times 10^{15} \text{ cm}^{-3}$. After the conditioning of the SiC-surface, the gate oxide process with subsequent deposition of an in-situ n-doped polysilicon layer of 1200 nm was performed. The samples were processed with dry oxidation and NO-annealing at 1300 °C, with a nominal GOx thickness (t_{ox}) of 55 nm. As a final step, the polysilicon pads were structured using a photo resist mask and reactive ion etching. Further details about processing are reported in [6].

Electrical characterization. To monitor t_{ox} and extract the GOx capacitance, IV and CV measurements on MOS capacitors have been performed. In addition, TDDB data were collected using constant-current stress (CCS) method at three different current densities of 100, 120 and 150 mA/cm². Capacitors area was 0.0707 mm², and experiments were performed at room temperatures.

Simulation Framework

To simulate IV, CV and TDDB of 4H-SiC/SiO₂ MOS capacitors, the commercially available multiscale defect-centric simulation platform Ginestra® [7] has been used. More details on the application of this platform on various technologies can be found in following references [8-11]. For what concerns the transport through the dielectric, simulations self-consistently account for all the relevant charge transport mechanisms such as Fowler-Nordheim (FN) tunneling and trap-assisted tunneling (TAT). TAT properly describes carriers-phonons coupling and lattice relaxation processes occurring at defect sites, which are characterized by thermal ionization energies E_T and relaxation energies E_{REL} [12].

TDDB has been simulated by adopting the thermochemical (TC) model which attributes the generation of defects within the dielectric to the interaction between an external electric field and weak bonds, and which is suitable to describe the intrinsic breakdown dynamics of thick SiO₂ [4,13,14]. In the TC model, the generation rate G of oxygen vacancies associated to molecular bond breakage is a function of the local temperature T and electric field F

$$G \propto \exp\left(-\frac{E_A - p_0\left(\frac{2+\kappa}{3}\right)F}{k_B T}\right) \quad (1)$$

where κ is the SiO₂ relative dielectric constant, k_B is the Boltzmann's constant, E_A is the zero-field activation energy and p_0 is the molecular dipole moment. Power dissipation and temperature are calculated consistently with charge transport, allowing to model the field- and temperature-driven feedback that occurs during the BD process [15,16]. The stochastic nature of the process is accounted for using the Monte-Carlo method that determines the positions of the generated defects and defect distributions. Simulations have been carried out on 4H-SiC/SiO₂/poly-Si capacitors with a t_{ox} of 55 nm, as shown in Fig. 2a inset.

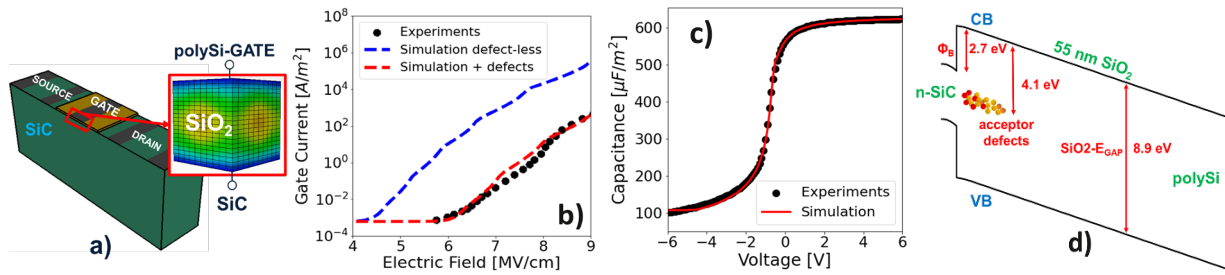


Fig. 2. a) Virtualization of a typical SiC planar MOS; the simulated stack is shown in the inset. b) Experimental vs. simulated current density as a function of the electric field. Trapped electrons locally modify the electrostatic potential, leading to an increase of the effective tunneling barrier Φ_B and significantly reducing the current compared to the defect-less case. Defects parameters are reported in Table I. c) Typical experimental and simulated CV curves at 10^4 Hz, which have been used for the extraction of the k-value, doping concentration, interface properties and for the uniformity screening of the test vehicle. d) Schematic band diagram of simulated 4H-SiC/SiO₂/poly-Si structure showing the defect distribution corresponding to the time-zero defect constellation and the 4H-SiC-SiO₂ barrier height Φ_B .

Table I. Physical parameters used in simulations.

Parameter	Value	Description
E_T	4.10 ± 0.35 eV	Acceptor thermal ionization energy
E_{REL}	0.30 eV	Acceptor relaxation energy
N_{DEF}	5×10^{19} cm ⁻³	Acceptor defect concentration
E_T	2.65 ± 0.35 eV	Vo thermal ionization energy
E_{REL}	0.34 eV	Vo relaxation energy
E_A	2.0 eV	TC Bond-breakage activation energy
p_0	6.5 eÅ	TC Molecular dipole moment

Results

A good agreement between experimental and simulated current vs. field characteristics has been obtained by implementing an acceptor defect distribution close to the SiC/SiO₂ interface using the defects parameters reported in Table I, as shown in Fig. 1b. Defects significantly reduce the current compared to the defect-less case. Namely, their occupancy increases with the electric field and trapped electrons enhance the effective SiC/SiO₂ tunneling barrier and so-called dielectric transparency in turn reducing the current.

CV characteristics were used for the extraction of the k-value, doping concentration and interfacial properties of the test vehicle (see, Fig. 2c). The schematic band diagram, corresponding to the time-zero defect constellation is depicted in Fig. 2d. Furthermore, CV measurements at 10^4 Hz were used for uniformity screening where the extracted process variation of the capacitance extracted at 5 V across the wafer is 0.83 ± 0.07 nF. After the calibration of IV and CV characteristics and obtaining of the time-zero defects inside the GOx, TDDb simulations have been compared with experiments. Fig. 3a shows typical simulated and measured voltage-time transients under the application of 50 mA/cm² CCS. Compared to the experimental transients, simulated curves exhibit abrupt but more discretized voltage steps (drops). This difference is due to the more precise sampling (small step, inherent to transient simulations) which is possible to define in simulation domain. In turn providing additional insights into the nature of the breakdown. Fig. 3b shows the oxygen vacancies (V_O) associated to the field-driven bond breakage which are randomly created across the SiO₂ layer at different stress times and the relative band diagram. V_O thermal ionization energy and relaxation energy are specified in Table I. When a defect cluster is formed, the current and the associated local power dissipation trigger positive feedback, leading to breakdown.

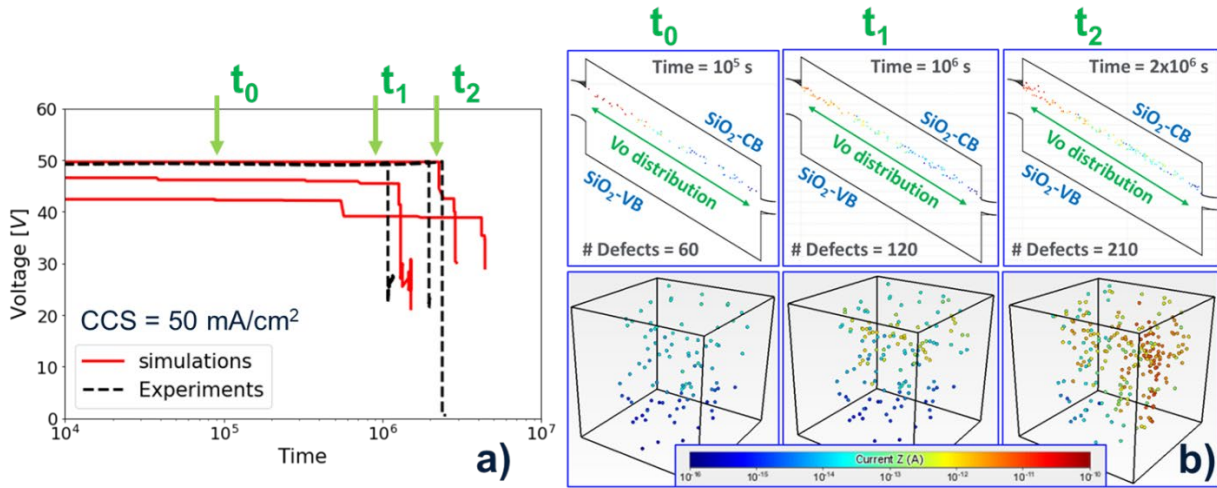


Fig. 3. a) Typical experimental and simulated voltage-time characteristics under a CCS of 50 mA/cm². b) Typical band diagram and device plots at three different stress times showing the oxygen vacancies defects V_O generation dynamics. During the stress, more and more defects are generated across the oxide layer, until breakdown is reached.

Kinetic Monte-Carlo (kMC) engine and discrete nature of the defects enable reproducing the data with the statistical significance. In Fig. 4a, simulated TDDB distributions are compared with experimental ones, which clearly exhibit a bimodal character. As expected, the intrinsic breakdown mode is captured with high accuracy by statistical simulations considering just the stochastic defect generation process reproduced by the kMC engine. To validate the intrinsic component of the breakdown, we compared simulations with experimental TDDB data of 15 nm Si/SiO₂ structures at different temperatures reported in [14]. The choice of using experimental data of Si MOSCAP structures for the intrinsic TDDB calibration was made in order to better capture intrinsic SiO₂ breakdown properties, excluding SiC-related failure mechanisms from the analysis. The intrinsic component of the failure was validated as the model clearly reproduced the measurements with statistical significance across the whole temperature range, as shown in Fig. 4b. It should be noted that the TC model parameters E_A and p_0 used in the simulations and specified in Table I agree with those reported in the literature [13]. Finally, we modeled the extrinsic TDDB tails associated to early failures by considering a statistical variation of t_{OX} from its nominal value through a normal distribution with a standard deviation of 4.5 nm as derived from the variability exhibit by the CV measurements. The result is shown in Fig. 4a, indicating that an accurate knowledge of process variability allows to explain and model early failure statistics, as well as to deconvolute the different contributions to TDDB.

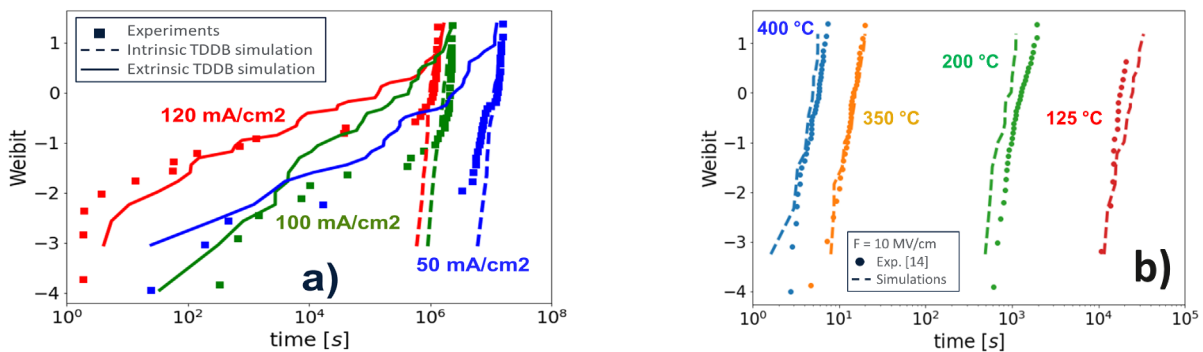


Fig. 4. a) Weibull plots of the measured (squares) and simulated (lines) time-to-breakdown at different CCS. Dashed lines represent default simulations with TC model, while solid lines are obtained if the random t_{OX} variation is accounted for. b) The validation of the intrinsic breakdown model has been obtained by comparing simulations with experimental TDDB data from the literature of 15 nm Si/SiO₂/poly-Si capacitors at different temperatures.

Conclusions

In this study we characterized the TDDDB of the SiC MOS capacitors and developed a model based on kMC simulations. Conducting defect spectroscopy on IV data, time-zero electronic defects properties were obtained. Initial defect constellation was used for development of the failure model which successfully captured the intrinsic breakdown at different temperatures as well as the extrinsic mechanisms and its impact on the bimodality of experimental TDDDB distributions. Statistical significance of developed physical model paves the path for the further improvements and understanding of the SiC/SiO₂ interfaces and premature failures and modeling-augmented diagnostics/metrology.

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