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SNDM Study of the MOS Interface State Densities on the 3C-SiC / 4H-SiC Stacked Structure

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Abstract. A stacked layer structure of 3C-SiC/ 4H-SiC has been implemented by simultaneous lateral epitaxy (SLE). The SLE, involving spontaneous nucleation of 3C-SiC(111) on the 4H-SiC(0001) surface followed by step-controlled epitaxy, facilitates the creation of a single-domain 3C-SiC layer with an epitaxial relationship to the underlying 4H-SiC, establishing a coherent (111)//(0001) interface aligned in the basal plane. An extremely low state density has been found to exist at the interface between the thermally-grown SiO_2 and the SLE-grown 3C-SiC layer in terms of local deep level transient spectroscopy (local-DLTS) based on scanning nonlinear dielectric microscopy (SNDM).

Introduction

The remarkable high voltage blocking capabilities and the reduced drift resistance exhibited by 4H-SiC Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) can be attributed to its wider bandgap over that of other SiC polytypes. However, challenges in 4H-SiC emerge due to its high density of the MOS interface states, causing high channel resistances as well as the insufficient reliability of the gate dielectrics that impact their practical applications. Conversely, 3C-SiC shows a much lower density of the MOS interface states which results in an improved reliability of the gate dielectrics [1, 2]. Nevertheless, its actual implementation has been impeded thus far due to generation of electrically active extended defects within the 3C-SiC crystal lattice [3]. These defects degrade the blocking capability, particularly under the influence of high electric fields [4, 5].

Implementing an optimal MOSFET entails harmonious integration of the advantageous properties of both 3C-SiC and 4H-SiC, while concurrently compensating their individual drawbacks. By employing a stacked structure of 3C-SiC on 4H-SiC, together with the use of a thermal oxide (SiO_2) film as the gate dielectrics on the 3C-SiC layer, a remarkable convergence of benefits becomes attainable. Notably, this methodology affords a substantial reduction in the state density at the SiO_2 film interface, consequently leading to a remarkable decrease in the channel resistance, while high breakdown voltages and low drift resistances are ensured by the 4H-SiC layer under the 3C-SiC layer.

The augmentation of the long-term stability of the SiO_2 film is also an integral outcome of this design, owing to the higher electron affinity of 3C-SiC. This characteristic, being higher than that of 4H-SiC by approximately 0.9 eV, contributes to an elevated potential barrier at the interface with SiO_2 [1]. Replacing the vicinal surface of 4H-SiC with 3C-SiC, intrinsically addresses the two prominent challenges, presenting a pivotal resolution.

To realize this idea, we have developed a novel epitaxial growth technique, described in the following section, which yields a high-quality 3C-SiC epitaxial layer on a 4H-SiC epitaxial layer.

Simultaneous Lateral Epitaxy (SLE)

As is well known, epitaxial growth of 3C-SiC on 4H-SiC substrate results in dense double positioning boundaries (DPB). This is because the basic unit cell of 4H-SiC includes hexagonal-site, which makes the stacking order of the cubic close-packed structure of 3C-SiC uncertain and generates twins. When twins coexist in the same basal plane, they generate DPBs, which forms one of the critical degradation factors in the device performance.

Controlling the stacking sequence on the topmost surface of 4H-SiC is one of the necessary conditions for eliminating twins within the 3C-SiC layer that is epitaxially grown on it. However, the twinning resolution of the 3C-SiC layer does not ensure DPB resolution. This is because the four Si-C molecular-layers (4 MLs) height step at the interface between the 3C-SiC and 4H-SiC layers causes a local phase shift in the stacking order of the 3C-SiC, which is originally 3 MLs period. To obtain a DPB-free 3C-SiC on 4H-SiC, therefore, its boundary must be strictly aligned in the basal plane. One practical method to achieve this has been developed by the NASA group. This method involves growing 3C-SiC after exposing the atomically-flat hexagonal SiC (0001) surface [6-8].

We also have succeeded in growing a DPB-free 3C-SiC(111) film on a 4H-SiC(0001) surface with inclined in the[11$\bar{2}$0] direction [9, 10]. This approach is termed Simultaneous Lateral Epitaxy (SLE). The schematic depiction of the SLE is presented in Fig. 1. In the conventional step-controlled epitaxy, the homoepitaxial growth of 4H-SiC proceeds as the surface of the 4H-SiC substrate is uniformly inclined at a consistent angle (θ) from the basal plane, typically around 4 degrees, in a specific direction, typically in the [11$\bar{2}$0] direction. This growth facilitates the lateral expansion of the 4H-SiC's specific structure across the entire surface. In contrast, SLE intentionally terminates the step-controlled epitaxy on the 4H-SiC in order to induce two-dimensional nucleation of 3C-SiC.

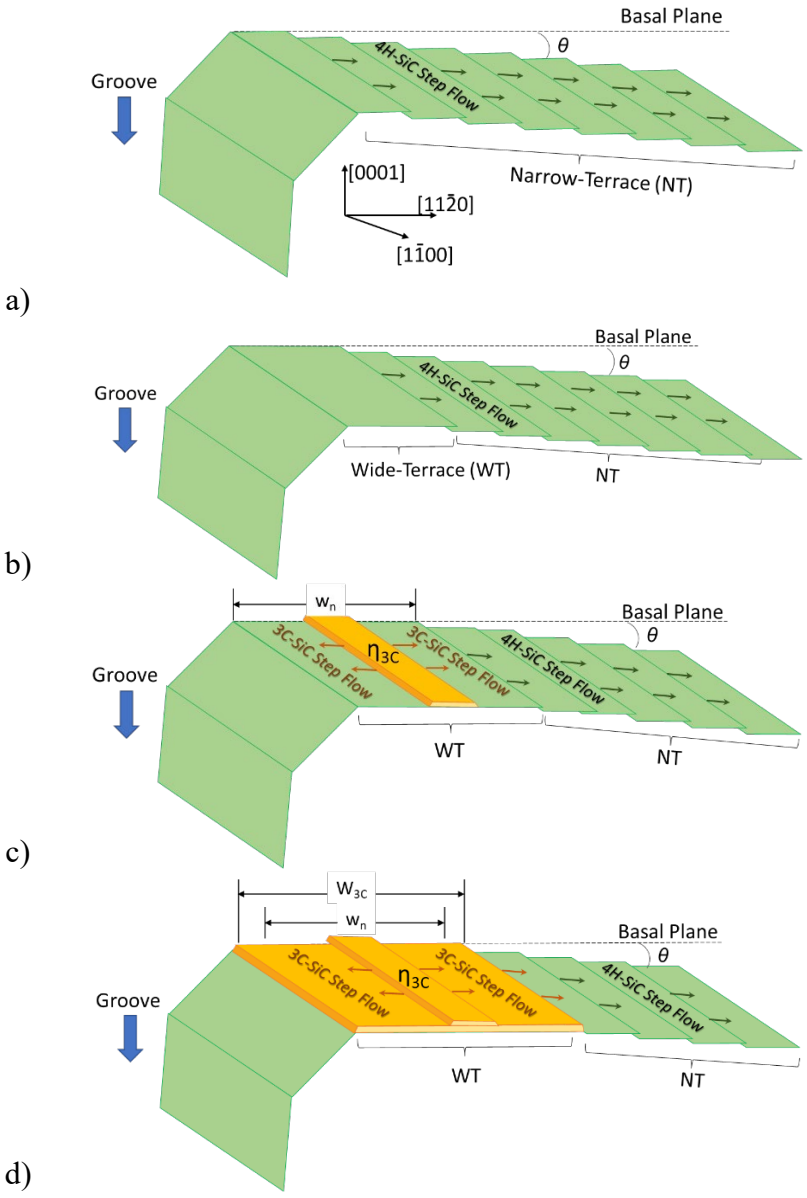

Fig. 1. Schematic of SLE growth: a) Groove in the [1$\bar{1}$00] direction terminates the step-controlled epitaxial growth of 4H-SiC; b) Atomically flat wide-terrace (WT) is formed adjacent to the groove; c) When the width of the WT exceeds a critical value for spontaneous SiC nucleation (w_n), 2-D nucleus of 3C-SiC (η_{3c}) is generated on the terrace, which provides new steps toward downstream. At the same time, 4H-SiC grows laterally from the step of narrow-terrace (NT); d) Additional η_{3c} is generated on WT of 3C-SiC, and it further promotes step-controlled epitaxial growth of 3C-SiC.

As shown in Fig. 1 a), the finite step-controlled epitaxy can be achieved by forming grooves parallel to the $[1\bar{1}00]$ direction at specific locations on the 4H-SiC surface. This groove intercepts the step flowing from upstream ($[\bar{1}\bar{1}20]$ direction) during the step-controlled epitaxy process and enlarges an atomically-flat wide-terrace (WT) downstream ($[11\bar{2}0]$ direction) adjacent to the groove (Fig. 1 b).

The WT expands progressively by increasing the supersaturation of the precursors as the epitaxial growth proceeds, and finally, when a critical width for spontaneous SiC nucleation (w_n) is reached, a two-dimensional nucleus of 3C-SiC (η_{3c}) is formed in the central region of WT (Fig. 1 c). Since the η_{3c} generates spontaneously, its crystal structure becomes that of 3C-SiC.

Once η_{3c} is formed on WT, it provides new atomic-height steps and expands the 3C-SiC structure in the $[11\bar{2}0]$ direction. At the same time, 4H-SiC grows laterally from the edge of the narrow-terraces (NT) on the misoriented surface of the 4H-SiC layer. As a result, the interface structure between the 3C-SiC and 4H-SiC layers propagates parallel to the basal plane, forming thereby a coherent interface suppressing the DPB generation.

As long as the groove acts as an obstacle to the step-controlled epitaxy, the WT expansion following the η_{3c} formation continues, so that the 3C-SiC layer expands in the $[11\bar{2}0]$ direction with increasing thickness (Fig. 1 d). The width of the resulting 3C-SiC area (W_{3c}) is determined geometrically with the epitaxial layer thickness (t_{epi}) as below.

$$W_{3c} = t_{epi} \cdot cot\,(\theta) \tag{1}$$

As schematically shown in Fig. 2, the distinctive feature of SLE is that 4H-SiC and 3C-SiC surfaces can coexist on the same flat surface and that the 3C-SiC surface can be extended to the desired width. For example, MOSFET cells can be arranged on the 3C-SiC area to reduce the channel resistance, and the adjacent 4H-SiC area can be used to fabricate a Schottky Barrier Diodes (SBDs) as for high-voltage freewheeling. SLE is attractive in that it provides flexibility in the device designing and simplifies the device fabrication process [9].

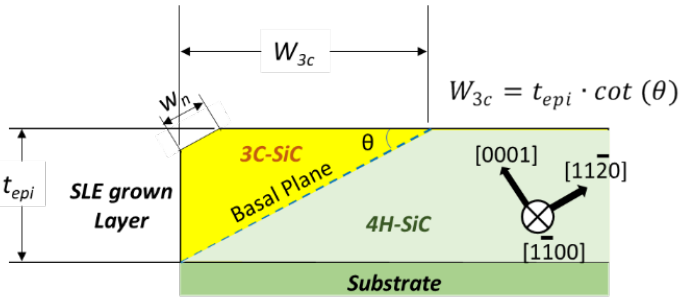

Fig. 2. Schematic cross-sectional structure of SLE growth layer: 3C-SiC layer stacks on 4H-SiC layer forming a coherent interface aligned in the basal plane. The width of 3C-SiC layer (W_{3c}) is determined by SLE layer thickness (t_{epi}) and tilt angle (θ) from the basal plane.

Experimental

This idea of SLE was verified experimentally according to the following procedure. A commercially available single-crystal 4H-SiC wafer was employed as a substrate. The wafer surface inclines 4 degrees from the (0001) orientation to the $[11\bar{2}0]$ direction. Multiple parallel grooves were formed on the wafer surface by femtosecond laser processing with a beam diameter of 3 μm, an output of 500 mW, and a repetition rate of 100 kHz [11, 12]. The grooves are roughly aligned in the $[1\bar{1}00]$ direction, and the groove period is 100 um with a typical depth of 4.5 um and a width of approximately 20 um.

After the laser processing, the 4H-SiC surface was subjected to a surface treatment called Step-Alignment®. This procedure is essential for specifying the stacking order on the WT top-surface to suppress the onset of twinning of 3C-SiC as well.

Then a 2.2 um-thick SiC layer was grown epitaxially in a $SiH_4 + C_3H_8 + H_2$ atmosphere. During the growth process, the donor concentration of the SiC layer was adjusted to 1×10^{16} cm^{-3} by adding nitrogen to the atmosphere. In contrast to the conventional SiC epitaxy, no high-temperature H_2

etching was performed prior to the growth in order to preserve the specific stacking order on 4H-SiC surface generated by Step-Alignment®.

The epitaxial layer formed by SLE was characterized as follows: The surface of the SLE-grown layer was observed by Scanning Electron Microscope (SEM) to distinguish different areas of the crystal structure. Electron backscatter diffraction (EBSD) was then performed to obtain pole figure (PF) and inverse pole figure (IPF) maps for both the 3C-SiC and 4H-SiC regions. The PF identifies the crystal structure of each distinguished area. The IPF maps show the orientation of 3C-SiC and 4H-SiC lattice planes on the specified area, which clarifies the stacking structure of 3C-SiC and 4H-SiC.

Finally, the interface state density (D_{it}), which strongly affects the MOSFET performance, was measured by forming a thermal oxide film on the SLE-grown SiC substrate. The formation of a thermal oxide (SiO_2) film onto the SLE-grown surface, which serves as the gate dielectric, facilitates a comparison of the D_{it} for both 3C-SiC and 4H-SiC. The 24 nm-thick SiO_2 thin film was thermally grown by $H_2 + O_2$ pyrogenic oxidation at 1323 K and atmospheric pressure for 4 hours.

Then, Scanning Nonlinear Dielectric Microscopy (SNDM) was employed to determine the D_{it} on both the 3C-SiC and 4H-SiC areas. SNDM is a kind of scanning probe microscope, and has a detection sensitivity for the capacitance changes as small as 10^{-22} F. In this investigation, a local deep level transient spectroscopy (local-DLTS) using the time-resolved SNDM technique was executed to measure D_{it} without fabricating MOS capacitors [13,14]. This enables the acquisition of a two-dimensional D_{it} distribution (D_{it} map), with a lateral resolution of approximately 30 nm.

Results and Discussion

Stacked Structure of 3C-SiC and 4H-SiC. Fig. 3 shows an SEM image of the surface of the SLE-grown layer. On the right of the laser-processed groove, which is in the downstream of the step-flow, a bright band of 32 μm-width and an adjacent dark-band of 41 μm-width are observed. The relationship between the 32 μm-width and the 2.2 μm-thick of the SLE-grown layer corresponds to Eq. 1.

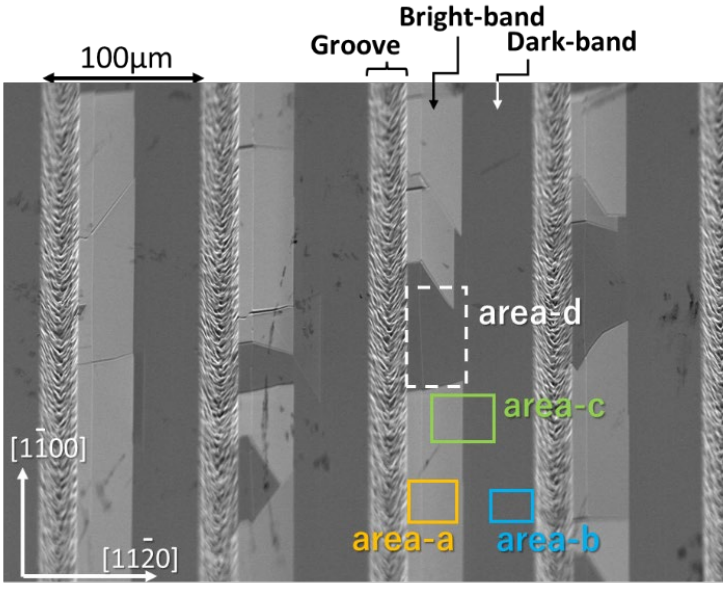

Fig. 3. SEM image of the surface of SLE-grown SiC epitaxial layer: a 32 μm-wide bright band is found on the right of the groove as well as a dark band adjacent to it on the right. The area-a on the bright band, the area-b and d on the dark band, and area-c on the boundary between the bright and dark bands are delineated and related to the result of EBSD observations.

The EBSD observations confirm that the bright band found in the SEM image of Fig. 3 corresponds to the single-domain 3C-SiC surface and the dark band to the 4H-SiC surface as described below. The PFs on the bright band (area-a) and the dark band (area-b) are shown in Fig. 4 a and b, respectively. The PFs on area-a (Fig. 4 a) correspond to that of 3C-SiC, indicating that the $\{1\bar{1}0\}$ and $\{100\}$ planes orient with a three-fold symmetric relationship, and the (111) plane orients in the normal direction. On the other hand, the arrangement of the PFs on area-b (Fig. 4 b) correspond to that of 4H-SiC, indicating that the $\{1\bar{1}00\}$ and $\{11\bar{2}0\}$ planes orient keeping a six-fold symmetric relationship, and the (0001) plane orients in the normal

direction. This suggests that the single-domain 3C-SiC(111) layer is epitaxially grown on 4H-SiC(0001).

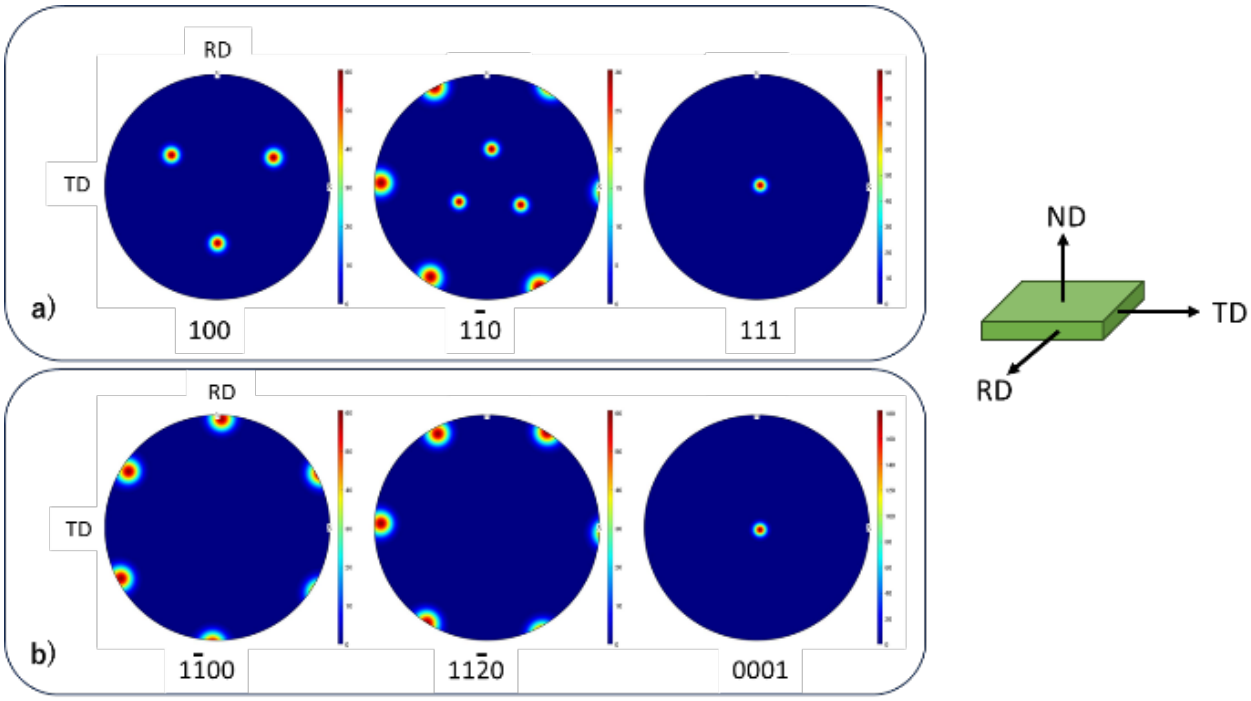

Fig. 4. EBSD Pole-figures: a) observed at area-a in Fig. 3 corresponds to the single domain 3C-SiC; b) at area-b corresponds to 4H-SiC

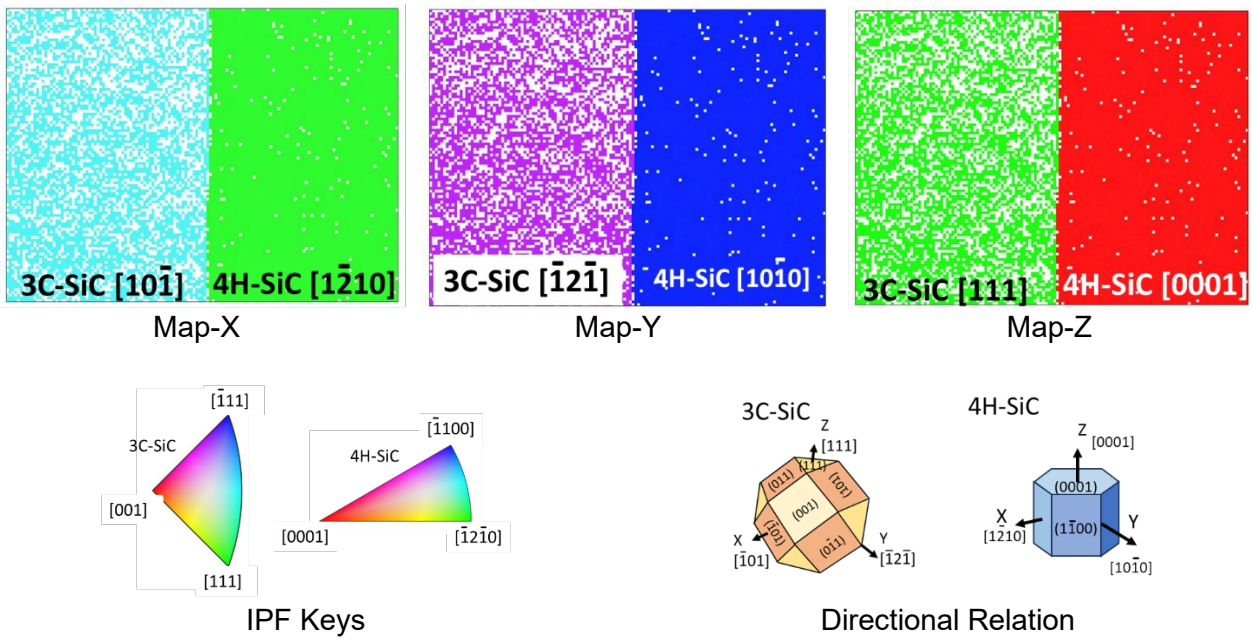

Fig. 5. EBSD IPF maps obtained at area-c in Fig. 3

The IPF maps obtained at around the boundary between the 3C-SiC and 4H-SiC surfaces give us further valuable insight. Fig. 5 shows the IPF maps observed at area-c in Fig. 3, just at the boundary between the 3C-SiC and 4H-SiC surfaces. The Map-X shows the 3C-SiC$[10\bar{1}]$ direction in the left half and 4H-SiC$[1\bar{2}10]$ in the right half. The Map-Y shows the 3C-SiC$[\bar{1}2\bar{1}]$ direction in the left half and 4H-SiC$[10\bar{1}0]$ in the right half. Furthermore, the Map-Z shows the 3C-SiC[111] direction in the left half and the 4H-SiC[0001] direction in the right half. The above observations confirm that all the bonding directions of the Si-C molecules in the twin-free 3C-SiC and 4H-SiC layers coincide and that a coherent interface is formed at the boundary between the 3C-SiC (111) and 4H-SiC (0001) planes.

Density of States at the Thermal Oxide Film Interface. The D_{it} maps measured by local-DLTS on the thermally grown SiO_2 film are shown in Fig. 6. The D_{it} map on 3C-SiC area (Fig. 6 a), where corresponds to area-a in Fig. 3, shows a random distribution of D_{it}, with a mean value of 7.3×10^{10} $eV^{-1}\cdot cm^{-2}$. In contrast, the D_{it} map on 4H-SiC area (Fig. 6 b), where corresponds to area-b in Fig. 3, shows a striped D_{it} distribution, with a mean value of 1.62×10^{13} $eV^{-1}\cdot cm^{-2}$. The fact that a clear difference in D_{it}, which amounts by more than 220-fold, is obtained between the polytypes on the same SLE-grown epitaxial layer means that the difference in D_{it} is not affected by the quality of the epitaxial layer or the difference of impurity concentration, but only by the difference in the crystal structure.

The observed low D_{it} in 3C-SiC is related to the difference in the electronic structure of the crystal. The D_{it} relates to near-interfacial intrinsic oxide defects with an energy position at 2.8 eV below the conduction band of the SiO_2, this energetically corresponds to the conduction band edge of 4H-SiC. On the other hand, the conduction band edge of 3C-SiC is shifted 0.9 eV below that of 4H-SiC, which implies higher electron affinity. Therefore, 3C-SiC MOS structure is less susceptible to the adverse effects of near-interfacial intrinsic oxide defects [16]. Actually, the respective D_{it} average values on the 3C-SiC and 4H-SiC regions are consistent with those on 3C-SiC (001) and 4H-SiC (0001) measured by a conductance method [2,15]. In addition to this, MOSFETs fabricated on that 3C-SiC(001) surface exhibit channel mobility of over 200 $cm^2\cdot V^{-1}\cdot sec^{-1}$ at room temperature [17]. There is a possibility that the formation of the channel region on the 3C-SiC (111) surface obtained on SLE can realize MOSFETs with high channel mobility comparable to that on the 3C-SiC (001) surface.

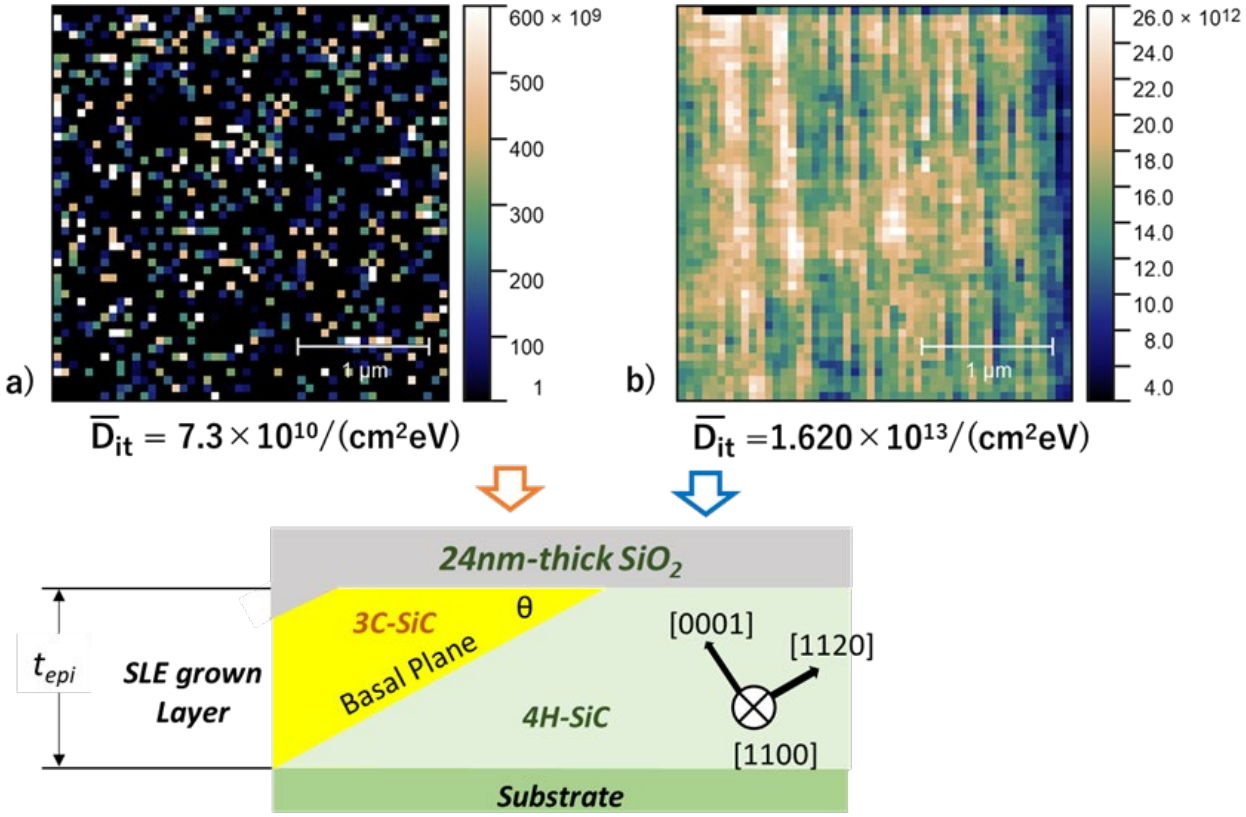

Figure 6. D_{it} maps measured by local-DLTS of SNDM on thermally grown SiO_2 on SLE-grown layer: a) on 3C-SiC area, b) on 4H-SiC area.

Summary

Simultaneous Lateral Epitaxy (SLE) of 3C-SiC and 4H-SiC is realized by locally preventing the step-controlled epitaxy on a 4H-SiC(0001) misoriented surface in the $[11\bar{2}0]$ direction. During the SiC epitaxial growth by SLE, 2-D nuclei of 3C-SiC are generated on an atomically-flat wide-terrace (WT)

in the basal plane of 4H-SiC, which provides steps of 3C-SiC structure. As a result, single-domain 3C-SiC layer is stacked on the 4H-SiC layer forming coherent interface as a boundary. The width of that 3C-SiC layer is defined by the geometric relationship between the thickness of the epitaxial layer and the misoriented angle of the 4H-SiC surface.

By growing a thermal oxide (SiO_2) film on the SLE surface where 3C-SiC and 4H-SiC are simultaneously exposed, a comparison of the respective interface state densities is achieved by local-DLTS with SNDM. The averaged interface state density on the 3C-SiC (111) area shows less than 1/220 of that on 4H-SiC(0001). This suggests that an extremely low channel resistance can be obtained by building a channel in the 3C-SiC layer grown by SLE.

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