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Confirmation of the Growth Mechanism of the Buffer Layer In Epitaxial Graphene on SiC

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Abstract This study substantiates the epigraphene formation theory on SiC, presenting it as freestanding graphene during thermal decomposition epitaxy. It was found that cool down process is responsible for the formation of the graphene buffer layer. Additionally the capping capabilities of the buffer layer have been evaluated using Raman spectroscopy and AFM measurements.

Introduction

Epitaxial graphene on SiC or so-called epigraphene has emerged as a highly promising candidate for nanoelectronic applications [1-2]. Integration of graphene and SiC allows for synergistic benefits by harnessing the unique properties of both materials. SiC is a wide band-gap semiconductor with excellent thermal and chemical stability, making it suitable for high-power and high-temperature applications [3]. On the other hand, graphene is a two-dimensional material with remarkable electrical, mechanical, and optical properties [4-6]. This integration enables the development of novel electronic devices that can take advantage of the wide band-gap characteristics of SiC and the unique properties of graphene. For instance, one application is the development of graphene-based field-effect transistors (GFETs) on SiC substrates [7]. The SiC provides a robust and thermally stable platform, while the graphene channel offers high carrier mobility, and both compatible with CMOS (complementary metal-oxide-semiconductor) processing techniques. This combination allows for the realization of high-performance and low-power electronic devices. The successful application of graphene relies on a comprehensive understanding of the growth process, which significantly influences the quality, structure, and properties of the resulting graphene layers, ultimately affecting their suitability for various applications [8]. Another significant challenge in graphene application lies in passivation layer technology. Among the various approaches, BN covering stands out as the most promising method [9]. SiC substrate has higher level of maturity compared to emerging materials as graphene, and its current main challenges lie in the area of integration into existing silicon technology infrastructure, which requires careful consideration of 3D integration, thermal compatibility, defect management etc. Overcoming these hurdles is essential for realizing the full potential of graphene-SiC hybrid systems in next-generation electronic and photonic devices and circuits.

In the present study, we conducted an experiment to validate the hypothesis regarding the growth process of epigraphene on the Si-face of 4H-SiC. It is proposed that, at temperatures exceeding 1400°C and an external pressure below 10^{-5} mbar, a Si thermal sublimation process occurs, and the excess carbon atoms arrange themselves into a graphene lattice. Consequently, graphene forms as a freestanding layer above SiC, allowing Si atoms to escape further. During the subsequent cooling process, the graphene layer gradually approaches the SiC surface and transforms into a buffer layer.

This transition could in principle be detected using Raman spectroscopy, but such elevated temperatures make experiments and interpretation of the results extremely difficult. Instead, in this study, we utilize the capping properties of graphene buffer layer to justify this growth hypothesis.

Methods

The growth and annealing procedures were carried out using an inductive furnace equipped with a graphite crucible. Samples were loaded and unloaded at room temperature. Ramp rates of 10°C/min were used for both heating and cooling steps. Initial graphene growth was done by sublimation at 1300°C for 5 hours under vacuum conditions (10-5 mbar). Annealing was performed at 1700°C for 30 minutes under an atmosphere of 1 atm. of Ar. Commercial inVia Renishaw system was utilized to conduct confocal Raman microscopy measurements at a 532 nm wavelength with 100x objective and 1800 l/mm grating. Raman spectral resolution is 0.3 cm^{-1}. Bruker Dimension Icon AFM was used in standard tapping mode with regular Si tip to scan the samples' topography after growth and annealing processes.

Results and Discussion

Epigraphene growth on SiC occurs through thermal decomposition, also known as thermal decomposition epitaxy (TDE), where the SiC substrate acts as a carbon source. In the TDE process, high temperature causes Si atoms to vaporize from the SiC surface, whereas carbon partial vapor pressure is negligible. The remaining carbon atoms rearrange themselves into a graphene lattice structure, forming the first graphene "floating" at specific distance from the SiC surface. Due to this distance, following Si sublimation is possible and it results in the creation of a next graphene layer underneath the existing one. Thus, TDE process leads to the formation of a multilayer graphene stack, where every subsequent graphene layer originates from the SiC substrate pushing up previous graphene layers and keep "floating" on top of SiC surface. The process window of this TDE is determined by the temperature and partial vapor pressure of Si (P_{Si}) in the proximity of SiC surface. Particularly for the Si-face, the P_{Si} is also related to the total number of grown graphene layers, providing a well-known self-limited epigraphene growth on SiC Si-face [8].

We assumed that, as the SiC is cooled down to room temperature, the bottommost graphene layer of the stack approaches the SiC surface, transitioning into what is commonly known as the "buffer" layer: graphene layer partially chemically bonded to the underlying Si-face of SiC substrate. We show that throughout subsequent temperature rise, the grown stack of layers maintains its integrity with SiC substrate up to certain temperature threshold restricting silicon sublimation and thus further graphene growth. Figure 1 presents AFM scans taken at the exact same position on the sample after graphene growth and after subsequent annealing, providing evidence that there is no discernible change in the topography.

In order to confirm that the cool down step is responsible for this shift of the growth process window we conducted a control experiment, where temperature was raised directly without a cool down to the room temperature. We observed the growth of graphene along with a change in the SiC surface morphology (Fig 1c), confirming the continued sublimation of silicon with increasing temperature. Figure 2 presents Raman spectra of graphene with consecutive and direct annealing after the initial growth. The pronounced increase in G-band intensity indicates a corresponding rise in the number of graphene layers in case of direct annealing process.

Additionally, this experiment provides evidence that the bare SiC surface can be annealed (up to 1700°C) without significantly degrading its roughness value, even in the absence of an external deposited carbon capping (initial RMS value of 2.42 nm vs. post 1700°C RMS value of 2.80 nm).

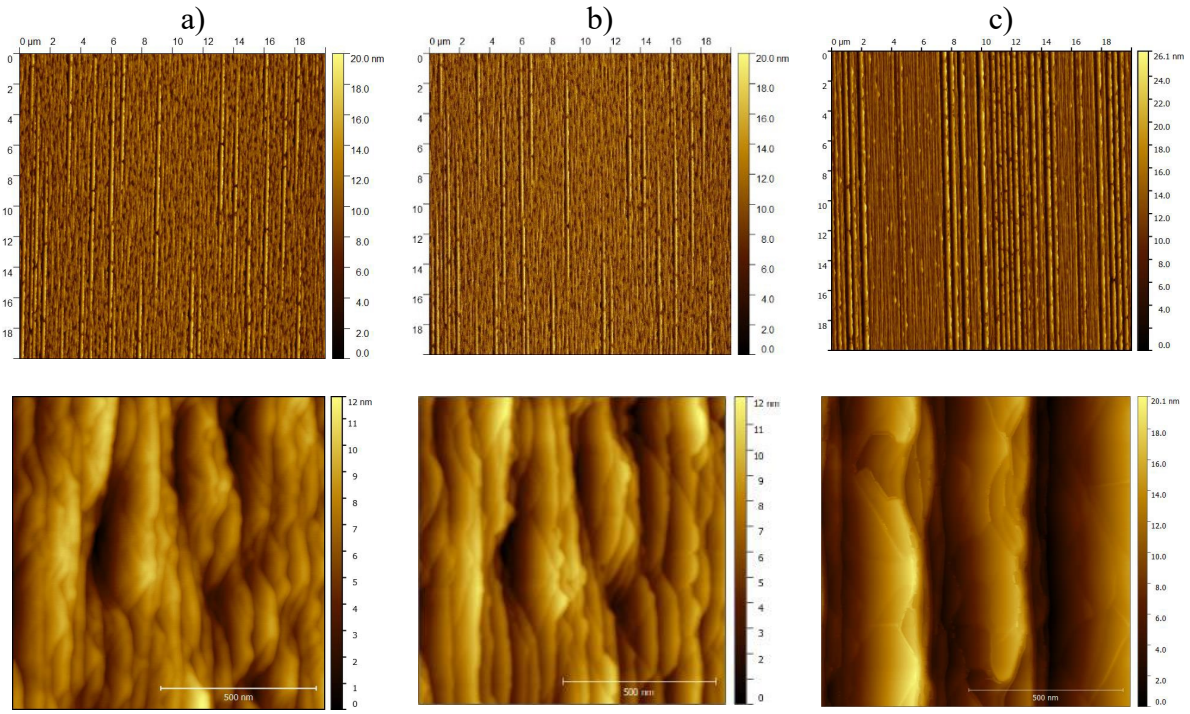

Fig. 1. AFM scans of 20x20 µm (top panels) and zoomed 1x1 µm (bottom panels) of 4H-SiC Si-face a) after initial graphene growth by sublimation at 1300°C, in vacuum 10^{-5} mbar; b) after subsequent annealing at 1700°C, in 1 atm. of Ar, scanned at the same place as in (a); c) after consecutive growth at 1300°C, in vacuum 10^{-5} mbar and annealing at 1700°C, in 1 atm. of Ar, without cooling down to the room temperature in between. Color bar corresponds to the full z-scale of each image. RMS roughness values for top panels: a) 2.42 nm b) 2.80 nm c) 3.80 nm.

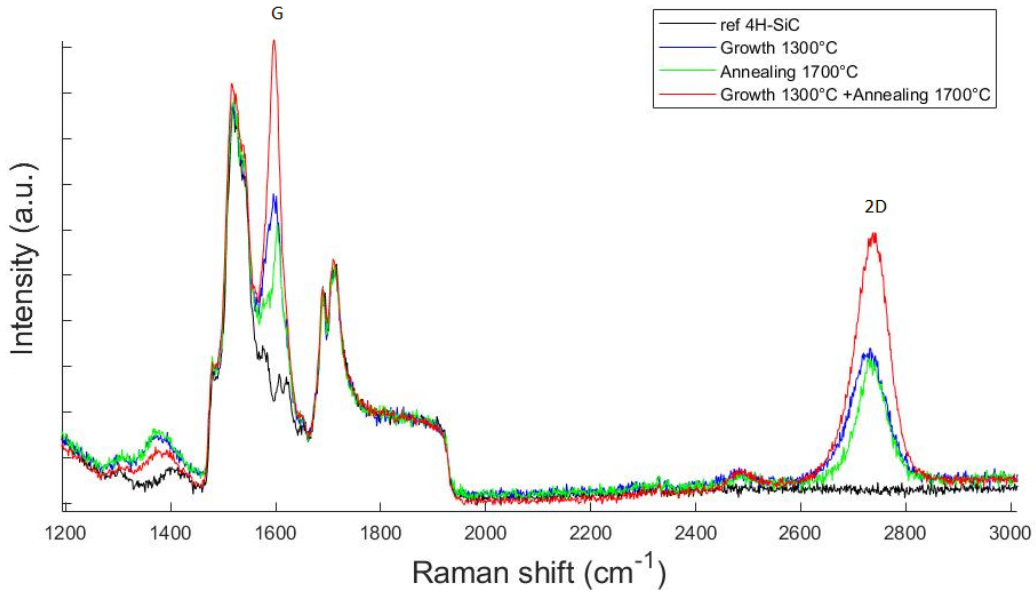

Fig. 2. Raman spectra of grown graphene (blue), graphene after cool down and annealing (green), graphene after consecutive growth and annealing without cool down step (red) and spectra of bare 4H-SiC (black). Laser excitation wavelength 532 nm.

Conclusion

In this study, we validated the growth mechanism of epigraphene formation on SiC, as a freestanding graphene during thermal decomposition epitaxy. As the temperature decreases, this graphene layer approaches and interacts with the SiC surface, forming chemical bonds and transitioning into a buffer layer. In case of multilayer growth process, subsequent layers of graphene, originating from SiC sublimation, emerge from beneath the existing graphene layers during the growth phase and the bottommost layer transforms into the buffer layer during the cooling down phase. A schematic representation of the growth mechanism can be found in Fig.3.

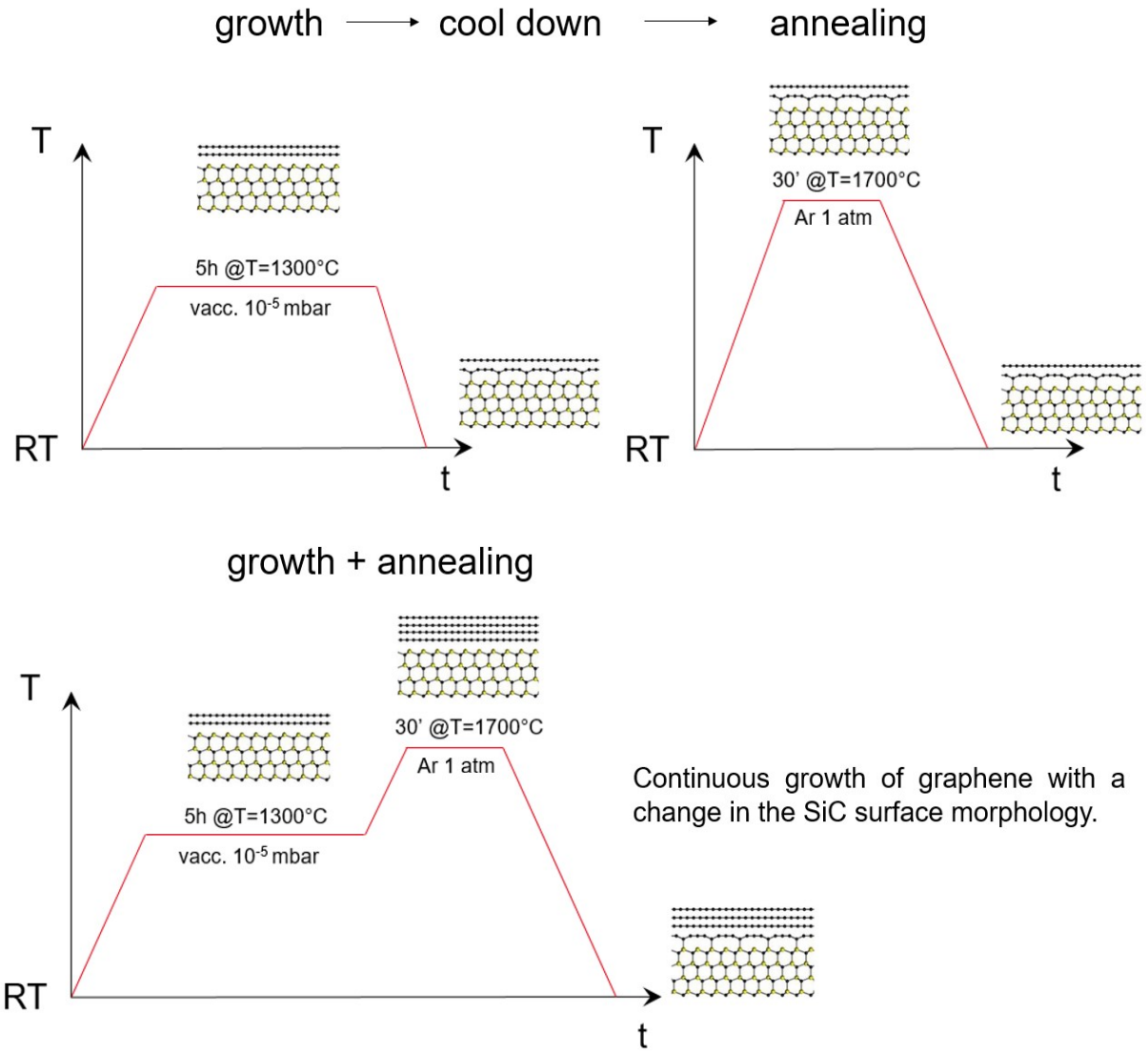

Fig. 3. Schematic representation of the epigraphene growth process, emphasizing buffer layer formation after the cool down phase and the buffer layer's capping capability (top panel).

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