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Investigations into the Impact of Deposition or Growth Techniques on the Field Oxide TID Response for 4H-SiC Space Applications

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Abstract. The total ionising dose (TID) reliability of a phosphorous pentoxide (P_2O_5) treated SiO_2 (silicon dioxide) layer is compared for the first time to other industrially relevant oxides formed on 4H-silicon carbide (SiC). Metal-oxide-semiconductor capacitors (MOSCAPs) are characterised before and after irradiation to ascertain changes in flat band voltage shift, leakage current, and dielectric breakdown (BV). Secondary ion mass spectrometry (SIMS) profiling reveals a significant phosphorus concentration near the SiO_2/SiC interface, which led to improved TID resistance. The P_2O_5 treated oxide had the lowest leakage current at high voltage bias due to the high-temperature (1,000°C) anneal, though it had a significantly negative flat band voltage due to the high concentration of deposited phosphorus atoms. The thermal and P_2O_5 oxides demonstrated a TID resistance, suffering only minor shifts in flat band voltage, while the P_2O_5 oxide suffered the smallest decrease in its BV and the smallest leakage current rise, post-irradiation.

Introduction

4H-silicon carbide (SiC) is a favourable material for power applications in space due to its wide-bandgap (WBG) properties, e.g., its high critical electric field, and high thermal conductivity [1]. One of the major influences behind the commercial development of SiC, is its ability to grow a simple and stable native oxide: silicon dioxide (SiO_2), which gives it a competitive advantage over other WBG semiconductors. However, the density of interface traps (D_{IT}) at the SiO_2/SiC interface is 1-2 orders of magnitude higher than in silicon (Si) systems, leading to a reduced channel mobility in metal-oxide-semiconductor field-effect transistors (MOSFETs) and threshold voltage instability issues [2]. The space environment is populated with a variety of ionising radiation, some highly energetic neutrons, protons, and heavy ions, which can contribute to instantaneous disruptions in the semiconductor device operation through a rapid electron-hole pair density generation within the active region - this issue is called single-event effect (SEE) [3, 4]. Commercial SiC devices have been shown to be especially vulnerable to SEEs, thereby limiting the material's use in space [5]. Recently however, a 1.2 kV reduced surface field (RESURF) diode has been demonstrated in TCAD to withstand ESA's standards for SEE hardness [6, 7].

Research into the SiO_2/SiC interface in space applications tackles the other main issue faced by SiC power devices from irradiation in space applications: Total ionising dose (TID). As a result of TID exposure, there is commonly a gradual shift in electrical characteristics caused by charge accumulation at the electrically active areas of the device, which eventually leads to total device failure [4]. Specifically, the TID response is drastically degraded in SiC devices with a field oxide structure, due to their higher D_{IT}. This is a major issue for novel RESURF device architectures, as conventional designs employ a relatively thick field oxide. Therefore, the development of SiC based devices that are resistant to both TID and SEE, and practically realisable, is of paramount importance for pushing this technology forward as an alternative to Si in the space field.

In this paper, we investigate the impact of different oxidation growth and deposition mechanisms on the TID reliability, including the use of a novel post oxidation anneal (POA) of phosphorous pentoxide (P_2O_5). Literature suggests that the treatment may prove to be better at passivating the SiO2/SiC interface than the conventional nitrogen ambient [8]. The POA generates a high concentration of phosphorus atoms at/near the device interface which can disrupt device function if proper charge balancing is not considered. Typical lateral diode drift region and MOSFET termination structures utilise thick field oxide surface passivation which suggests that the P_2O_5 treatment is possible on both vertical & lateral device topologies. Here, the P_2O_5 treated oxide was included to reduce charge accumulation during TID exposure by creating high energy traps that collect electrons and introduce recombination centers for charge removal [9]. To examine the TID impact of these oxides, metal-oxide-semiconductor capacitors (MOSCAPs) were fabricated and characterised in both capacitance-voltage (C-V) and leakage current measurements (I-V). The change in flatband voltage during exposure and dielectric breakdown (BV) before and after TID exposure are used to quantify the radiation-based degradation.

Experimental

To compare the impact of depositing P_2O_5 in the SiO_2 layer to the industrially relevant deposition/growth techniques for benchmarking, metal-oxide-semiconductor capacitors (MOSCAPs) were fabricated. 4H-SiC material was used that had a 350µm thick n+ substrate, which had a 10µm thick n- ($2\text{-}4\times10^{15}$ cm^{-3}) layer grown on top of it. The following oxidation splits were carried out, resulting in oxides that were all approximately 500nm thick:

1. **LPCVD:** Deposition of approx. 500nm SiO_2 by means of low-pressure chemical vapour deposition (LPCVD).
2. **Thermal + LPCVD:** Deposition of a thin (60nm) high-quality interface oxide, which was then topped up with a thick (460nm) LPCVD-deposited SiO_2 layer.
3. **ALD + LPCVD:** Deposition of about 40-50nm of SiO2 by means of atomic layer deposition (ALD), which was then topped up with a thick LPCVD-deposited SiO2 layer.
4. **ALD Plus FG + LPCVD:** Deposition of about 40-50nm of SiO_2, followed by a forming gas-anneal (FG), which was then topped up with a thick LPCVD-deposited SiO_2 layer.
5. **LPCVD + P_2O_5 anneal + LPCVD:** Deposition of 200nm LPCVD, which was then followed by a P_2O_5 deposition over 4 hours at 1,000°C, topped up by another 260nm of SiO_2 by means of LPCVD.

Pre-irradiation room temperature C-V measurements were recorded at 1, 10, 100 kHz and 1 MHz, using an Agilent E4980A precision LCR meter, while pre-irradiation room temperature I-V measurements were recorded using a Low Signal probe station with a semiprobe semiconductor parameter analyser.

The MOSCAP samples were put under gamma irradiation at the Cobalt-60 source in the Universite Catholique de Louvain cyclotron facility. The sample set was positioned to obtain a dose rate of approximately 726 rad/hour up to a total dose of 200 krad. The dose rate was then increased up to 1 krad/hour to reach a maximum dose of 500 krad, and conform to the European Space Agency (ESA) standards of electronic device certification for radiation hardness[10]. C-V Measurements were taken at steps of 100, 200, and 500 krad, at room temperature after samples were removed from the Cobalt-60 exposure chamber and measured immediately using a Low Signal probe station with semiconductor parameter analyser. A sample size of 5, 5, 3, 3, and 3 were taken for the P_2O_5, thermal, LPCVD, ALD, and ALD+FG MOSCAPs, respectively.

Post-irradiation room temperature I-V measurements were recorded at the same setup at the University of Warwick using new devices on the MOSCAPs.

Results

SIMS profiles in Fig. 1 show that the placement of phosphorus doping is close to the SiO_2/SiC interface, which is the ideal location to counteract the positive charge deposition, and capture charge for recombination during a TID event. Pre-irradiation, the P_2O_5 oxide is seen in Fig.2 to achieve the lowest leakage current above 200V, and the highest BV of 435V. The pre-irradiation C-V data in Fig.3 indicates that the P2O5 oxide has a significant negative flat band voltage, averaging -63.2 V. This has been explained through the presence of phosphorus-oxygen-hole-centers, which are positively charged in their active form [9].

Fig.3 also shows the C-V characteristics of the fabricated MOSCAPs at each stage of the TID exposure. The large negative shift in flat band voltage observed in the LPCVD and ALD MOSCAPs identifies a significant increase in positive trapped charge at the SiO_2/SiC interface. This trapped charge is attributed to the high number of interface and shallow traps that capture holes and protons. The large positive shift seen in the ALD+FG MOSCAP data indicates a high density of induced negative charge, trapped at high-energy interfacial defects. In comparison, the MOSCAPs that deployed a thermally oxidized dielectric layer posed little negative shift in flat band voltage due to an improved interface with less low and high-energy interfacial states during fabrication. In addition, the P_2O_5 MOSCAP displays a reduced positive flat band voltage shift due to charge negation that occurred during irradiation. This entails an initial sweep of electrons that are trapped at the high-energy state defects at the interface, seen in the flat band voltage shift of the P_2O_5 oxide between pre-radiation to 100 krad irradiation in Fig.3. However, the electron trapping efficiency has been shown to drop significantly as the majority of the P_2O_5 induced defects are occupied [9]. Furthermore, the P_2O_5 treatment acts as a high-temperature anneal, due to the high temperature (1000°C) that is used during the phosphorous diffusion process. This allows for passivation of the interface which reduces the shallow trap and interface states for positive charge trapping. These factors result in an equal positive and negative charge trapping rate near/at the interface, subsequently there is no observable shift in flat band voltage between 100 – 500 krad.

The post-irradiation I-V data seen in Fig.2 further reflects the increase in charge accumulation at the interface across the entire dataset. Compared to the pre-irradiation condition, which presents a ‘hard’ breakdown across all MOSCAPs, the post-irradiation dataset shows a significant increase in leakage current, such that there is 10μA of current by 250V. As such, they are compromised by the leakage current before they suffer a dielectric breakdown. In addition, all MOSCAPs show an increase of base leakage current to 2.3×10^{-10} A, which suggests that the density of induced mobile charge is the same across all MOSCAP structures. The lower difference in leakage current and voltage at 10μA exhibited by the P_2O_5 MOSCAP can be attributed to the superior interface passivation by the P_2O_5 treatment, despite the additional electron charge trapping occurring at the density of high-energy state interfacial traps.

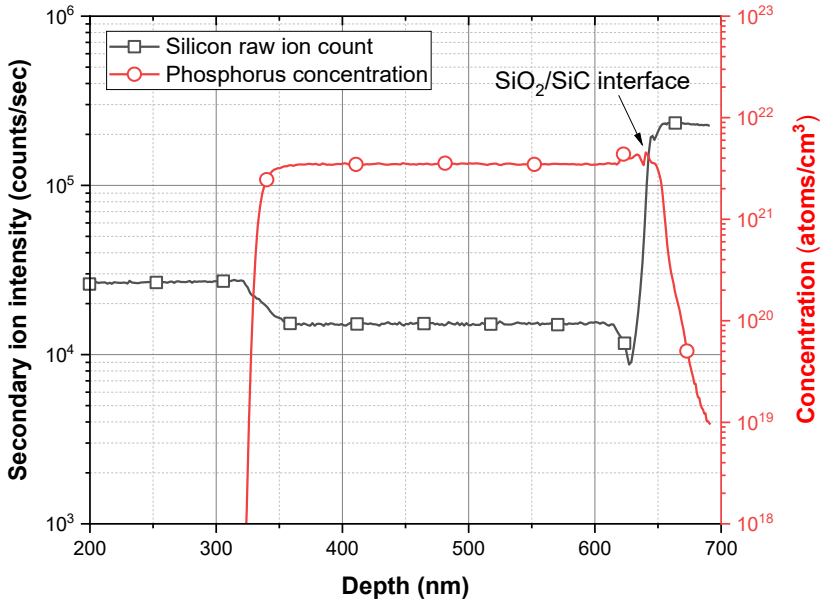

Fig. 1. SIMS measurements, showing the phosphorous concentration within the field oxide after deposition, pre-irradiation

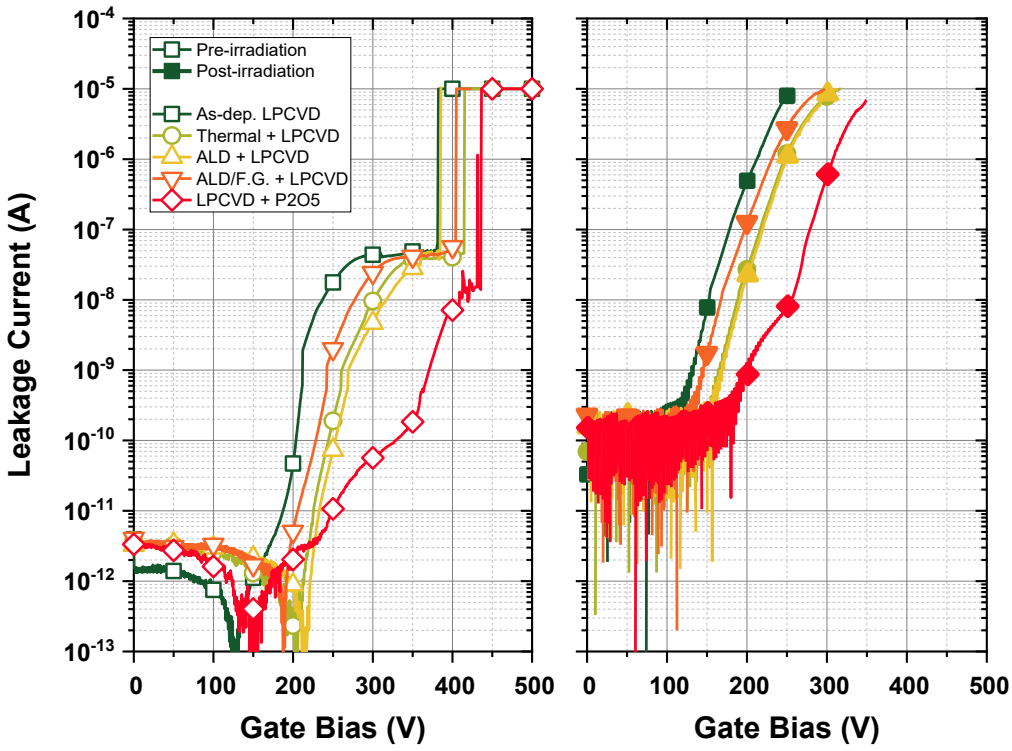

Fig. 2. Comparison of TID MOSCAP I-V response before (left) and after (right) irradiation. Measurements were carried out at 23°C and device area of 2.1×10^{-5} cm^2

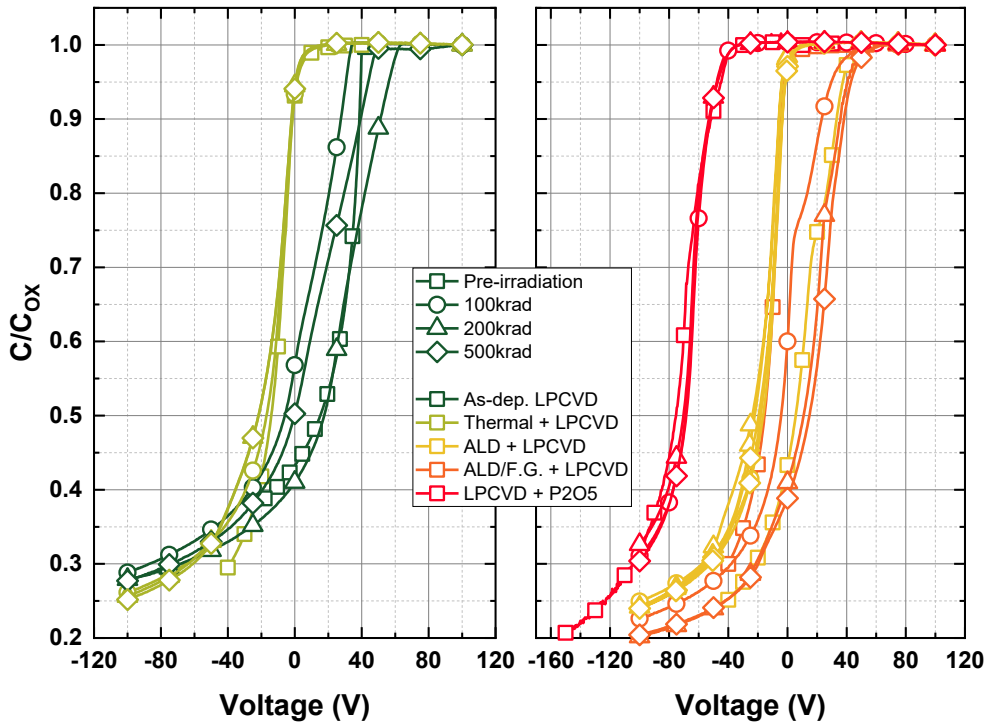

Fig. 3. Representative C-V graphs at 1 MHz before TID irradiation, and at 100, 200, and 500krad exposure. Measurements were carried out at 23°C and device area of 2.1×10^{-5} cm^2

Table 1. Flatband voltage, voltage at 10µA leakage current, and base leakage current of the MOSCAP dataset, before, during, and after irradiation. 5, 5, 3, 3, and 3 were measured for the P_2O_5, thermal, LPCVD, ALD, and ALD+FG MOSCAPs for flatband voltage before & during irradiation, respectively. 10 devices were measured for leakage current on each MOSCAP, before & after irradiation.

Oxidation technique	Pre-irradiation flatband voltage (V)	100, 200, 500krad irradiation flatband voltage (V)	Voltage at 10µA leakage current, pre-irradiation (V)	Decrease in voltage at 10µA leakage current, post-irradiation (%)	Base leakage current, pre-irradiation (pA)	Base leakage current, post-irradiation (pA)
LPCVD	37.5	24.0, 46.0, 34.0	382.5	32.4	1.59	29.6
Thermal + LPCVD	-4.26	-5.0, -5.5, -5.5	415.5	23.6	3.54	37.9
ALD + LPCVD	30.2	-4.5, -6.5, -4.5	385.5	22.7	3.62	29.6
ALD Plus FG + LPCVD	-4.68	21.0, 34.5, 37.0	406.0	22.8	2.95	40.2
LPCVD + P_2O_5 anneal + LPCVD	-63.2	-61.5, -60.0, -61.0	435.0	20.0	3.33	18.3

Summary

TID reliability in a novel method of P_2O_5 oxide deposition was compared to industrially relevant oxide growth techniques by gamma-ray irradiation of MOSCAP structures at steps of 100, 200, and 500 krad. The P_2O_5 treated oxide exhibited lower leakage current at higher gate bias (300-400V) and a significantly higher negative flat band voltage compared to the industrial oxides. The thermal and P_2O_5 oxides showed the lowest shift in flat band voltage with increasing radiation dose. Post-

irradiation, all oxides exhibited much higher leakage currents that compromise their BV. However, the P_2O_5 oxide exhibits the lowest leakage current increase between gate bias of 200-300V of all tested MOSCAPs.

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