Analysis of Lattice Damage in 4H-SiC Epiwafers Implanted with High Energy Al Ions with Silicon Energy-Filter for Ion Implantation

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Zeyu Chen^{1,a*}, Qianyu Cheng^{1,b}, Shanshan Hu^{1,c}, Balaji Raghothamachar^{1,d}, Charles Carlson^{2,e}, Dannie Steski^{2,f}, Tomas Kubley^{2,g}, Florian Krippendorf^{3,h}, Michael Rüb^{3,4,i,j}, Robert Koch^{3,k}, Reza Ghandi^{5,l}, Stacey Kennerly^{5,m} and Michael Dudley^{1,n}

¹Department of Materials Science & Chemical Engineering, Stony Brook University, Stony Brook, NY 11794 USA

²Brookhaven National Laboratory, Upton, NY, 11973 USA
³MI2-Factory GmbH, Moritz-von-Rohr-Straße 1A, Jena, 07745 Germany
⁴University of Applied Sciences Jena, Carl-Zeiss Promenade 2, Jena, 07745 Germany
⁵GE Research, Niskayuna, NY, 12309, USA

^azeyu.chen@stonybrook.edu, ^bqianyu.cheng@stonybrook.edu, ^cshanshan.hu@stonybrook.edu, ^dbalaji.raghothamachar@stonybrook.edu, ^eccarlson@bnl.gov, ^fsteski@bnl.gov, ^gtkubley@bnl.gov, ^hflorian.krippendorf@mi2-factory.com, ^hmichael.rueb@mi2-factory.com, ^jmichael.rueb@eah-jena.de, ^krobert.koch@eah-jena.de, ^lGhandi@ge.com, ^mStacey.kennerly@ge.com, ⁿmichael.dudley@stonybrook.edu

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Abstract. Multi-step high energy ion implantation enables uniform doping to depths up to 12 μm in 4H-SiC epiwafers for superjunction devices but extent of lattice damage is of significant concern for device fabrication. 4H-SiC wafers with 12 μm thick epilayers implanted with Al ions at a concentration of 5 x 10¹⁶ cm⁻³ using the Tandem Van de Graaff accelerator at Brookhaven National Laboratory across an energy range of 13.8 to 65.7 MeV and at different temperatures: room temperature, 300 °C, and 600 °C were analyzed by reciprocal space mapping measurements. Implanted layers exhibited tensile strains that decreased with increasing implantation temperature indicating dynamic annealing effect reduces lattice damage. On annealing at 1700 °C, for recovery of the lattice strain, RSM measurements show that the highest implantation temperatures have the lowest residual strains. In addition, the use of a Silicon Energy-Filter for Ion Implantation (EFII) for Al implantation in a single stage to the depth of 15μm is found to further reduce lattice strain compared to wafers implanted without EFII to the same doping concentration. This preliminary study will assist in optimizing the implantation and annealing conditions for the development of superjunction devices.

Introduction

Silicon Carbide (SiC) is a wide bandgap semiconductor with exceptional properties that make it ideal for power devices, including wide bandgap, high breakdown voltage, and excellent thermal stability [1]. The demand for 4H-SiC devices capable of handling voltages ranging from 1.7 to 6.5 kV is increasing, driven by their applications in hybrid systems, shipboard and power grid configurations, and high-speed trains. These devices are generally fabricated on 4H-SiC wafers with thick epilayers to improve breakdown voltages [2], but uniformly doping such thick epilayers poses significant challenges. A promising approach to address this involves using multi-step high-energy ion implantation, utilizing the system at Brookhaven National Laboratory's Tandem Van de Graaff accelerator facility [3], which can implant ions with energies up to 150 MeV. This technique has successfully produced medium voltage charge balance devices, including 2 kV and 3.8 kV superjunction structure PIN diodes [4]. Nonetheless, high-energy ion implantation introduces

considerable lattice strain by displacing host atoms in the epilayer, making it crucial to characterize this strain to understand the damage induced by high-energy implantation. One way to reduce lattice damage is by employing high temperature annealing process, however, annealing temperature of up to 2000 °C is needed to fully recover the strain [5] and these elevated temperatures can result in rough wafer surfaces, which is detrimental for device fabrication. Another approach to reduce the annealing temperature is to perform high-energy implantation at elevated temperatures, as the dynamic annealing effect can partially reduce lattice strain in the as-implanted wafer. The dynamic annealing effect has been extensively studied over the years. Kuznetsov and colleagues [6] suggested that this reduction in lattice damage is due to the annihilation of vacancies and interstitials created during implantation. The level of lattice damage following heated implantation is influenced by the balance between the generation and annihilation rates of these point defects. Conventional implantations at temperatures up to 600 °C have been demonstrated to mitigate the formation of basal plane dislocations (BPDs) caused by the strain induced during implantation [7].

Synchrotron X-ray plane wave topography (SXPWT) and reciprocal space mapping (RSM) techniques have demonstrated their capability to evaluate the strain distribution in a 12 μm epilayer of a 4H-SiC epiwafer subjected to multi-step, high-energy implantation with 4.4 x 10¹⁶ cm⁻³ Al ions at room temperature. The results indicated that the strain in the implanted region was approximately 2.5 x 10⁻⁴ higher than in the non-implanted region [8]. To reduce the damage caused by implantation, multi-step implantation with 5 x 10¹⁶ cm⁻³ Al ions was conducted at room temperature, 300 °C, and 600 °C. Strain measurements from RSM showed values of 4.1 x 10⁻⁴, 3.3 x 10⁻⁴, and 2.0 x 10⁻⁴, respectively [9]. The data clearly demonstrate a reduction in strain with increasing implantation temperature due to the dynamic annealing effect. Recently, Steinbach and colleagues reported that using a jagged Energy-Filtered for Ion Implantation (EFII) device manufactured by MI2-Factory can produce a box-shaped concentration profile with a single implantation [10]. This technique may further reduce the strain level in the implanted wafer. Characterization of post-annealed wafers multistep high-energy implanted with Al ions and as-single-step implanted wafer with EFII will be discussed in this paper.

Experiment

4H-SiC wafers with 12 μm epilayers were blanket implanted with Al ions by multi-step high energy implantation at room temperature (RT), 300 °C and 600 °C at BNL via the Tandem Van de Graaff accelerator with energy range of 13.8 to 65.7 MeV. The concentration of the implanted Al ions is 5 x 10¹⁶ cm⁻³. Following implantation, the wafers were annealed at 1700°C (typical temperature for implanted SiC wafers). Besides, another wafer was subjected to single-step high energy implantation at RT with EFII manufactured by MI2-Factory at 60 MeV, then Secondary Ion Mass Spectrometry (SIMS) analysis was carried out to confirm the concentration and depth of the Al ions.

The wafers were characterized by high resolution X-ray diffraction (HRXRD) to analyze the effect of temperature on the lattice strain generated by the implantation. Rocking curves and reciprocal space mapping (RSM) in (0008) reflections were carried out on a Bede D1 diffractometer with Cu K α (λ =1.54056 Å). The beam was conditioned by a MaxFlux multilayer mirror and channel-cut Ge (004) monochromator at 40 kV and 30 mA. For triple axis scan and RSM, a channel-cut Si (111) analyzer was placed in front of the detector (see Fig. 1 for schematic of the experimental setup).

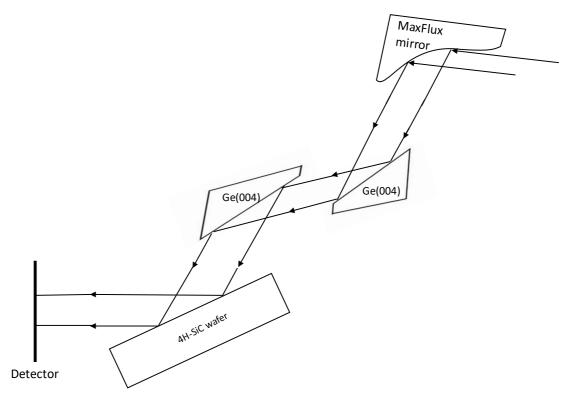


Fig. 1. Schematic of experimental setup of HRXRD.

Result and Discussion

Multistage high energy implantation has previously been shown to achieve box implantation [11]. Therefore, SIMS analysis was performed for wafer subjected to single-step high energy implantation with EFII as shown in Fig. 2 to measure the doping profile. The result shows a box profile with Al concentration of 5x10¹⁶ cm⁻³ to the depth of 15 µm, proving the effectiveness of employing EFII to achieve box profile with a single-step implantation. The corresponding triple axis $\omega - 2\theta$ scan by HRXRD shown in Fig.3 displays main and satellite peaks with a peak separation of 45", indicating tensile strain in the epilayers after implantation. RSMs were recorded to analyze the strain characteristics of the wafers implanted with multi-step implantation at RT, 300 °C, 600 °C, as well as the single-step implantation with EFII at RT, as illustrated in Fig. 4. The RSMs reveal two peaks, with the satellite peak diffracted from damaged epilayer yielding higher intensity compared to the substrate peak due to the relatively thick epilayers that attenuate diffracted intensity from the substrate. The vertically aligned peaks suggest the absence of lattice tilt, while the satellite peaks, positioned on the negative side of the main peak along the y-axis, indicate that the epilayers experience tensile strain following implantation. This observation is consistent with the results from the triple axis scans [9]. The strain level of 4.1×10^{-4} , 3.3×10^{-4} , 2.0×10^{-4} and 3.1×10^{-4} was estimated from RSM by the following equation:

$$\frac{\Delta d}{d} = -\Delta Q_{y} d \tag{1}$$

where d is the lattice spacing of 4H-SiC (0008) and Q_y is the change in peak position along the vertical axis in the RSM. The peak separation and estimated strain level of wafer implanted with EFII are comparable to those of wafer implanted with multi-step high energy at 300 °C, illustrating that the single-step implantation with EFII can reduce the level of as-implanted damages. Kuznetsov and coworkers have discovered that the relative damage due to implantation can be lowered by decreasing the ion flux [6]. By employing EFII, only single-step implantation is needed to create a box profile, which can significantly decrease the accumulated time for implantation compared to multi-step implantation. Therefore, the flux or dose rate of implantation employing EFII can be much smaller

than that of multi-step high energy implantation, leading to reduction of the lattice strain after implantation for wafer implanted with EFII.

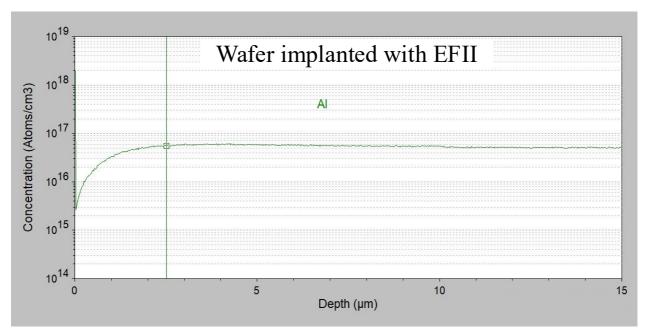


Fig. 2. SIMS result of wafer subjected to single-step implantation with EFII.

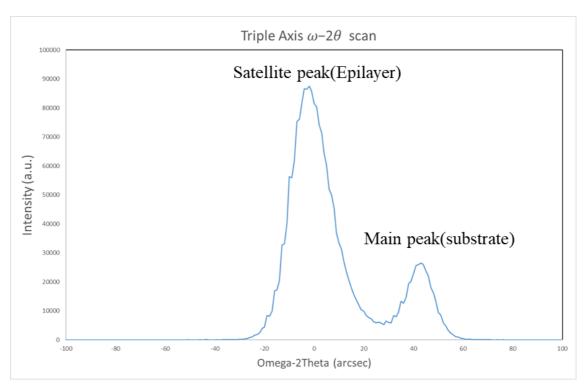


Fig. 3. Triple axis $\omega - 2\theta$ scan wafer implanted with EFII.

Fig.5 shows RSMs of wafers after multi-step implantation at RT, 300 °C, and 600 °C and after annealing process. The RSMs of post-annealed wafers, plotted in rotation axis with intensity scaled at 100%, 50%, 10%, 1%, 0.1% and 0.01%, indicate single peak without satellite peaks, meaning that the damages due to implantation have been recovered, since the high temperature condition increase the mobility of dopant atoms, interstitials and vacancies and encourage them to move to the correct lattice sites. Overall, the RSMs of annealed wafers exhibit symmetric contours along the $\omega - 2\theta$ axis. However, for the contour of 0.1% of peak intensity (highlighted by orange dashed line), the

width of the contour of wafers implanted at RT, 300 °C, and 600 °C are 122", 118" and 100" respectively. The residual strain in the annealed wafer will have a larger effect of diffuse scattering, leading to an increase of width at low intensity. Therefore, implantation at higher temperature can lower the residual strain after annealing process.

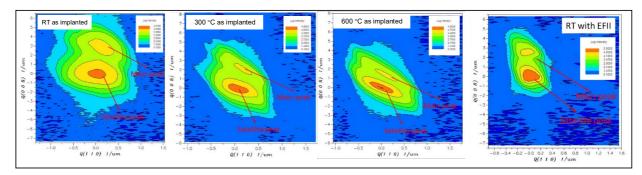


Fig. 4. 0008 Reciprocal space maps of wafers as-implanted with multi-step implantation at RT, 300 °C, 600 °C and single-step implantation with EFII at RT.

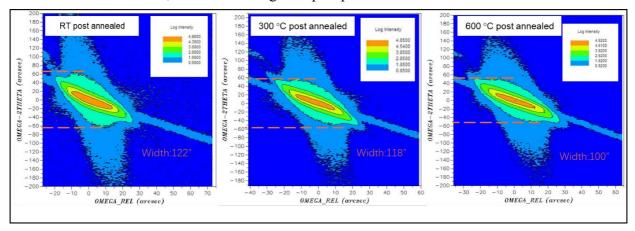


Fig. 5. Post-annealed at 1700 °C of wafers with multi-step implantation at RT, 300 °C, 600 °C. The orange dashed line indicates the contour having 0.1% maximum intensity.

Summary

High resolution X-ray diffraction have been employed to characterize implanted and post-annealed 4H-SiC wafers implanted at RT, 300 °C, and 600 °C. The result shows that the major damages have been recovered, while the residual strain decreases as implant temperature increases. Implantation with Si Energy-Filter for Ion Implantation has been conducted, indicating a box concentration profile can be achieved by single-step implantation and the as-implanted strain is lower due to the effective dose rate is smaller for single-step implantation.

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