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Evaluation of 4HSiC Epitaxial CVD Process on Different 200 mm Substrates for Power Device Applications

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Abstract. The increasing demand for WBG materials like SiC has led STMicroelectronics to expand wafer diameter from 150 mm to 200 mm, enhancing production yield and reducing costs. However, this expansion poses challenges in preserving crystalline quality. This investigation examines the impact of defects on 200 mm wafers, focusing on Total Usable Area (TUA) and electrical performance, particularly in wafers with polytype inclusions and high basal plane dislocation (BPD) density. Although the results for non-standard wafers show a significant reduction in TUA and an increase in electrical failures, the overall distribution of functional and non-functional devices remains stable, indicating process consistency.

Introduction.

The demand for reliable Wide Band Gap (WBG) materials like SiC and GaN for power devices and high-voltage products has been steadily growing over recent decades, driven by their extensive use in various applications [1,2]. SiC and GaN offer an optimal balance between their theoretical advantages – such as high voltage blocking capability, high-temperature operation, and high switching frequencies – and the commercial availability of the base materials (wafers) and the maturity of their manufacturing processes [3,4]. These materials have significant potential to miniaturize power electronic converters, enabling operation at higher frequencies and temperatures with far greater power conversion efficiency compared to current silicon power devices [5]. The market for SiC power devices has expanded so rapidly in recent years that many suppliers are struggling to keep up with demand, as production has traditionally relied on 150 mm diameter wafers. In response, STMicroelectronics has initiated production of SiC wafers with a 200 mm diameter. The main challenge in scaling up from 150 mm to 200 mm lies in increasing the size of the bulk crystals while maintaining productivity and crystal quality. A 50 mm increase in wafer diameter results in a 78% increase in area, thereby boosting the number of devices per wafer [6-8]. This shift enhances the productivity of front-end manufacturing lines, which in turn lowers the cost of the final devices. The resulting increase in production volume and cost reduction is expected to drive the widespread adoption of SiC-based power devices in the automotive industry, which is rapidly advancing towards electrification [9].

Experiment Set-Up

In the view of seed enlargement (from current 150 mm to 200 mm substrates), twenty-four 200 mm SiC substrates were grown with the same process in the same reactor in order to evaluate, mainly in wafers having % polytype (3C, 6H or 15R-SiC mainly) and BPD values higher than commercial specifications, the impact of defect on Total Usable Area (TUA) and electrical tests.
For this purpose, the substrates were selected as follows: 12 standard 4H-SiC wafers, 6 wafers 4H-SiC with polytype inclusion (6H/15R) ≤ 99% and 6 wafers with BPDs density > 3000 cm^{-2} (in 2 of them there are also polytype inclusion).

Growth. The growth of n-type 4H-SiC 200 mm epitaxial layer 4H-SiC on Si-face substrates (0001) at 4° off axis was performed on low-pressure, single-wafer, hot-wall chemical vapor deposition (LP-CVD) reactor. The homo-epitaxial growth process is carried out at temperatures of about 1650 °C and involves the use of silane (SiH_4), propane (C_3H_8), and ethylene (C_2H_4) as silicon and carbon precursors, respectively. Nitrogen (N_2) was added as n-type dopant, and high purity industrial grade hydrogen (H_2) was used as carrier gas as well as a reducing agent for epitaxial layer growth. The presence of HCl, due to the chemistry system, is required to prevent the formation of Si droplets (Si-C bonds stronger than Si-Si ones). The epilayer specifications, required for medium/high voltage device technologies, are ~6.5 μm for thickness and ~1.8E16 cm^{-3} for doping.
The uniformity of thickness and doping concentration distribution in the epitaxial layers, expressed as [maximum value – minimum value]/mean [%], was assessed using Fourier Transform Infrared (FT-IR) spectrometry and Mercury-Probe Capacitance Voltage (Hg-CV), respectively. Bow and warp measurements were conducted using FRT; these parameters after epi are reduced with a typical symmetrical bowl shape reported on all wafers (data not shown). No impact was observed on the epitaxial process concerning the out of spec in % polytype and density of BPDs.

Characterization and EWS analysis. The defectivity characterization was conducted using Candela® and Altair® tools, both from KLA. The Candela tool uses highly sensitive optical technology able to simultaneously measure scattering intensity at various angles of incidence, topographic variations, surface reflectivity and phase shift, and photoluminescence for the detection and classification of a wide range of defects, such as crystallographic defects. A simultaneous Bright-field and Dark-field optical path to capture a variety of defects in the sub-micron to 5-micron range is used in the Altair optical microscope.
Defective Die Percentage (DDP) and Total Usable Area (TUA), critical parameters commonly used to evaluate the yield and manufacturing efficiency of semiconductor devices, were analyzed. Using a grid with dimensions similar to the device, the impact of defects on TUA (calculated as 100 – DDP by Altair) *post* epitaxial growth can be quantified. As illustrated in **Fig. 1**, wafers with a polytype inclusion and BPDs values exceeding commercial specifications exhibit a TUA reduction of approximately 12% for polytype (PT) and 18% for high-BPD (hBPD), respectively.

Wafer Feature	Polytype 4H on Si-face [%]	BPD mean density[cm^{-2}]	THK EPI [µm]	DOP EPI [cm^{-3}]
STD	100	316	6.480	1.815E+16
STD	100	108	6.528	1.818E+16
STD	100	177	6.559	1.765E+16
STD	100	276	6.554	1.896E+16
PT	99,1	1897	6.536	1.805E+16
PT	99,3	1961	6.535	1.810E+16
PT	99,8	263	6,451	1,560E+16
PT + hBPD	>99,5	3927	6,461	1,750E+16
hBPD	100	3428	6.574	1.805E+16
hBPD	100	3182	6.583	1.908E+16
hBPD	100	3394	6,49	1.770E+16
hBPD	100	2416	6.477	NA

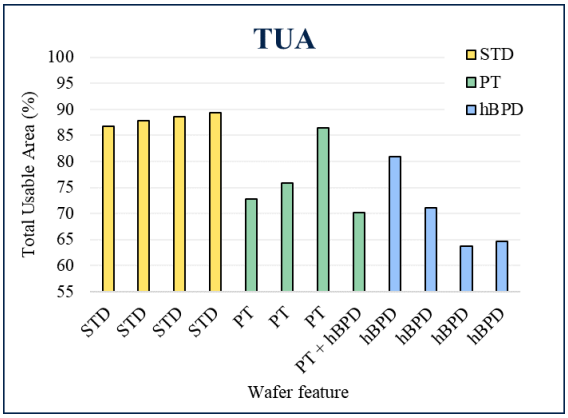

Fig. 1. On the right is the table with data on the characteristics (% of polytype on the Si face and BPD density) of the substrate and epilayer (thickness and average doping, denoted as THK and DOP respectively) of a sample consisting of twelve 200-mm 4H-SiC wafers. Wafers with polytypical inclusion are displayed in green, standard wafers in yellow, and wafers with high BPDs density in light blue. On the left, the Total Usable Area (TUA) of the 12 wafers is shown.

An example of a wafer with polytype inclusion is shown in **Fig. 2**. Both the Candela and Altair maps reveal an increased concentration of defects (such as carrots, topo defects, and surface triangles) in the region close to polytype. In this area there is a marked correlation between the defect maps and the EWS (Electrical Wafer Sorting) map, with most defects causing catastrophic failures.

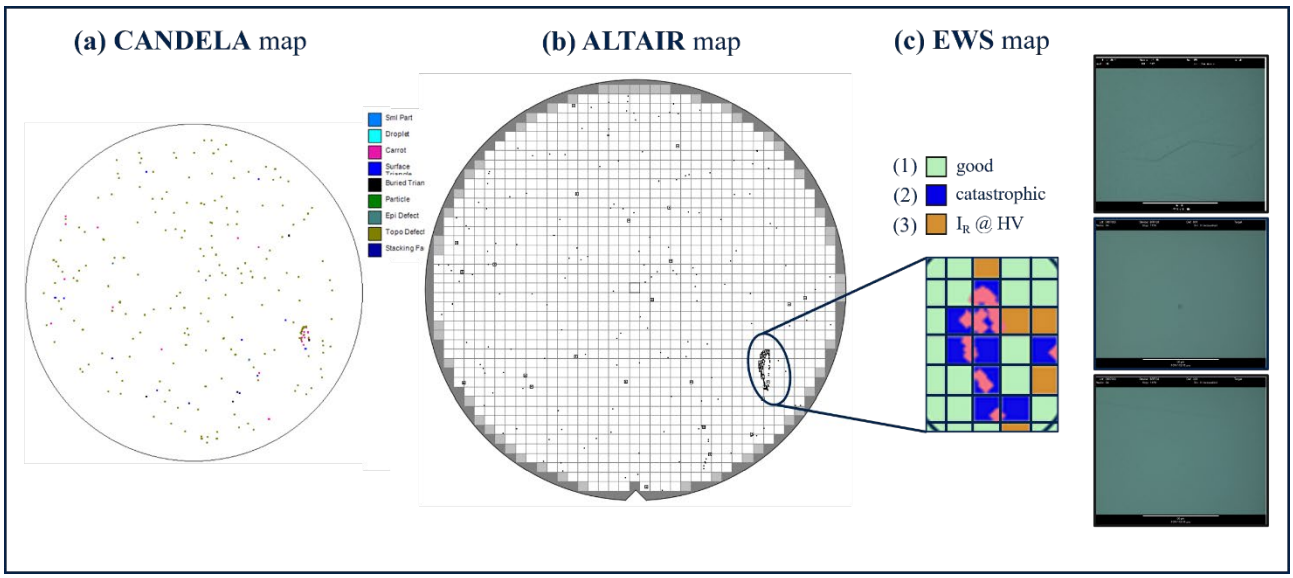

Fig. 2. Composite characterization of an out-of-spec wafer for the polytype percentage. On the left, the Candela map displays various types of defects (crystallographic and morphological) on the wafer surface, categorized by color. The Altair map in the center provides a morphological defect view, with an enlarged region highlighting the EWS map, which illustrates device failures (catastrophic or due to leakage under high voltage) caused by defects, depicted in pink, in the polytype region. On the right, optical images illustrate the most common defects as physical manifestations of these failures.

The Electrical Wafer Sorting (EWS) phase is critical in the semiconductor manufacturing process, serving to rigorously test all devices with the primary goal of identifying non-functional dies, thereby preventing their integration into final packages. This phase involves a sequence of electrical measurements that classify each device as either "good" or failed. By analyzing the data obtained from the testing of a Power MOSFET of 650V with area of 17mm^2, the origin of the failures can be traced, identifying both the specific phase of the process and the tools involved. **Fig.3** illustrates the EWS test bin results on a limited sample of wafers. Each graph represents the occurrence of failure or non-failure normalized against the mean value of that event on the standard sample of wafers analyzed. The graphs display the portion of devices classified as “good”, i.e., having no failures, “catastrophic” fails, where the devices fail immediately during the first measures of test program, and, finally, the “leakages-related” fails that occur during the check of leakage between drain and source at high biases similar to the device's operating voltage (IR@HV). In (a) it is observed that wafers with polytype inclusion show an occurrence of good devices greater than or at least overlapping with standard wafers (good, PT>1) and that wafers with high density of BPDs an occurrence less than 1. In (b) the occurrence of catastrophic failures in wafers with hBPDs is much higher than in wafers with PT and STDs. This is consistent with the defect maps shown in **Fig.2** in which polytype inclusion is in a well-localized region and therefore predictable at the catastrophic failure level. In contrast, in wafers with a high density of BPDs, failures are spread across the entire wafer and thus not easily predictable; in this sense, an XRT analysis could assist in establishing a correlation between BPDs and failures. A different trend is observed in graph (c) in which the occurrence of leakage failures is overlapping in wafers with hBPDs and STDs, less than 1 instead in wafers with polytype inclusion, emphasizing the role of BPDs and related defects across the epi in the increase of failure events due to high leakage.

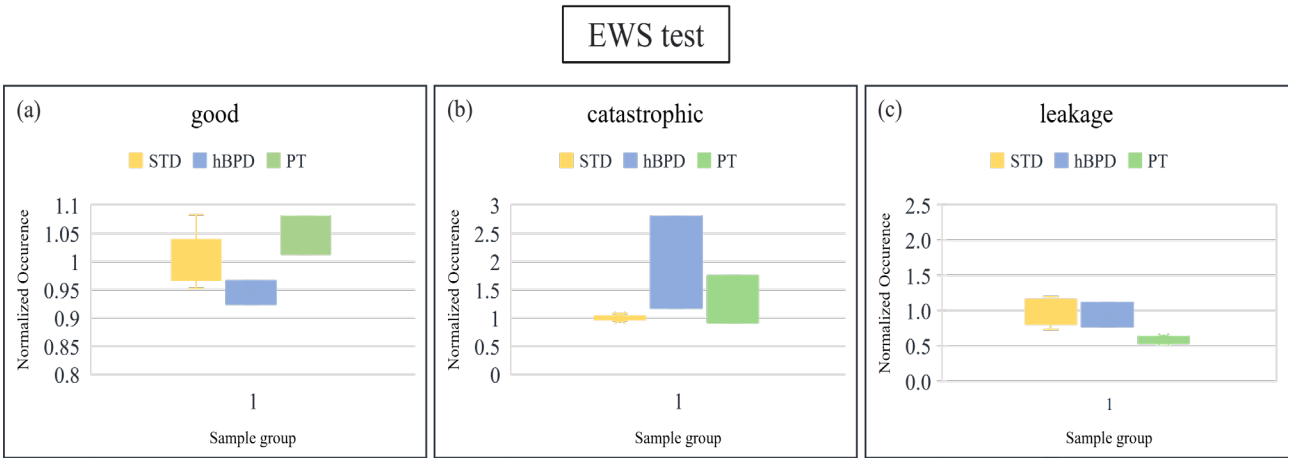

Fig. 3. The three vertical bar graphs report the results of EWS tests performed on three types of wafers: standard (STD, yellow left-bar of the graph), with high density of BPDs (hBPD, blue center-bar), and with polytype inclusion (PT, green right-bar). Graph (a): occurrence of devices classified as “good,” i.e., free of failures. Graph (b): incidence of catastrophic type failures. Graph (c): occurrence of failures due to leakage. Bars represent normalized values against the standard wafer average, with error bars indicating statistical variability.

Summary/Conclusion. The transition from 150 mm to 200 mm SiC substrate has significant challenges, particularly regarding the impact of polytype inclusions and high densities of BPDs (BPDs) on wafer quality and device performance. Our study shows that these defects contribute to a substantial reduction in total usable area (TUA) compared to standard wafers. On the electrical side, while polytype inclusion is a localized and controlled phenomenon, the high density of BPDs has a considerable impact on the incidence of failures, including catastrophic failures and high-voltage losses. Advanced characterization techniques have revealed a clear correlation between defect

concentrations and the device failure location especially in wafers with polytype inclusion. Despite polytype inclusion, therefore, the overall distribution of functional and nonfunctional devices on wafers remained constant, suggesting a level of process stability even when working with materials outside typical commercial specifications. A prediction on the occurrence of failures in wafers with high density of BPDs, however, is currently not possible since they are distributed throughout the wafer. The future goal is to be able to find a clear correlation between BPDs and failures using advanced non-destructive analysis techniques. These results highlight the importance of ongoing efforts to improve crystalline quality and reduce defects in the production of 200-mm SiC wafers. Achieving these improvements will be critical to maximizing the yield and ensuring the reliability of SiC-based power devices, particularly as demand increases in high-volume industries such as automotive electrification.

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