Solid State Phenomena
ISSN: 1662-9779, Vol. 375, pp 49-53
doi:10.4028/p-Bwhh0v

Submitted: 2024-09-16
Accepted: 2025-03-10
Online: 2025-09-05

Characterization of Interface Trap and Mobility Degradation in SiC MOS Devices Using Gated Hall Measurements

Suman Das[1,a*], Daniel J. Lichtenwalner[1,b], Shane R. Stein[1,c], and Sei-Hyung Ryu[1,d]

[1]Wolfspeed, Inc., 4600 Silicon Drive, Durham, NC 27703, USA

[a]suman.das@wolfspeed.com, [b]daniel.lichtenwalner@wolfspeed.com, [c]shane.stein@wolfspeed.com, [d]sei-hyung.ryu@wolfspeed.com

Keywords: 4H silicon carbide (SiC), Hall measurement, mobility, interface traps, gate stress.

Abstract. Gated Hall measurements are conducted to calculate interface trap density of a nitric oxide (NO) annealed 4H silicon carbide (4H-SiC) MOSFET. The free carriers are measured using split CV method. Application of body bias confirms that the total trap quantity does not change at the interface when changing the electric field through body bias for a given device. The effect of positive gate stress on Hall mobility is also studied. A stress voltage of +36 V is applied for different stress times (0, 10, 30, 100, and 300 sec). With the increased stress time, the Hall mobility value drops at low gate voltages, while at higher gate voltages they merge. Higher stress creates more interface traps that in turn increase Coulomb scattering which lowers mobility at low gate voltages. The effect of gate stress on Hall mobility provides accurate insight of the channel behavior due to interface traps at 4H-SiC / SiO_2 interface.

Introduction

The performance of silicon carbide MOSFETs is limited by a high density of traps at the oxide semiconductor interface (4H-SiC/SiO_2) giving rise to low channel mobility for the MOSFETs. Several different gate oxide processes were employed in the past to reduce oxide semiconductor interface traps and to improve channel mobility. Post oxidation nitric oxide annealing [1,2] became the most extensively used industrial annealing treatment for power device fabrication. Some other approaches to change the interface that have been studied are introducing high k dielectrics [3,4], high temperature nitrogen annealing [5,6], or buried channel and/or counter doped channel MOSFETs [7,8].

To fully understand device characteristics and improve channel mobility, it is crucial to quantify these traps. Depending on the energetic location of these traps there are several methods [9] that can correctly quantify the traps, although most techniques only access traps at certain regions of the bandgap. One of the most effective methods for computing the total number of interface traps is gated Hall measurements [10-12], which give total trap quantities near the band edges, which directly affect carrier mobility. Hall mobility gives the actual value of carrier mobility which is directly extracted from the free carriers present in the channel. Thus, it gives an idea of how much the field effect mobility could be improved if most/all traps could be passivated, thus how much additional R_{on} improvement is possible in a planar channel device if trap density could be reduced. Due to the direct measurement of free carriers and mobility in a Hall mobility measurement, it can also be used to characterize interface degradation effects observed when threshold voltage shift is detected after gate stress [13,14].

In this work, gated Hall measurements are performed to quantify interface traps on the upper half of the bandgap. Furthermore, positive gate stress effects have been studied using lateral MOSFET I_d-V_{gs} evaluation, and gated Hall measurements. Gate stress effects on the field effect mobility has been studied before; however as employed here, the effect of gate stress on real (Hall) mobility can produce more insight.

Experimental Methods

Figure 1 shows a MOS Hall bar top-view. The Hall bar is fabricated on a Si-face 4° off-axis SiC (0001) wafer, on a 2×10^{17} cm^{-3} implanted Al-doped p-well, activated around 1600 ºC. This is a long channel (Lch=1 mm, Wch=200 um) lateral MOSFET with Hall voltage contacts, fabricated with a thermal oxide passivated with a NO anneal. Al was used as contact metal. The Hall bars are wire bonded on a larger sample holder and Hall measurements were performed at 25°C in a Lake Shore system with a permanent magnet of 1 Tesla.

Results

Figure 2 shows the measured MOS Hall mobility (μ_{Hall}) and field effect mobility (μ_{FE}) versus gate voltage at room temperature. The lower value of μ_{FE} comes due to the high density of interface traps. μ_{Hall} gives the actual value of the carrier channel mobility, directly measured. The value of the interface trap concentration is calculated in Fig. 3 from the measured Hall data. First, the total carrier concentration (n_{total}) is extracted from a split CV measurement. The free carrier concentration (n_{free}) is obtained from the gated Hall measurements and then subtracted from n_{total} to extract the total trapped charge density (n_{trap}). As the gate voltage increases, n_{trap} increases rapidly due to faster occupation of interface traps, while at high gate voltage the trapped charge density increases at a slower rate but doesn't saturate. These trap levels are in the upper half of the band gap and close to the conduction band edge, the density of which increases exponentially. Hall carrier concentration reveals that about half the channel charge is trapped and not contributing to channel current. Figure 4 shows the Hall and field effect mobilities at different body bias. The values of n_{trap} are extracted from these measurements as shown in Fig. 5. When the trapped carrier concentrations are plotted as a function of the gate overdrive

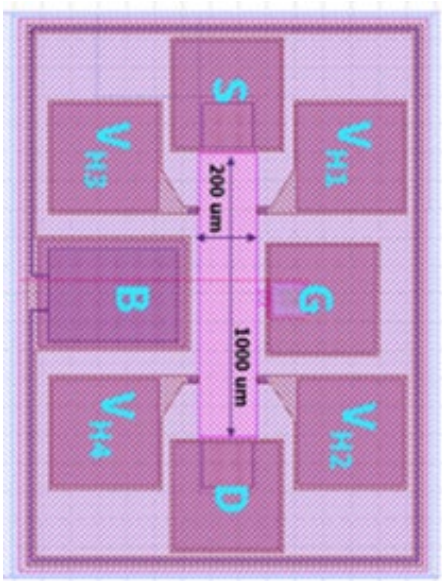

Fig. 1. Schematic diagram of Hall bar.

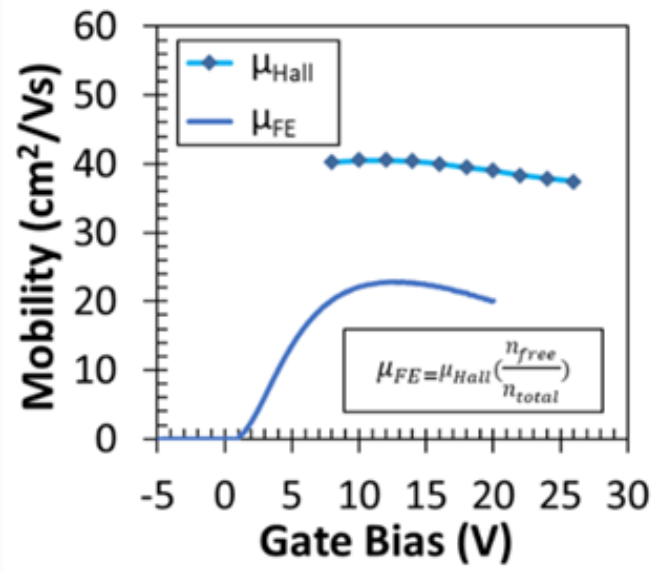

Fig. 2. Hall and Field effect mobility versus gate voltage for fabricated device.

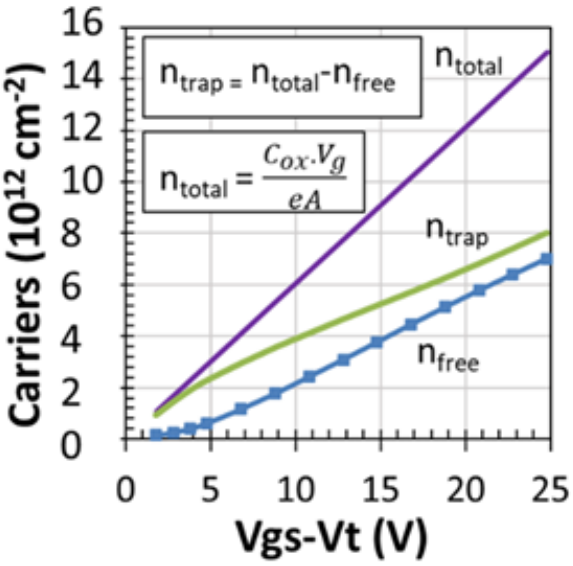

Fig. 3. Carrier concentration versus gate overdrive voltage showing total, free and trapped carriers.

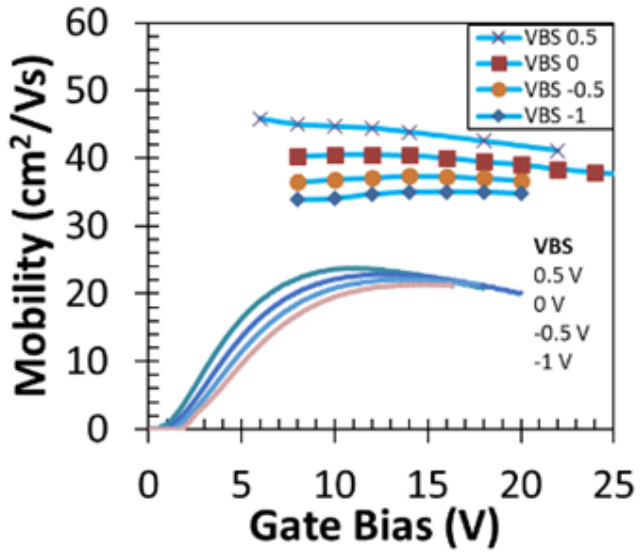

Fig. 4. Hall and field effect mobility versus gate bias at different body bias.

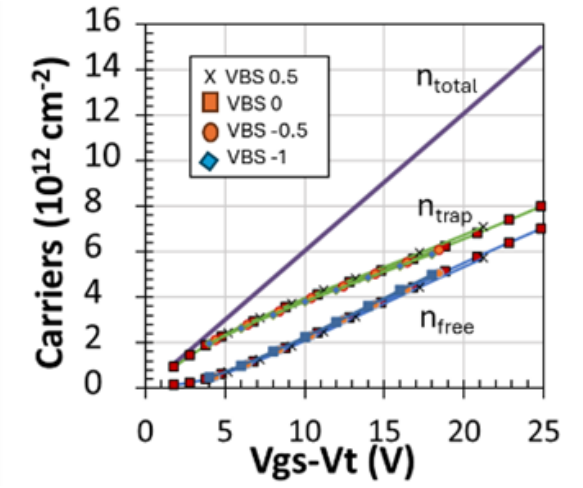

Fig. 5. Carrier concentration versus gate overdrive voltage at different body bias showing no change in trapped carriers due to different body bias

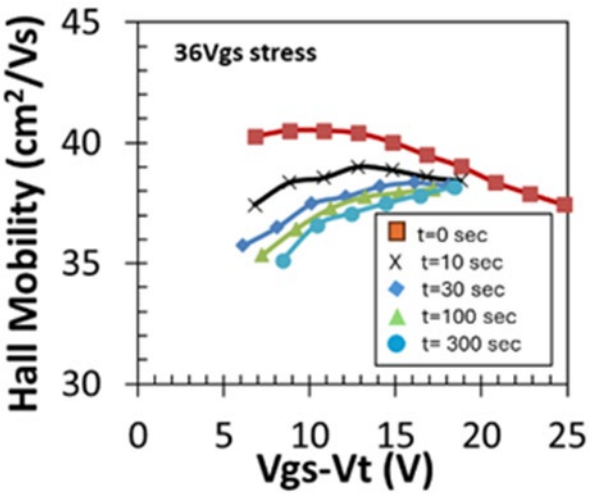

Fig. 6. Hall mobility versus gate overdrive voltage for a gate stress of +36 V for different times

voltage (V_{gs}-V_t), all the n_{trap} curves merge onto each other. This proves that body bias does not change the interface trap densities, only the value of transverse electric field changes, thus changing the mobilities.

Next, Hall measurements are used to perform a channel degradation characterization. The gate is stressed at +36 V for different times (0, 10, 30, 100, and 300 sec) and the Hall measurements are performed in between the stresses. Figure 6 shows Hall mobilities as a function of gate overdrive voltage after each stress condition. At low voltage the mobility reduces due to the stress; however, at high gate voltage they overlap. In addition, trapped charge densities are calculated after each gate stress condition. Figure 7 shows with increasing stress time, the free carrier density drops, indicating an increase of trapped charge carriers at the interface. Figures 6 and 7 are summarized in Fig. 8 which shows the changes of Nit and mobility (extracted at V_{gs}-V_t= 15 V) with stress time. Mobility decreases, and the value of Nit increases as the stress time increases, proving a direct correlation between N_{it} and mobility.

It can be concluded that, at zero stress time, half of the carriers are trapped and therefore do not take part in conduction resulting in higher channel resistance and channel mobility. As the stress time increases, more interface states are generated which captures more free carriers that in turn lowers the mobility at low gate voltages. However, Fig. 6 shows that at high gate voltage the mobility curves tend to merge with each other. The change in trap density increases Coulomb scattering at the interface and therefore lowers the mobility at low gate voltages. However, at high gate voltage mobility is governed by phonon scattering and they remain unchanged.

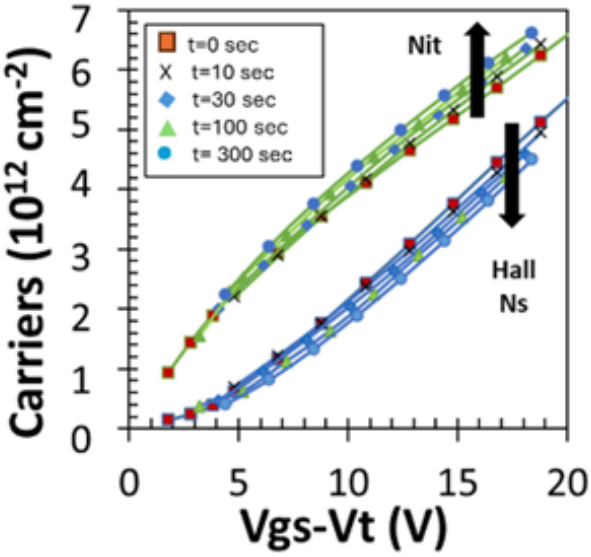

Fig. 7. Carrier concentration versus gate overdrive voltage showing that with the increase of stress time trapped carriers increasing and free carriers are decreasing.

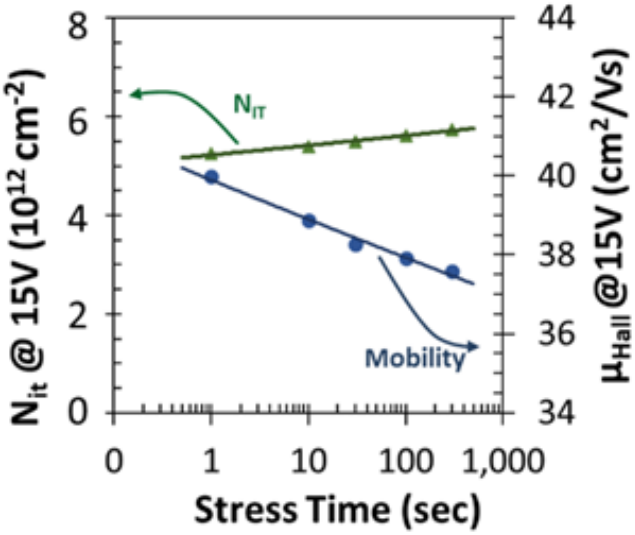

Fig. 8. Summary of calculated Nit and extracted mobility versus stress time shows direct correlation between increased trap levels and decreasing mobility.

Conclusion

In summary, gated Hall measurements show the effect of traps on carrier mobility and allow the calculation of trap concentration at the 4H-SiC/SiO_2 interface. The effect of gate stress on channel Hall mobility is observed here. An increase in stress time is seen to generate more traps at the interface. At low voltages mobilities are limited by Coulomb scattering and therefore shows a reduced value at increased stress. Whereas, at high gate bias mobilities are limited by phonon scattering for which the mobilities tend to merge at different stress timing. Overall, gated Hall measurements clearly reveal the free and trapped carrier densities and carrier mobility and is a powerful way to analyze channel degradation under stress, showing the effects on N_{it} and mobility.

References

[1] G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, R. K. Chanana, Robert A. Weller, S. T. Pantelides, Leonard C. Feldman, O. W. Holland, M. K. Das, and John W. Palmour, "Improved inversion channel mobility for 4H-SiC MOSFETs following high temperature anneals in nitric oxide," in *IEEE Electron Device Letters*, vol. 22, no. 4, pp. 176-178, April (2001).

[2] J. Rozen, A. C. Ahyi, Z. Xingguang, J. R. Williams, and L. C. Feldman, IEEE Trans. Electron Devices 58(11), 3808–3811 (2011).

[3] D. J. Lichtenwalner, L. Cheng, S. Dhar, A. Agarwal, and J. W. Palmour, Appl. Phys. Lett. 105, 182107 (2014).

[4] X. Yang, B. Lee, and V. Misra, “Effect of post deposition annealing for high mobility 4H-SiC MOSFET utilizing lanthanum silicate and atomic layer deposited SiO2,” in the 2nd IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 2014.

[5] K. Tachiki and T. Kimoto, "Improvement of Both n- and p-Channel Mobilities in 4H-SiC MOSFETs by High-Temperature N_2 Annealing," in *IEEE Transactions on Electron Devices*, vol. 68, no. 2, pp. 638-644, (2021).

[6] S. Das, H. Gu, L. Wang, A. Ahyi, L. C. Feldman, E. Garfunkel, M. A. Kuroda, S. Dhar; Trap passivation of 4H-SiC/SiO2 interfaces by nitrogen annealing. J. Appl. Phys. 7 June 2023; 133 (21): 215701.

[7] M. Okamoto, Y. Makifuchi, M. Iijima, Y. Sakai, N. Iwamuro, H. Kimura, K. Fukuda, and H. Okumura, Appl. Phys. Express 5(4), 041302 (2012).

[8] A. Modic, G. Liu, A. C. Ahyi, Y. M. Zhou, P. Y. Xu, M. C. Hamilton, J. R. Williams, L. C. Feldman, and S. Dhar, IEEE Electron Device Lett. 35(9), 894–896 (2014).

[9] M. E. Bathen, C. T.-K. Lew, J. Woerle,1 C. Dorfer, U. Grossner, S. Castelletto, and B. C. Johnson, Characterization methods for defects and devices in silicon carbide, J. Appl. Phys. 131, 140903 (2022).

[10] M. Noguchi, T. Watanabe, H. Watanabe, and N. Miura., Comparative Study of Hall Effect Mobility in Inversion Layer of 4H-SiC MOSFETs with Nitrided and Phosphorus-doped gate Oxides, IEEE Trans. Elec. Dev., 68, 12, (2021).

[11] S. Das, Y. Zheng, A Ahyi, M. A. Kuroda, and S. Dhar, Study of carrier mobilities in 4H-SiC MOSFETS using Hall analysis, MDPI Materials, 15, 19 (2022).

[12] S. Das, T. Isaacs-Smith, A Ahyi, MA Kuroda, S Dhar, High temperature characteristics of nitric oxide annealed p-channel 4H-SiC metal oxide semiconductor field effect transistors, JAP 130, 22 (2021).

[13] J. Berens; T. Aichinger, A straightforward electrical method to determine screening capability of GOX extrinsics in arbitrary, commercially available SiC MOSFETs, IEEE IRPS, pp. 1-5 (2021).

[14] A. K. Biswas, D. J. Lichtenwalner, S. Das, C. Isaacson, S. Ganguly, D. A. Gajewski, Effects of High Gate Voltage Stress on Threshold Voltage Stability in Planar and Trench SiC Power MOSFETs, Solid State Phenomena, 1662-9779, 358 (2023).