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Investigation on Bipolar Degradation Caused by Micropipe in 3.3 kV SiC-MOSFET

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Abstract. In this study, high current stress was applied to the body diode of SiC-MOSFETs, and chips exhibiting leakage current degradation due to the bipolar degradation phenomenon were analyzed to identify the crystal defects responsible for the abnormal leakage current. Failure analysis and defect inspection during the device fabrication process revealed that abnormal leakage occurred at the periphery of extended stacking faults originating from or near the micropipe itself. As these extended stacking faults also increase the forward voltage drop of MOSFETs, these results suggest that micropipe are critical defects in SiC-MOSFETs inducing both forward voltage and leakage current degradation in the bipolar degradation phenomenon.

Introduction

For decades, the bipolar degradation phenomenon has been a key issue faced by SiC-MOSFETs [1–5]. This phenomenon involves two types of degradation: an increase in the forward voltage drop (V_{DSon} of the MOSFET and V_{SDon} of body diode (BD)) and an increase in the leakage current of MOSFETs in blocking mode (I_{DSX}). Such degradation can cause MOSFET characteristics to deviate from datasheet values during operation, raising reliability concerns. The impact of bipolar degradation is particularly pronounced in high-power applications, where chips have large active areas and/or thick epitaxial layers to handle high currents and voltages. Therefore, careful consideration of this phenomenon is crucial for devices used in these applications.

Screening MOSFETs degraded by high current stress to the BD (BD stress) is the most direct and reliable method for managing this degradation. Consequently, this approach has been applied for many years in the screening process for some of high-voltage SiC-MOSFETs in mass production [6, 7]. However, because this method is relatively time-consuming, various alternative methods have been proposed to control this degradation mode [8–13]. Despite these efforts, fundamental studies on the bipolar degradation phenomenon itself are becoming increasingly important for addressing this issue more competitively. Although numerous studies on V_{DSon} degradation have been conducted over the years, research on I_{DSX} degradation remains limited [3–5, 7], and the defects responsible for this degradation are still unclear. Therefore, to fully understand the bipolar degradation phenomenon in SiC, studies focusing on I_{DSX} degradation are essential.

In this study, high current stress was applied to the BD of many 3.3 kV SiC-MOSFETs, and I_{DSX} degraded chips were identified. These degraded MOSFETs were then analyzed in detail, and the crystal defects responsible for this degradation phenomenon were identified.

Experimental

Figure 1(a) shows the planar-type 3.3 kV SiC-MOSFET fabricated on an n^+-type 4H-SiC substrate in this study. The size of the MOSFET was approximately 9×8 mm^2. During device fabrication, defect inspection using photoluminescence (PL) was performed after epitaxial growth and activation annealing. Figure 1(b) illustrates the experimental flow of this study. After the device fabrication process, an initial chip test was conducted to select "good" chips for the BD experiment. At this stage, these "good" chips exhibited no abnormal *I-V* characteristics or signs of degradation. Subsequently, a high current stress of 300 A/cm^2 at ~175ºC was applied to the BD of each chip. In the following chip test, chips with increased leakage current compared to the initial test were characterized as "I_{DSX} degraded chips", while those showing only an increase of V_{DSon} (without I_{DSX} degradation) were characterized as "V_{DSon} degraded chips". Furthermore, some of the I_{DSX} degraded chips were selected for failure analysis.

In the failure analysis, the points of abnormal leakage in the I_{DSX} degraded chips were first identified using photoemission microscopy from the backside of the chip after removing the backside electrode. Following this, the frontside electrodes and gate structures were removed, and PL imaging was performed to analyze the expanded single Shockley stacking fault (1SSF). The result of photoemission microscopy and PL imaging were then overlaid to identify the crystal defects causing abnormal leakage. In addition, defect inspection results from the device fabrication process were reviewed, and the crystal defects responsible for the degradation were determined.

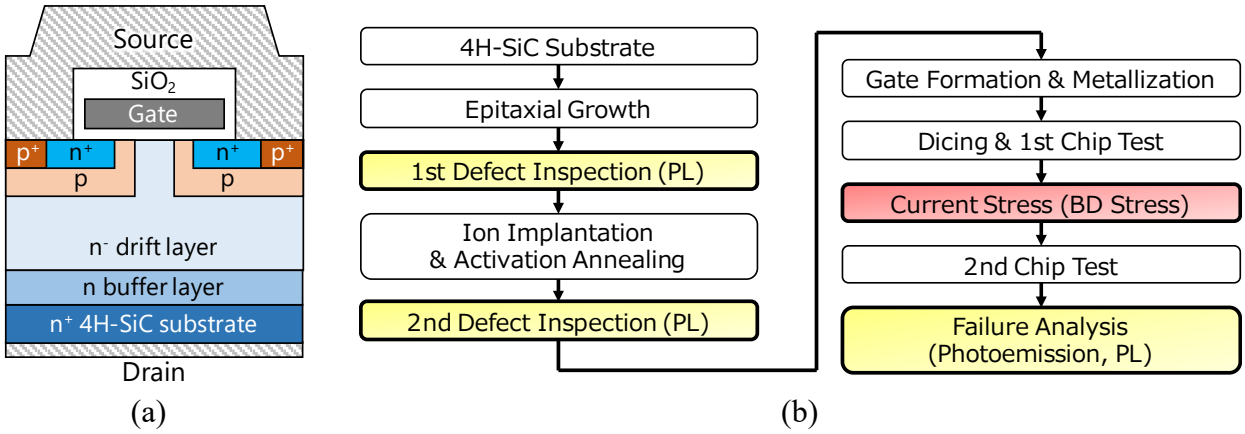
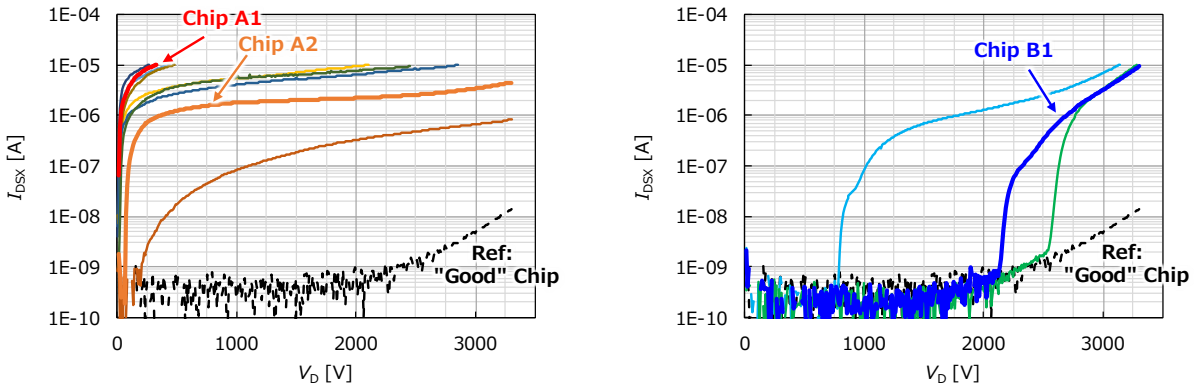


Fig. 1. (a) Schematic cross-section of the planar-type 3.3 kV SiC-MOSFET investigated in this study. (b) Flow-chart of the experimental procedure. During failure analysis, photoemission microscopy and PL imaging were conducted to identify the crystal defects.

Analysis of I_{DSX} Degraded Chips

BD stress was applied to more than 1,500 chips, and out of the 159 degraded chips, 45 showed I_{DSX} degradation. Figure 2 shows the leakage current characteristics of the I_{DSX} degraded chips (n = 13) selected for failure analysis. Compared to the passing chip, a clearly abnormal leakage current was observed. Two types of leakage current characteristics were identified: chips with abnormal leakage starting at a relatively low drain voltage (V_D) are referred to as Type A (Fig. 2 (a)), while those with leakage starting at a high V_D are categorized as Type B (Fig. 2 (b)).



(a) Type A (b) Type B

Fig. 2. Leakage current characteristics of I_{DSX} degraded chips. The compliance current in the measurement was set to 10μA. (a) Type A: Chips with abnormal leakage starting at low V_D. (b) Type B: Chips with abnormal leakage starting at high V_D.

Type A. Figure 3 shows the PL image and the results of photoemission microscopy for Chip A1, as shown in Fig. 2 (a). In the initial PL image taken during defect inspection (after epitaxial growth), a white dot was detected, identified as a micropipe [12]. After activation annealing, basal plane dislocations (BPDs) propagated from the micropipe, and 1SSFs expanded from the propagated BPDs and micropipe itself (more precisely, from the BPDs surrounding it) after the high current stress. Notably, the strain associated with the micropipe generates a BPD cluster around the micropipe in the epitaxial layer [14]. Overlaying the photoemission and PL image revealed abnormal leakage near the periphery of the expanded 1SSF originating from the BPDs.

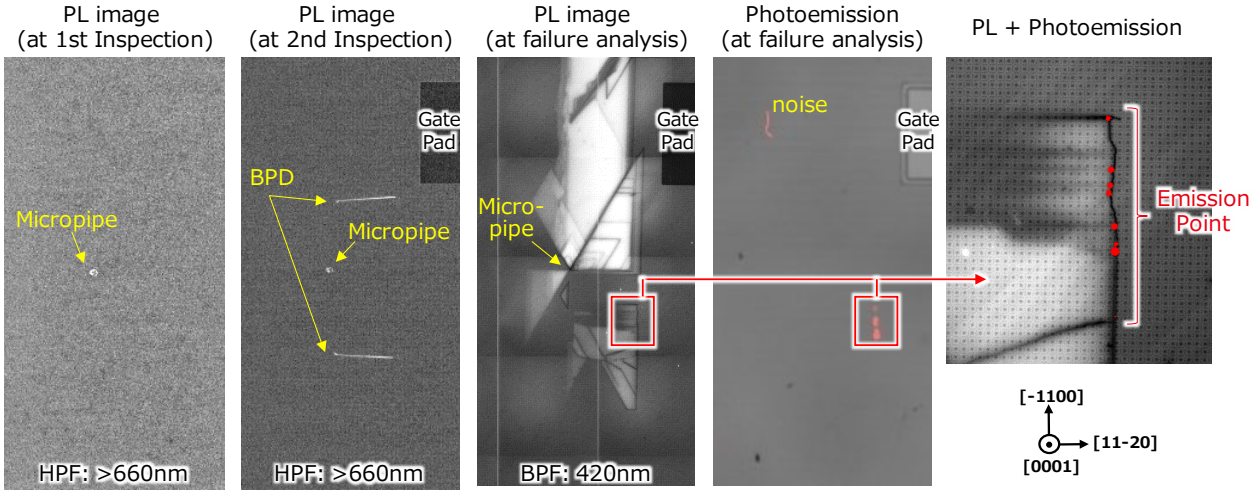


Fig. 3. PL images and photoemission microscopy results of Chip A1.

Figure 4 shows the analysis results for Chip A2 shown in Fig 2 (a). In this chip, BPDs also propagated after activation annealing, and photoemission was observed near the periphery of the expanded 1SSFs originating from these BPDs. Notably, the micropipe itself is in a neighboring chip, not within Chip A2. This indicates that the micropipe does not directly cause I_{DSX} degradation; rather, the propagated BPDs are responsible for the I_{DSX} degradation in Chip A2. Although failure analysis was not conducted on the neighboring chip containing the micropipe, it was categorized as an I_{DSX}-degraded chip after BD stress. This finding further supports the idea that BPDs propagate from the micropipe, leading to I_{DSX} degradation.

Analysis of other Type A chips, as shown in Fig. 2 (a), revealed that abnormal leakage in all such chips occurred similarly at the periphery of the expanded 1SSFs. In each case, the origins of the expanded 1SSFs were BPDs either propagating from the micropipe inside the chip or from a neighboring chip, indicating that these BPDs around the micropipe are the primary cause of the degradation observed in Type A chips.

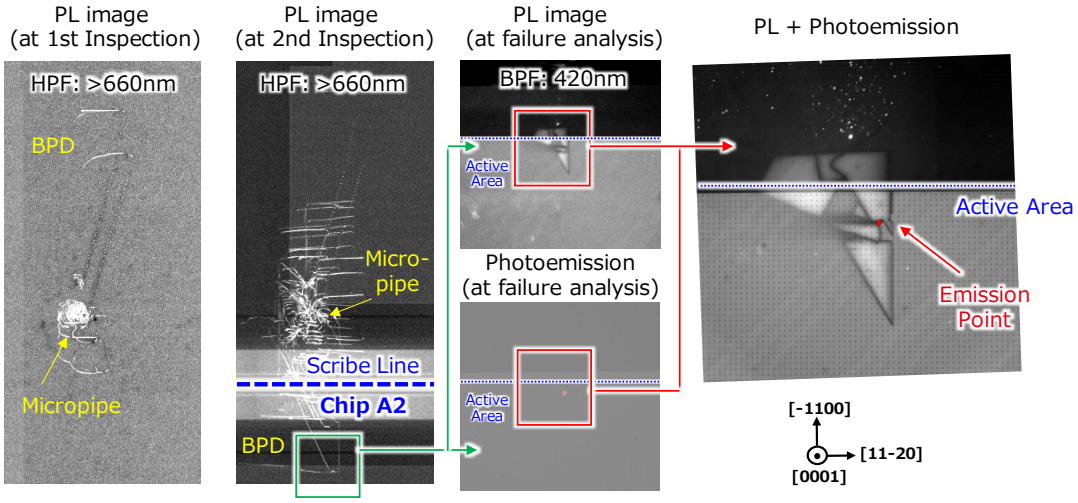


Fig. 4. PL images and photoemission microscopy results of Chip A2.

Type B. In Type B, abnormal leakage begins at a high V_D, unlike Type A. Figure 5 shows the analysis results for Chip B1 to determine if this type of degradation is also caused by the BPDs propagating from the micropipe, similar to Type A. The results in Fig. 5 show that 1SSF expanded from a micropipe, as observed in Type A; however, photoemission was detected near the micropipe itself. Unlike Type A, BPDs did not propagate from the micropipe after activation annealing in Chip B1, although BPDs are expected to be present around the micropipe since the 1SSF expanded following BD stress. This suggest that the specific BPDs causing I_{DSX} degradation in Type A may remain around the micropipe even after activation annealing, leading to degradation near the micropipe after BD stress. Similar results were observed for other Type B chips, as shown in Fig. 2 (b), where BPDs did not propagate from the micropipe after activation annealing. Thus, I_{DSX} degradation in both Types A and B is believed to be caused by similar BPDs around the micropipe.

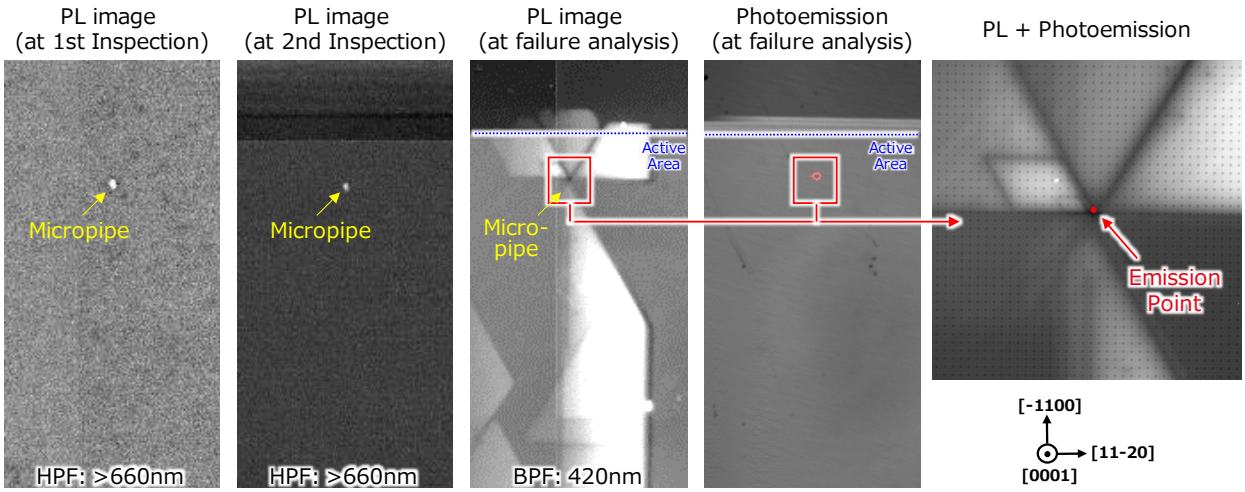


Fig. 5. PL images and photoemission microscopy results of Chip B1.

The difference in *I-V* characteristics can be discussed by the photoemission point: the periphery of 1SSF in Type A and near the micropipe in Type B. In Type A, emission is observed near the periphery of 1SSF, especially at the surface side of the chip. This indicates that the defective area causing I_{DSX} degradation is near the surface of the chip, requiring a very low V_D to create a high electric field sufficient to initiate abnormal leakage. In contrast, for Type B, the defective area causing abnormal leakage is likely near the starting point of 1SSF around the micropipe. Since the starting point of 1SSF is deep within the drift layer, a high V_D is needed to achieve a sufficiently strong electric field to induce abnormal leakage at that depth. Thus, although the *I-V* characteristics of Types A and B are different, the underlying physical mechanisms of the leakage current may be similar, with the observed differences attributed to the varying depths of the defective areas.

Discussion

Analysis of all chips shown in Fig. 2 revealed that I_{DSX} degradation was associated with BPDs around the micropipe. To estimate the origin of other I_{DSX}-degraded chips identified in this study, defect inspection results from the device fabrication process were examined to confirm whether a micropipe was present in each chip. Table 1 shows the number of degraded chips due to BD stress and those containing micropipes. Among the 45 I_{DSX} degraded chips, 43 contained micropipes. The two chips without micropipes were similar to Chip A2, where BPDs propagating from a micropipe in a neighboring chip caused I_{DSX} degradation. These results suggest BPDs around the micropipe were responsible for I_{DSX} degradation in all cases studied, as shown in Figs. 3–5.

Notably, I_{DSX} degradation is not caused by all micropipes. Table 1 shows that nearly twice as many V_{DSon}-degraded chips contained micropipes, without I_{DSX} degradation. PL analysis of these V_{DSon} degraded chips revealed the presence of expanded 1SSFs originating from the micropipe, similar to those in I_{DSX}-degraded chips shown in Fig. 3–5. In addition, 34 V_{DSon}-degraded chips without micropipes were associated with conventional 1SSFs, such as a bar-shaped 1SSFs originating from BPDs in the substrate [15], or triangular-shaped 1SSFs from BPDs that did not convert to threading-edge dislocations (TEDs) during epitaxial growth. This suggest that most BPDs frequently observed in past studies do not induce 1SSFs with abnormal leakage. Instead, a specific structure of "killer" BPDs is likely responsible for I_{DSX} degradation. These "killer" BPD may occur within micropipe or in the half-loop arrays observed in previous studies [4]. Identifying these structures is crucial for better understanding the bipolar degradation phenomenon and enhancing the reliability of SiC-MOSFETs. The high probability that such BPDs arise from the presence of a micropipe indicates that micropipes are a major crystal defect responsible for I_{DSX} degradation. Since expanded 1SSFs also cause V_{DSon} degradation, micropipes are critical for contributors to both V_{DSon} and I_{DSX} degradation in the bipolar degradation phenomenon.

Table 1. Result of high current stress testing (BD stress) and the number of degraded chips containing micropipes.

Test Chips [pcs]	After High Current Stress		
	I_{DSX} Degradation [pcs]	V_{DSon} Degradation [pcs]	Total [pcs]
>1500	45	114	159

	I_{DSX} Degradation [pcs]	V_{DSon} Degradation [pcs]
w/ Micropipe	43	80
w/o Micropipe	2*	34

*Degradation due to micropipe in the neighborhood chip

Summary

To further understand the bipolar degradation phenomenon in SiC, I_{DSX} degraded SiC-MOSFETs after BD stress were analyzed in detail. The findings suggested that micropipes was the root cause of all I_{DSX} degradation observed in this study. BPDs propagating from the micropipe after activation annealing led to I_{DSX} degradation in many chips, and even BPDs from neighboring chips could cause I_{DSX} degradation, despite the absence of micropipes in the degraded chips themselves. Given the micropipes can also induce V_{DSon} degradation, they must be considered as one of the most critical crystal defects in the bipolar degradation phenomenon.

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