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Exploring the Influence of Implant Profile and Device Design on Basal Plane Dislocation Generation in 1.2kV 4H-SiC Power MOSFETs

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Abstract. Several 1.2kV 4H-SiC devices of various cell architectures have been successfully fabricated by employing different P+ implantation conditions, resulting in varying levels of Basal Plane Dislocation (BPD) densities across the different device designs. It was found that by utilizing devices designed with an orthogonal P+ source layout as opposed to the traditional P+ stripe pattern, the long-term reliability under sustained 3rd Quadrant current stress conduction can be greatly improved even in devices with medium BPD densities. In addition, the use of the unipolar current of the JBSFET can further enhance long-term reliability under sustained 3rd Quadrant current stress by mitigating stacking fault expansion, even in devices with a high BPD density.

Introduction

The wide bandgap of 4H-SiC offers significant advantages over Silicon as a material of choice for high voltage power devices. This large bandgap, along with the ability to withstand high electric fields, allows for the creation of a thin and heavily doped epitaxial drift layer, resulting in a device with lower resistance when compared with silicon-based devices at voltage ratings greater than or equal to 600V [1]. Although the material properties of 4H-SiC are preferred for power device applications, the material itself provides unique challenges not encountered in silicon processing. For silicon processing, ion implantation can be performed at room temperature [2] however, for 4H-SiC processing, the ion implantation process has been performed at elevated temperatures to mitigate the generation of Basal Plane Dislocation (BPDs) which can lead to device degradation under bipolar current stress [3]. This high temperature ion implantation requires the use of an oxide blocking layer rather than the use of the photoresist layer, adding further processing steps and increasing the overall processing complexity, cost, and time [4].

Studies have been conducted to develop methods that mitigate lattice damage, such as BPDs, from ion implantation damage while simultaneously performing the process at room temperature. It was found that by carefully controlling the implantation profile through a combination of energy and dose adjustments, BPD generation can be suppressed even at doses approximately 10 times greater than the previously reported critical dose of 1×10^{15} cm^{-2} for Al ions at room temperature implantation [5,6]. Although the implantation profile is a vital component to consider in the mitigation of BPD formations, the proper architecture of the device active area is another essential consideration. By properly optimizing the active area cell architecture, potential BPD generation from the ion bombardment during RT implantation can be mitigated and thus stacking fault expansion can be suppressed. In this study, two MOSFETs with different cell layouts and a JBS-Diode integrated MOSFETs (JBSFETs) were examined under various aluminum ion implantation profiles to investigate the impact of cell architecture on BPD generation and subsequent ruggedness under continuous body diode current stress.

Device Design and Process Conditions

Fig 1. displays the top view of the various device types utilized in this study. The P+ stripe MOSFET adopts a conventional vertical power MOSFET architecture, where the source regions consist of long uninterrupted P+ implanted area in the y-direction to establish a contact to the P-Well. However, this approach leads to an excessively large cell pitch when compared to other design approaches. In the case of the Orthogonal P+ MOSFET cell structure, the overall cell pitch was reduced when compared to the traditional P+ stripe architecture by isolating the P+ implanted regions and placing them periodically in the orthogonal direction. This reduces the overall cell pitch, thus the overall specific on resistance ($R_{on,sp}$) is improved. For the JBSFETs, the Schottky openings also employ an orthogonal pattern as opposed to the traditional stripe type layouts. In this design, the dimensions of the ohmic area in between the Schottky contact areas measures 4µm, enabling greater conduction in the 3rd quadrant of operation without adversely affecting forward device characteristics of the JBSFET [7]. The optimal Schottky width to ensure sufficient current density while minimizing the leakage current was determined to be 2µm, which was integrated into the JBSFET structure. The current rating and size of the P+ Stripe MOSFETs were 6A and 0.85mm^2, respectively, and for the Orthogonal P+ MOSFET and JBSFET the current rating and size were 30A and 4.5mm^2, respectively. In addition, the P+ Stripe MOSFET utilized a floating field ring (FFR) edge termination whereas both the Orthogonal P+ MOSFET and JBSFET utilized a hybrid JTE edge termination [8]. A summary of the device parameters can be observed in Table 1.

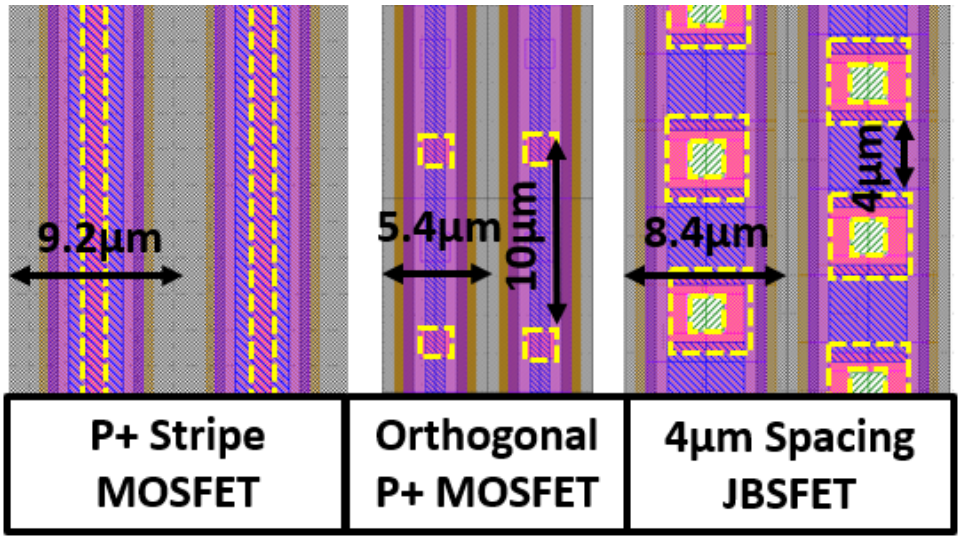

Fig. 1. Top layout views of the P+ Stripe MOSFET, Orthogonal P+ MOSFET and the 4µm Spacing JBSFET employed within this study. Boundaries of the P+ implanted areas are highlighted in yellow for each device active area cell.

Table 1. Parameter summary of the devices utilized within this study.

Device Type	Active Area [mm^2]	Current Rating [A]	Cell Pitch [µm]	Schottky Open [µm]	Edge Termination
P+ Stripe	0.85	6	9.2	N/A	FFR
Ortho P+	4.5	30	5.4	N/A	Hybrid
JBSFET	4.5	30	8.4	2	Hybrid

For each device type, several different P+ source implantation profiles were utilized, as shown in Fig. 2. The three different implantation profiles were designed to create devices with low, medium, and high BPD-generation throughout the device structure, allowing for the assessment of BPD effects on each device cell architecture. This was achieved by varying the doping concentrations (either medium (M) or high (H)) for both the surface (S) and the body (B) of the junction [5,6]. The low BPD-generating 'HSMB' profile has a total aluminum dose of 9×10^{15} cm^{-2} (referred to as 9x), while the medium BPD-generating 'MSHB' profile had a total aluminum dose of 4.95×10^{15} cm^{-2} (referred

to as 5x). Lastly the high BPD generating profile has a near uniform surface and body concentration with a total dose of 5×10^{15} cm^{-2} and thus can be simplified to the '5x RT Box' profile. All profiles were implanted at room temperature (RT); however, the medium damage 'MSHB' profile was also implanted at an elevated temperature of 600°C (HT) for comparison purposes. The remaining implantations steps (i.e. JFET, PWell, N+ and JTE) used all implanted at room temperature.

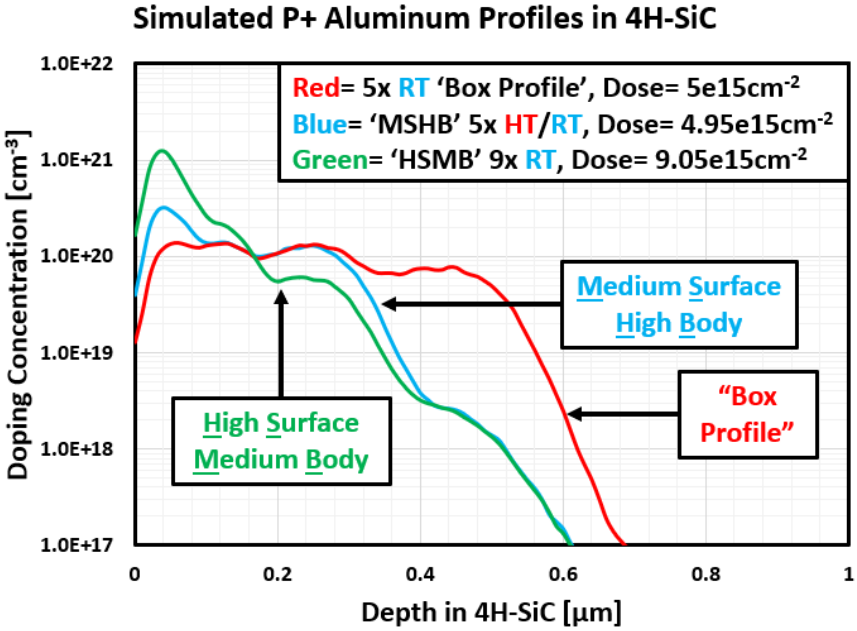

Fig. 2. Simulated aluminum concentration profiles utilized to form the P+ implanted regions within the devices by varying the surface and body of the main junction. All profiles were implanted at room temperature; however, the 'MSHB' profiles were also implanted at an elevated temperature for comparison purposes.

Results and Discussion

The representative X-Ray topography maps, along with their corresponding BPD densities can be observed in Fig. 3 and Table 2 respectively. For the low and medium damage implantations, BPDs can be observed forming around both edge terminations and periphery regions in all three device architectures whereas negligible BPD generation is observed in the devices fabricated with the 5xHT profile. Since all BPD generation can be observed along areas subjected to the P+ implantation, this defect generation was process related as opposed to being native to the 4H-SiC wafer. For the low damage implantation, the estimated BPD density was $2x10^3cm^{-2}$ and $5x10^3cm^{-2}$ for the hybrid JTE and FFR edge terminations, respectively. For the medium damage implantation estimated BPD density was $5x10^3cm^{-2}$ and $2.1x10^4cm^{-2}$ for the hybrid JTE and FFR edge terminations respectively. In both implantation conditions, the FFR edge termination generated a greater amount of BPDs and no BPDs were observed originating within the active area [9]. For the high damage implantation, BPD generation can be observed around the edge terminations, and periphery regions, for the nominal MOSFETs and JBSFETs with a BPD density of approximately $2.5x10^4cm^{-2}$. However, for the P+ stripe MOSFET fabricated under the high damage implantation condition, BPD generation was observed throughout the entirety of the device, including the active area due to the greater amount of mismatch lattice stress between the PWell and P+ regions [10]. The BPD density for both the active area and FFR edge termination of the P+ Stripe MOSFET was too large and therefore, an exact density could not be determined.

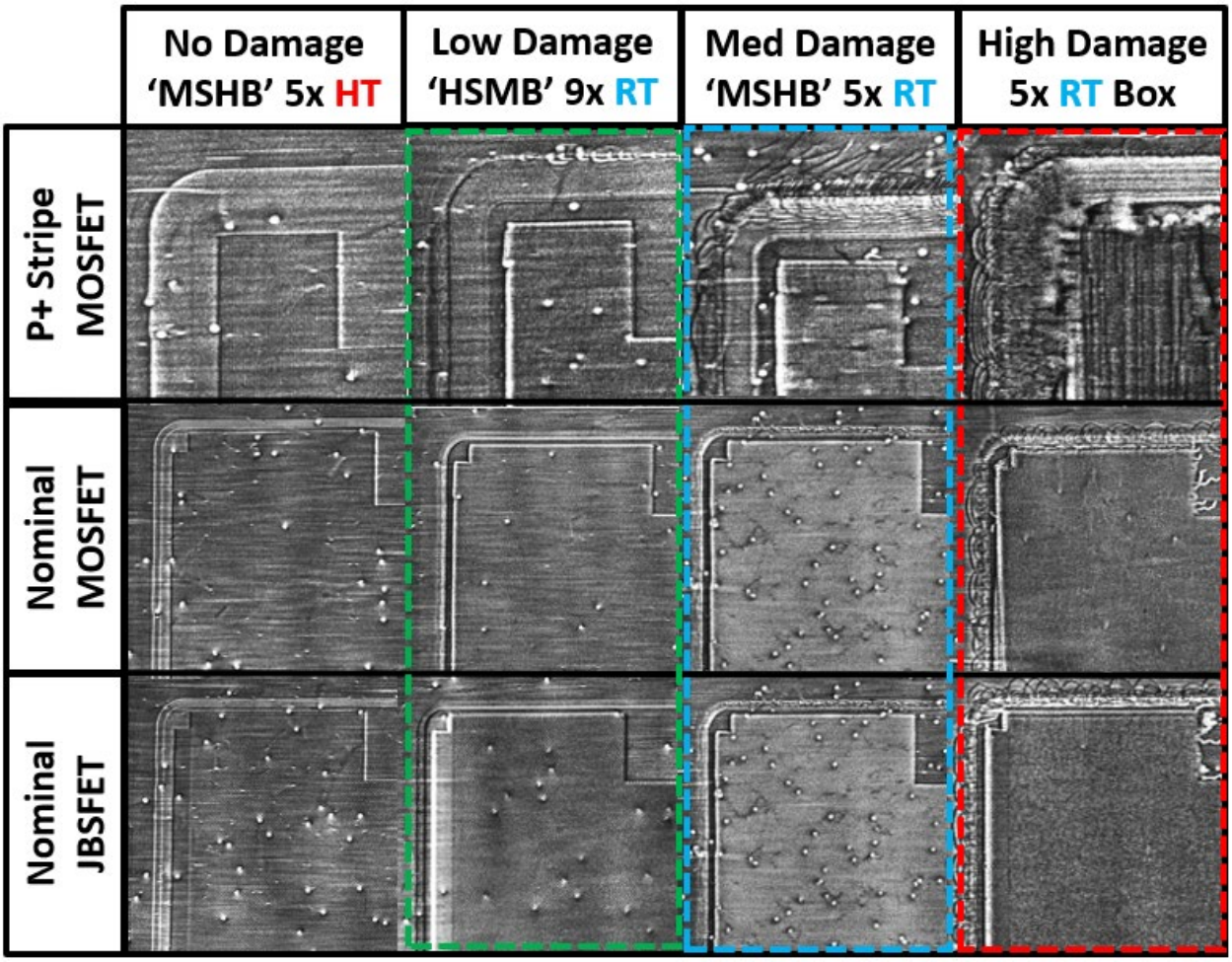

Fig. 3. Representative X-Ray topography images of the P+ stripe MOSFET, Nominal MOSFET, and Nominal JBSFET are presented under each of the no, low, medium, and high damage P+ implantation conditions. BPD generation can primarily be observed within the edge termination, and periphery regions of the devices.

Table 2. BPD density calculations of the active device and edge termination areas for each device fabricated utilizing the various implantation conditions.

Device Area	Device Design	BPD Densities for each Implantation Condition [cm^2]			
		MSHB 5x HT	HSMB 9xRT	MSHB 5xRT	5xRT Box
Active Area	P+ Stripe	~0	~0	~0	$>10^5$
	Ortho P+	~0	~0	~0	~0
	JBSFET	~0	~0	~0	~0
Periphery and Edge Termination	FFR	~0	$0.5x10^4$	$2.1x10^4$	$>10^5$
	Hybrid*	~0	$0.2x10^4$	$0.5x10^4$	$2.5x10^4$

*Hybrid BPD density was taken from the Nominal MOSFET structures.

The static measurements and continuous body diode stress conditions used are depicted in Fig. 4. Initially, the devices underwent screening for their forward IV, forward blocking and 3rd Quadrant output characteristics. This was followed by a continuous 15-minute body diode current stress at 125A/cm^2. To minimize the 3rd Quadrant channel current, a bias of -5V was applied to the gate, effectively shutting off the channel and allowing the current to flow solely through the body diode of the device. This process was repeated until the device was stressed for a total of 90 minutes. The wafer temperatures were monitored to keep the devices at approximately 25˚C for the entire duration of the body diode current stress cycle. This procedure was performed for each device type and implantation condition.

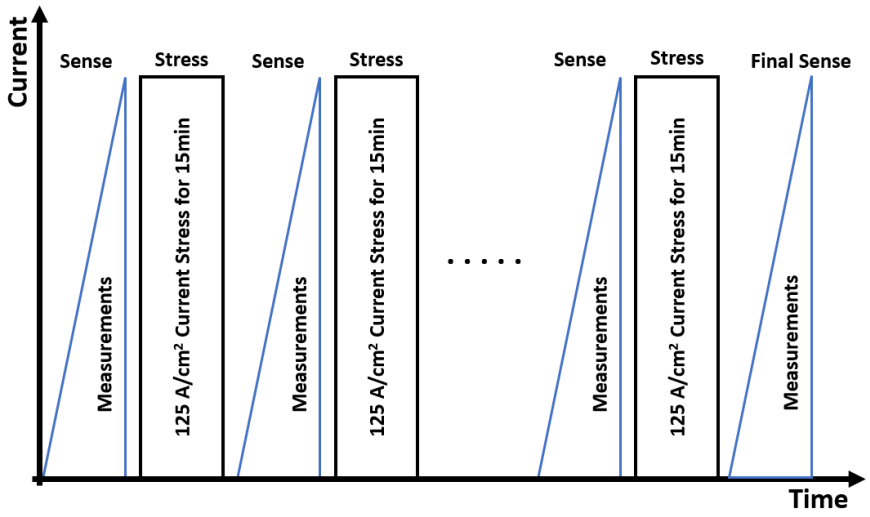

Fig. 4. Simplified schematic highlighting the measurement performed for each device analyzed within this study. Each sense condition consisted of a forward IV, forward blocking, and 3rd quadrant output measurement followed by a 125A/cm^2 current for 15 minutes. This was then repeated until each device had been stressed for a total of 90 minutes.

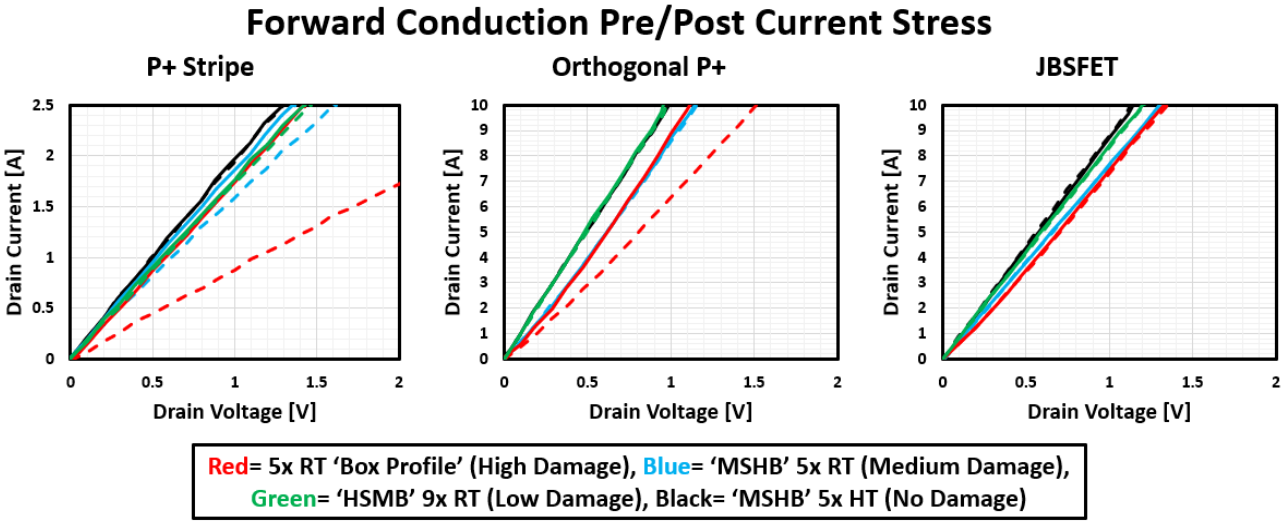

Fig. 5. Forward conduction characteristics of the P+ stripe MOSFET, Orthogonal P+ MOSFET, and JBSFET fabricated with different P+ profiles, before (Solid) and after (Dashed) the 125A/cm^2 current stress analysis. Measurements were performed on wafer and at a gate bias of V_{gs}=20V.

Fig. 5 shows forward conduction output characteristics both pre and post current stress for the various device types, respectively. Notably, even before current stress the 9xRT devices exhibited output characteristics similar to the 5xHT implanted devices, whereas non-linear pinching behaviors were observed within the 5xRT and 5xRT Box implanted devices [6]. However, after the current stress analysis, significant device degradation is evident in the 5x RT Box P+ Stripe MOSFET, 5x RT Box Orthogonal P+ MOSFET, and 5x RT P+ Stripe MOSFET. The on-resistance (R_{on}) for the 5x RT Box P+ Stripe MOSFET, 5x RT Box Orthogonal P+ MOSFET, and 5x RT P+ Stripe MOSFET increased by 102%, 37.8%, and 16.5% respectively. In contrast, no discernible differences are observed in the remaining devices, likely due to their low BPD density within the active area or by leveraging the unipolar current within the JBSFET devices.

The forward blocking characteristics of the devices, both before and after the current stress measurements, are observed in Fig. 6. Leakage current and forward blocking behaviors remained relatively constant throughout all devices both before and after the current stress. However, it is noteworthy that the leakage current was significantly higher in the RT implanted P+ Stripe MOSFETs

before stress due to the use of the FFR edge termination [9]. This higher leakage current was also observed within the orthogonal P+ 5xRT device [6], and within the RT implanted JBSFETs due to integrated JBS diode [5]. Additionally, the 5x RT Box profile showed no blocking capabilities with all 3 device types even prior to the current stress. As a result, the combination of these already high leakage currents or no blocking capabilities led to minimal observable differences, unlike what was seen within the forward conduction.

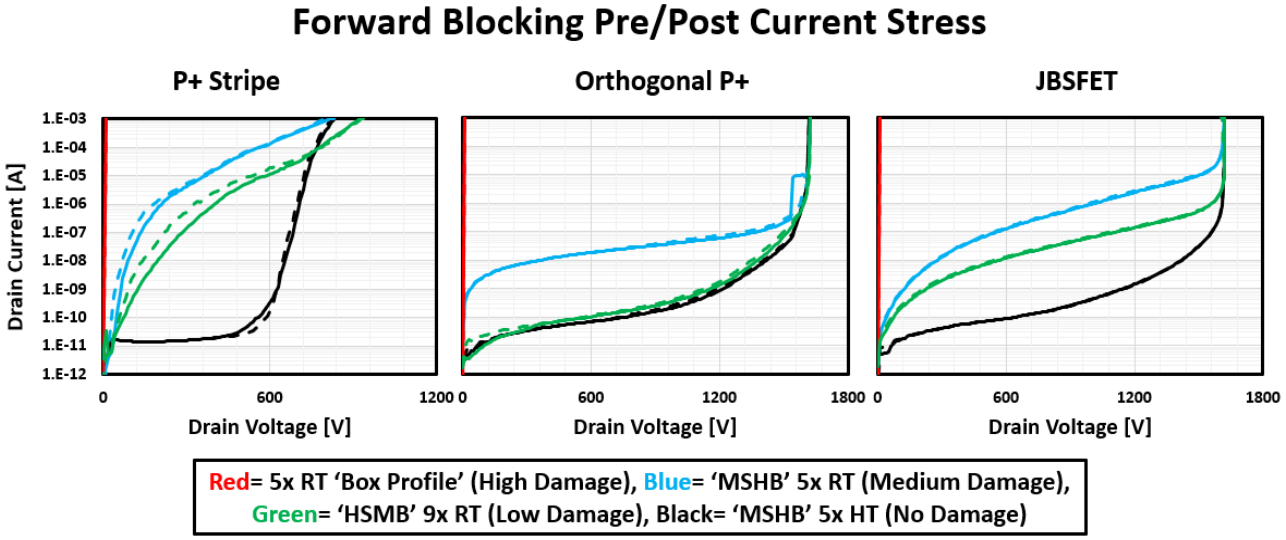

Fig. 6. Forward blocking characteristics of the P+ stripe MOSFET, Orthogonal P+ MOSFET, and JBSFET fabricated with different P+ profiles, before (Solid) and after (Dashed) the 125A/cm^2 current stress analysis. Measurements were performed on-wafer and at a gate bias of V_{gs}=-5V to minimize leakage through the channel.

Fig. 7 shows the 3rd quadrant output characteristics, both before and after the current stress for the various devices analyzed. Similar to the forward conduction results, device degradation is evident only with the output of the 5x RT Box P+ Stripe MOSFET, 5x RT Box Orthogonal P+ MOSFET, and 5x RT P+ Stripe MOSFET, following the current stress. The 3rd quadrant forward voltage drop (V_f) increased by 14.6%, 8.6%, and 2.5% for the 5x RT Box P+ Stripe MOSFET, 5x RT Box Orthogonal P+ MOSFET, and 5x RT P+ Stripe MOSFET respectively. Additionally, negligible changes were observed in the output characteristics of the remaining structures, due to their low BPD densities within the active area or the use of unipolar current as seen in the JBFET devices. Although no degradation is observed within the JBSFETs, the output of the integrated JBS diode was still hindered prior to the current stress due to the high presence of BPDs within the 5xRT and 5xRT Box implanted devices when compared to the 9xRT and 5xHT devices[5].

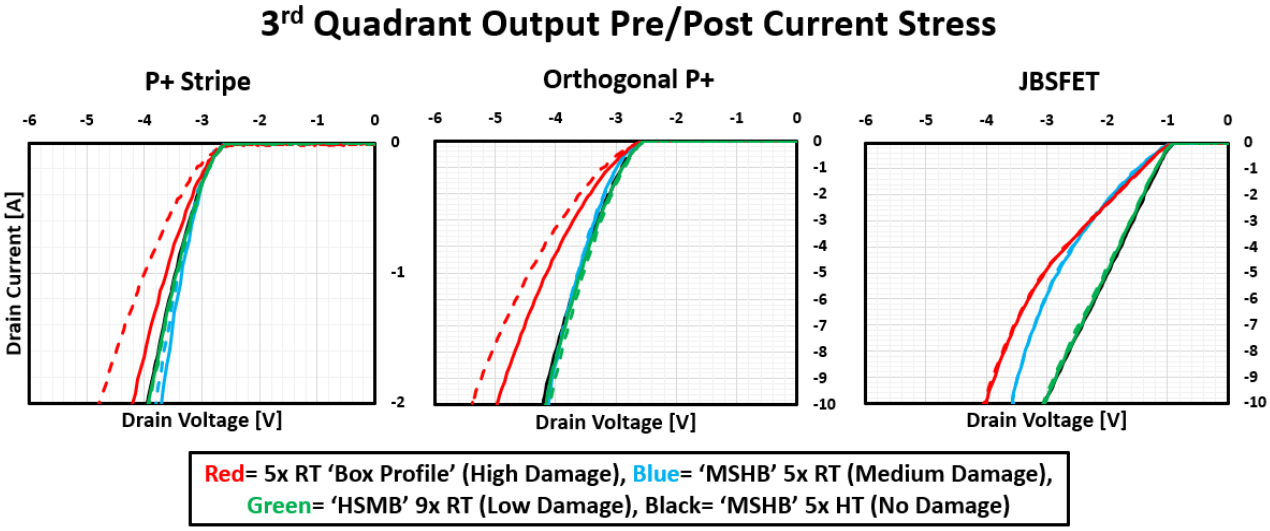

Fig. 7. 3rd Quadrant output characteristics of the P+ stripe MOSFET, Orthogonal P+ MOSFET, and JBSFET fabricated with different P+ profiles, before (Solid) and after (Dashed) the 125A/cm^2 current stress analysis.

Table 3. shows the overall degradation of the various device architectures, for the forward IV and 3rd quadrant output respectively. All devices fabricated under the negligible and low damage implantation condition exhibited no observable degradation in the forward IV, forward BV, and 3rd quadrant output characteristics. Under the medium damage implantation, despite the presence of BPDs, the orthogonal P+ structure of the nominal MOSFET showed resilience to device degradation, and to a lesser extent in the high damage scenario, when compared to the traditional P+ stripe MOSFET under the same fabrication condition. However, the JBSFETs showed no degradation even under the high BPD density implantation condition as the unipolar nature of the JBSFETs prevents the electron hole recombination utilizing BPDs and thus prevent device degradation through SF expansion.

Table 3. Percentage change in both $R_{on,sp}$ and 3rd Quadrant V_f for the various device architectures and implantation conditions after the current stress analysis.

Device Type	Increase in R_{on}				Increase in 3rd Q V_f			
	5xHT	9xRT	5xRT	5xRT Box	5xHT	9xRT	5xRT	5xRT Box
P+ Stripe	~0%	~0%	16.5%	102%	~0%	~0%	2.5%	14.6%
Ortho P+	~0%	~0%	~0%	37.8%	~0%	~0%	~0%	8.6%
JBSFET	~0%	~0%	~0%	~0%	~0%	~0%	~0%	~0%

Summary

Several device architectures have been successfully fabricated under various implantation conditions, resulting in a wide range of BPD densities within the devices. Even under high BPD-generating implantations, the device and cell layout can be optimized to reduce the effects of device degradation. By utilizing the orthogonal P+ source pattern, the BPD density within the active area can be suppressed, improving long-term reliability compared to the P+ stripe MOSFET counterpart. However, by switching to a unipolar device, such as the JBSFET, device degradation can be heavily suppressed even in high BPD density devices, resulting in improved long-term reliability. While the implantation profile has proven to be a critical factor, careful consideration for the cell architecture was shown to be another vital factor in suppressing BPD generation and subsequent SF expansion. Therefore, proper control over both aspects is essential for fully implementing room temperature implantation, increasing device reliability and longevity, while simultaneously reducing processing complexity, cost, and time.

Acknowledgements

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References

[1] B Jayant Baliga, *Fundamentals of power semiconductor devices*. New York, NY: Springer, 2008, Chap.3, pp. 91-155.

[2] S.Wolf and R.N. Tauber, *Silicon Processing for the VLSI Era Volume 1:Process Technology*. Sunset Beach, U.S.A. : Lattice Press, 1986. pp. 280-283.

[3] A. Agarwal, H. Fatima, S.Haney, S.-H. Ryu, "A New Degradation Mechanism in High-Voltage SiC Power Mosfets". *IEEE Electron Device Letters vol. 28, no. 7, pp.587-589, 2007*. doi.: 10.1109/LED.2007.897861.

[4] D. Kim, N. Yun and W. Sung, "Advancing Static Performance and Ruggedness of 600 V SiC MOSFETs: Experimental Analysis and Simulation Study," 2021 IEEE International Reliability Physics Symposium (IRPS), 2021, 10.1109/IRPS46558.2021.9405109.

[5] S. A. Mancini *et al*., "Static Performance and Reliability of 4H-SiC Diodes with P+ Regions Formed by Various Profiles and Temperatures," 2022 IEEE International Reliability Physics Symposium (IRPS), 2022, pp. P62-1-P62-6, doi: 10.1109/IRPS48227.2022.9764538.

[6] S. A. Mancini *et al*., "Investigation of Static Performances of 1.2kV 4H-SiC MOSFETs Fabricated Using All 'Room Temperature' Ion Implantations," in *IEEE Journal of the Electron Devices Society*, vol. 12, pp. 150-158, 2024, doi: 10.1109/JEDS.2024.3359974.

[7] S. A. Mancini *et al*., "Increased 3rd Quadrant Current Handling Capability of 1.2kV 4H-SiC JBS Diode-Integrated MOSFETs (JBSFETs) with Minimal Impact on the Forward Conduction and Blocking Performances," *2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2021, pp. 101-106, doi: 10.1109/WiPDA49284.2021.9645152.

[8] W. Sung and B. J. Baliga, "A Near Ideal Edge Termination Technique for 4500V 4H-SiC Devices: The Hybrid Junction Termination Extension," *IEEE Electron Device Letters*, vol. 37, no. 12, pp. 1609–1612, Dec. 2016, doi: 10.1109/led.2016.2623423.

[9] S. A. Mancini *et al*., "Edge Termination Design Considerations for 1.2kV 4H-SiC MOSFETs While Utilizing Room Temperature Ion Implantations," *2023 IEEE 10th Workshop on Wide Bandgap Power Devices & Applications (WiPDA)*, Charlotte, NC, USA, 2023, pp. 1-6, doi: 10.1109/WiPDA58524.2023.10382208.

[10] Z. Chen et al, "Analysis of Basal Plane Dislocation Motion Induced by P+ Ion Implantation Using Synchrotron X-ray Topography" *2022 19th International Conference on Silicon Carbide and Related Materials (ICSCRM)*, September 2022, doi: 10.4028/p-4mo61y.