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Coherency between Epitaxial Defectivity, Surface Voltage, Photoluminescence Mapping and Electrical Wafer Sorting for 200mm SiC Wafers

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Abstract. Electrical Wafer Sorting (EWS) on 12 000, 650 V SiC MOSFETs devices from 7 wafers of 200 mm 4H-SiC are compared with electrical deviations and defectivity of initial epitaxial layers measured using Charge biased non-Contact Voltage imaging, QUAD (Quality Uniformity And Defects), and optical surface detection with PL-imaging, respectively. We successfully demonstrate an increased prediction rate in both KR (kill-ratio) and YI (yield-impact) compared to conventional PL-imaging. It is also shown that QUAD not only supplements PL-imaging but supersedes it predicting failure in some electrical test conditions. We therefore show that the combination of QUAD and PL-imaging results significantly improves the accuracy of device failure prediction by uniquely locating faults in the wafers, and thus, improving foresight of successful device fabrication.

Introduction

Wide-bandgap semiconductor-based electronics are in constant development, with Silicon Carbide (SiC) leading the way in next generation power devices. In particular within power electronics, SiC carries intrinsic advantages thanks to its higher thermal operation and lower switching losses compared to Silicon-based (Si) electronics [1]. However, the desirable properties of SiC comes with both a higher manufacturing cost and lower device-yield compared to the more conventional and malleable Si, owing to the complicated crystal growth process and subsequent manufacturing of SiC devices. Additionally, it is well known that the presence of surface and crystallographic defects impact the quality of epitaxial layers [2-4]. However, it is important to gauge the significance of each defect, to create models that can accurately predict the final device yield by adding additional layers to the conventional critical and non-critical classification [2-5]. Therefore, the importance of reliable metrology at an early stage of device making is, not only critical to improve yield prediction accuracy, but also to steer material to the appropriate application, and close feedback loops, ensuring improvement in the subsequent material growth and manufacturing.

Herein we follow up on the study conducted and presented in the prior year on the topic of linking epitaxial defectivity with surface voltage and photoluminescence (PL) mapping of epitaxially grown SiC-layers on 200mm 4H-SiC substrates [6]. We combined the industry standard way of classifying topographical variations, reflectance, photoluminescence, and phase shift, by using optical surface detection systems, with surface voltage mapping using non-contact C-V (CnCV) metrology

incorporating the "QUAD" (Quality Uniformity And Defects) method [7]. The QUAD technique uses whole wafer surface voltage mapping after charging the SiC surface to deep depletion. Electrically active defects are detected as cluster regions or spots with respect to the surrounding defect area. Applying a combined QUAD defect detection methodology, we have facilitated comparison to final EWS of SiC MOSFET devices using surface voltage contrast and in-die voltage values using a die-bin map analysis. Die-bin map creation converts the surface voltage map into die grids, which in turn can be aligned to match various die-sizes of devices in production. This type of analysis gives the possibility to consider a die failed if the depletion voltage is below or the reverse bias leakage current is above a defined threshold value. By looking at the analogy of die failures related to some of the EWS parameters of the MOSFET, such as Gate and Drain leakage current (I_{GSS}, I_{DSS}), or Threshold Voltage (V_{TH}), it is possible to compare QUAD wafer bin map results to EWS tests.

Experimental Details

In this work, 7 wafers of 200 mm 4H-SiC with n-type SiC epitaxial layers were used. All substates were grown with a layer thickness of 6 µm and a doping concentration of $1x10^{16}$ cm^{-3}, on top of a 0.5 µm thick buffer-layer with a doping concentration of $1x10^{18}$ cm^{-3}. For the PL-mapping we used a KLA Candela 8520 and for surface voltage mapping we used a Semilab CnCV 210 [7-8]. With the CnCV tool we identified electrically active defects using the incorporated QUAD technique which involves whole wafer corona charging of SiC wafers to deep depletion followed by measurement of the surface voltage using a vibrating Kelvin Probe [6, 9]. **Fig. 1** shows a QUAD map of depletion voltage. This map is then used to create a bin-die map using a particular device die size and depletion voltage threshold.

Following initial data acquisition, the wafers were used to produce ~12 000, 650 V SiC n-channel MOSFET devices. To quantify yield and individual device failures, EWS results were used to check the functionality of each die by applying various conditions and evaluating the performance and electrical characteristics. Results from PL-mapping, QUAD and EWS are parsed and processed to a matching die-coordinate system, then spatially correlated, in order to see optically captured defectivity overlapping with reduced depletion voltage sites, and EWS results; see an example of one wafer in **Fig. 2**. With the results, yield impact was calculated using a method based on kill-ratio (KR) analysis, first published by M. Ono et al. [10] for Si integrated circuits using a four-category approach, later extended to SiC Trench-MOSFET devices by D. Baierhofer et al. [11], see **Eq. 1**.

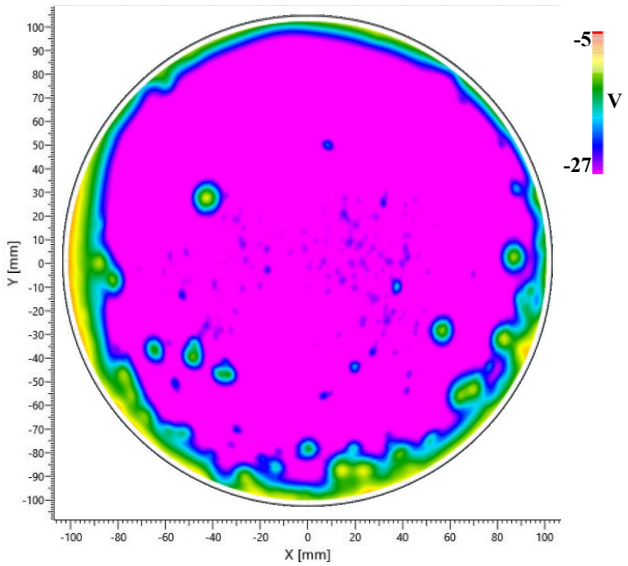

Fig. 1. A QUAD map showing localized areas with lowered depletion voltage due to electrically active defects.

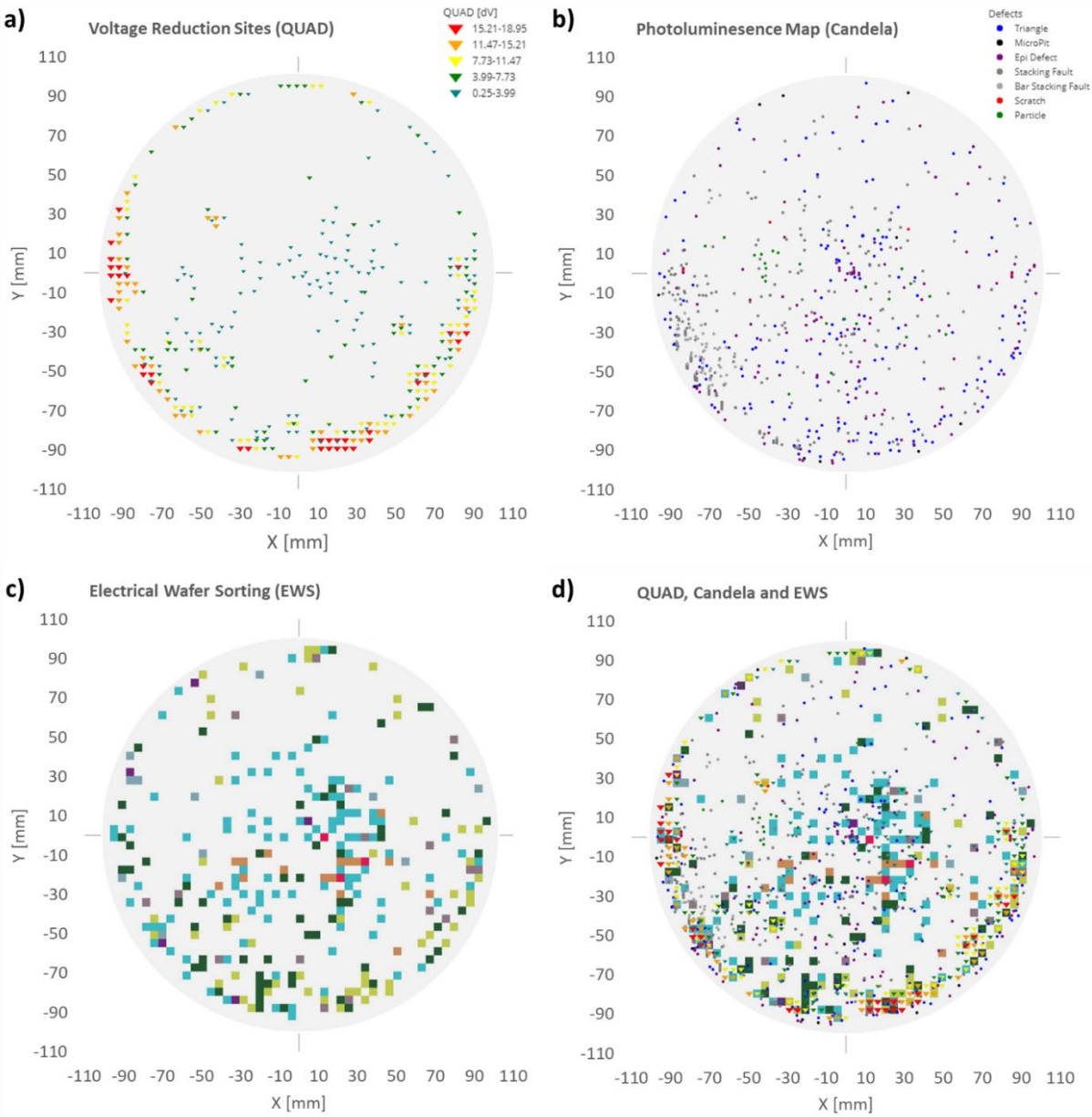

Fig. 2. Example of wafer map with a) QUAD measured reduced depletion voltage sites, b) photoluminescence map and c) various electrical wafer sorting parameters map superimposed to form d) a combined map. Each color from the EWS map corresponds to different pass (white) or fail conditions (color).

$$KR = 1 - \frac{\frac{G_D}{G_D + B_D}}{\frac{G_{ND}}{G_{ND} + B_{ND}}} \quad \textbf{(1)}$$

Either the die shows good or bad electrical properties after EWS testing, denoted as *G* or *B*. In both cases it can either be, or not be, occupied by a defect or a reduced voltage site, subscripted as *D* and *ND*, respectively, see **Table 1**.

Table 1. The four-category approach utilized in **Eq. 1**.

	Defect or Reduced Depletion Voltage Sites	No Defect or Reduced Depletion Voltage Sites
Good	G_D	G_{ND}
Bad	B_D	B_{ND}

Furthermore, yield-impact, *YI*, can be calculated using the *KR*:

$$YI = \frac{KR(G_D + B_D)}{G_D + B_D + G_{ND} + B_{ND}} \quad \textbf{(2)}$$

Nominal yield-impact, YI_N, can be calculated using Poisson distribution yield model [12]:

$$YI_N = 1 - e^{-\frac{KD}{TD}} \quad \textbf{(3)}$$

Where KD and TD are the killer- and total-number of defects, or reduced depletion voltage sites. **Fig. 2** shows an example of how the reduced depletion voltage sites and PL defects from the epitaxial layer are superimposed on the 650 V MOSFET grids matching the device positions. Utilizing the results from the 7 substrates in the previous study, we get a clear distribution of failures in nearly 12 000 unique dies.

Experimental Results and Discussion

In **Fig. 3** a failure type distribution is shown of all dies failing any electrical test at EWS, where I_{DSS} is the drain-source leakage current, defined by testing the maximum rating V_{DS} between drain and source, I_{GSS} is the gate-source leakage current, similarly defined by applying a maximum rating V_{GS} between the gate and the source, and V_{TH} is the threshold voltage, defined by a minimum I_G needed to create a conduction path between the source and drain terminal. Each failure type is defined by a subset of test conditions, for example I_{DSS} includes several V_{DS} conditions, I_{GSS} includes several V_{GS} conditions and V_{TH} several I_G conditions. The defect types shown are the conventional ones, except the class "Epi Defect", which is a subset of defects in the epitaxial layer either too small or irregular to be accurately classified by the surface detection system, but significant enough to possibly cause parametric failure. On deep analysis, most of these are either small Triangles, Carrots or Micropits. Looking at the definable defects, see **Fig. 3 a)**, Triangles and Stacking Faults are the most prominent, with the former causing more failures in V_{TH} tests and the latter causing more failures on the I_{DSS} and I_{GSS} tests. Triangles typically originate from substrate dislocations, like threading screw and basal plane dislocations, or surface roughness of the bare substrate. The distortion is thus mainly caused in the epitaxial layer, explaining why the failure cause by this type of defect is predominantly gate related. Stacking Faults in the epitaxial layer typically originate from Stacking Faults in the substrate. As the substrate acts as a drain in the device, a pronounced I_{DSS} failure due to this defect is not unlikely.

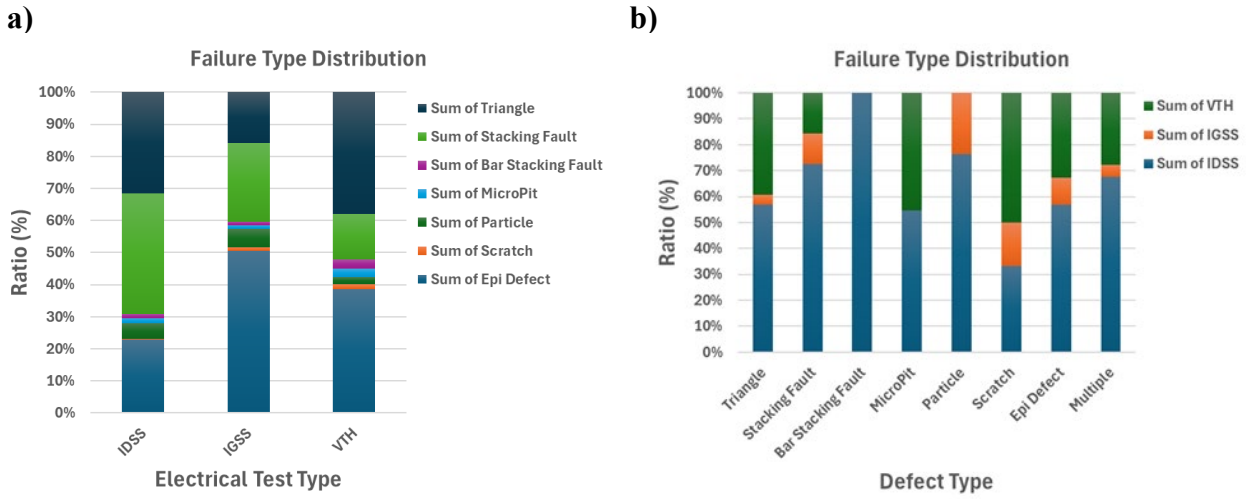

Fig. 3. Failure type distribution shown as a) distribution of defects for each failure test and b) distribution of failure types for each defect.

Particles appear to cause failures in all test types, but in **Fig. 3 b)** they only show failure in I_{GSS} and I_{DSS} tests. This is coincidently due to the die failing V_{TH} tests is not only occupied by a Particle, but also accompanied by at least one other defect. Looking at the total amount of failures, Bar Stacking Fault, Micropit and Scratches contribute very little. This does not imply they are non-significant, but rather that the sheer volume of Triangles and Stacking Faults causes more problems.

This is further highlighted in **Table 2**, showing that Bar Stacking Faults causes a higher rate of failure, ~26%, compared to Stacking Faults, ~16%. Similar for Micropit, with a low presence but high likelihood to cause failure, ~45%. Close to half of all the triangles and Micropits overlapped with depletion voltage leakage sites (QUAD), whereas less than 15% of all the failed dies with a Stacking Fault, Bar Stacking Fault, Particle, or other smaller Epi Defect and showed electrical signature during QUAD measurements. Defects causing depletion voltage reduction during QUAD appear more likely to cause problems at EWS. Looking at the overall fail rate, Triangle defects are not only the most present defectivity, as seen in **Fig. 3**, but also causes the highest fail-rate, equal to a Micropit, as well as having the largest electrical signature as seen from QUAD, see **Table 2**.

Table 2. Fail rate of dies occupied by epitaxial defects and the ratio of those that are also occupied by a reduced depletion voltage site measured by QUAD.

	Triangle	Stacking Fault	Bar Stacking Fault	Micropit	Particle	Scratch	Epi Defect
Die Fail Rate	42.69%	15.89%	25.97%	44.68%	18.11%	32.00%	35.33%
Overlapping QUAD Site	43.37%	8.21%	5.00%	42.86%	13.04%	25.00%	8.04%

By applying the KR and YI model on the entire subset of defects and reduced depletion voltage sites, see **Eq. 1-3**, we can calculate the predication rate of both PL- and QUAD-mapping, see **Table 3**. Looking at all defects found through PL-mapping, the KR rate would be as low as 10%. This is explained by the ratio of good to bad dies occupied by a Stacking Fault being too high. Examining **Eq. 1**, the numerator must be smaller than the denominator for the model to function and give sensible values. In essence, if a defect of a specific classification is more frequent on good dies than bad dies, the accuracy diminishes, and the model fails due false positives. If we remove Stacking Fault from the subset of all PL-Defects, we raise the KR of PL-Defects to ~23%. A similar trend can be seen for Particles, the occupancy of said defect on bad dies compared to good dies is very similar, so KR and YI are very low.

While the fail-rate, as seen in **Table 2**, gives a good estimate of what caused specific dies to go bad, the KR and YI, as seen in **Table 3**, gives a prediction on the entire population based on defects on both good and bad dies. Example: If defect X is present on all dies, good and bad, the fail rate would be 100%. This is because defect X is on all bad dies, but it is also present on all good dies, so while fail rate is 100%, the KR and YI would be very low due to false positives. Particles have a low KR at 1.8%, even though looking at all the bad dies in the study, 18% of them are occupied by a Particle. A wafer with plenty of particles post-epitaxy is thus unlikely to have a significant effect on YI. Both Triangles and Micropits show high KR, but Triangles, being more frequent, cause a higher YI. If a wafer was occupied by an equal number of Triangles and Micropits, the defects would have a similar effect on YI, but Triangles are 16x more frequent in the epitaxial layer than Micropits in this study and consequently the YI is of the Triangle defect is larger.

QUAD gives a significantly better accuracy on KR, ~37%, and is a better YI predictor, ~5%. Even if we refine the KR for all PL-Defects by removing false positives related to Stacking Faults, giving a KR of ~23%. **Fig. 4** shows an overlay of a) EWS-QUAD and b) EWS-PL Defects that visually support the above calculation. The improved accuracy of QUAD is likely because it maps depletion voltage that is sensitive to the electrical behavior of defects in the epitaxial layer, as opposed to PL-mapping.

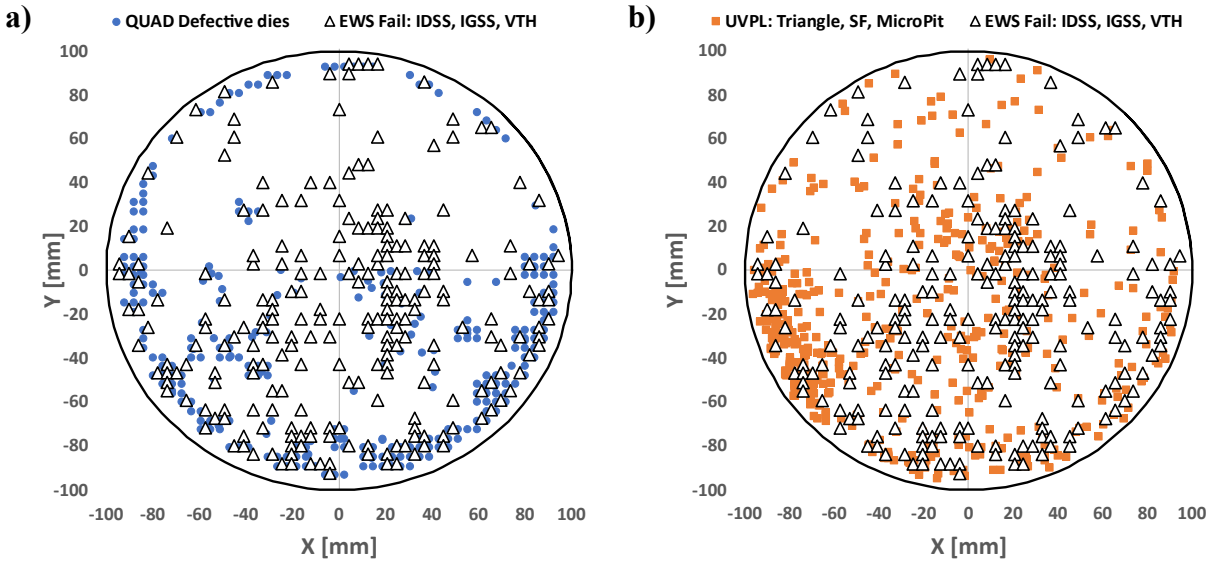

Fig. 4. Overlay EWS (I_{GSS}, I_{DSS}, V_{TH}) failed die with a) QUAD detected defects using bin-die map and b) PL (Triangles, Stacking Faults, MicroPits) defects.

PL can be associated with electrical properties, as the excitation and recombination in effect is locally more likely to happen due to changes of the energy states, a more observable phenomena in mono-crystalline material since the event is isolated to crystal abnormalities (defects) but less relatable with parametric failures than localized reduced depletion voltage, which is observed at defective sites by QUAD.

Table 3. Kill-ratio and yield-impact of all QUAD sites, as well as PL-Defects and the respective classification, of the entire test-batch of ~12 000 MOSFET devices. The number of Stacking Faults causing device failure with respect to the total number of actual Stacking Faults is too small, making the Kill-ratio model unapplicable.

	Kill-Ratio (%)	Yield Impact (%)	Nominal Yield Impact (%)
QUAD	36.81	5.20	6.01
All PL-Defects	10.61	2.71	5.64
Triangle	33.13	2.33	2.94
Stacking Fault	NA	NA	2.17
Bar Stacking Fault	12.92	0.07	0.14
Micro Pit	35.51	0.14	0.18
Particle	1.86	0.04	0.35
Scratch	25.23	0.06	0.09
Epi Defect	16.33	0.71	1.25
All PL-Defects (no Stacking Fault)	22.51	3.00	4.27

In **Fig. 5** the accuracy of PL- and QUAD-mapping is illustrated by calculating the ratio of bad dies each respective method successfully captures. For I_{DSS} and I_{GSS} related failures both methods can identify a similar quantity of bad dies while for V_{TH} related failures QUAD-mapping seems more accurate, finding nearly 10% more dies. The combined capture rate is calculated by looking only at uniquely found bad dies for each respective method. Here it is clear that both methods complement each other very well as the combined capture rate is significantly higher than for each method on its own. Worth noting is that both PL- and QUAD-mapping relies heavily on measurement conditions and recipe tuning.

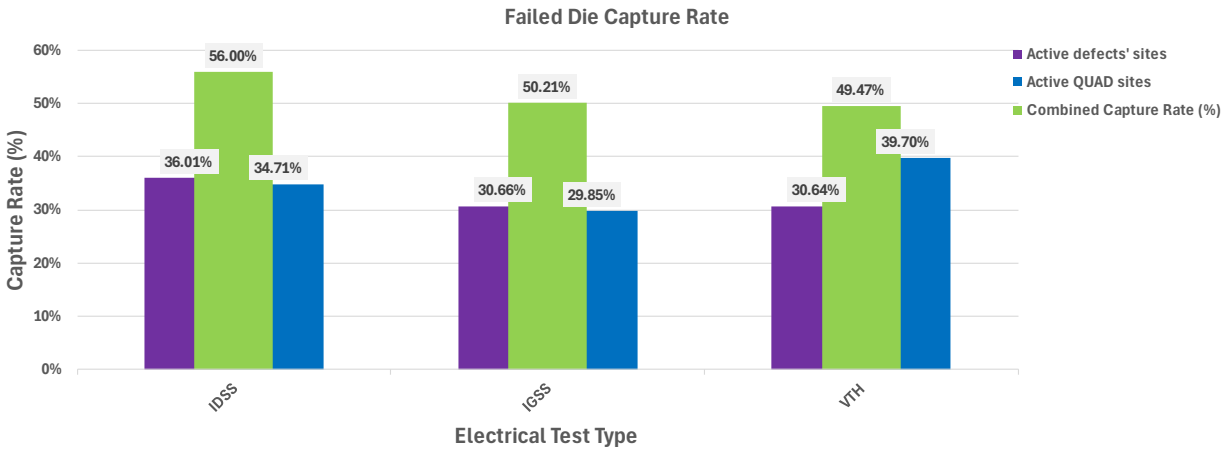

Fig. 5. Rate of overlap with EWS tests for PL-mapping, purple bar, and CnCV QUAD-mapping, blue bar, and the combined capture rate of both methods, green bar, with bad dies measured by EWS. Combined capture rate is calculated from dies uniquely captured by either method.

The capture rate of either method can be improved marginally by further tuning of the tools and recipes used. In this study we replicated PL-imaging conditions used in a device production line, while QUAD tuning is still in implementation phase. The remainder of the EWS failures associated with neither PL-Defects or QUAD sites are attributed to device fabrication faults occurring between initial epitaxial growth and EWS testing. In essence, this means that roughly one half of the failures are due to defectivity in the epitaxial layer while major parts of the other half is related to the device fabrication process itself. Further work to also include a possible effect of dislocation could strengthen the conclusion of PL and QUAD-imaging as complementary techniques to verify the quality level of substrate and epitaxy.

Summary

Comparison between PL- and QUAD-mapping of wafers post-epitaxy, used before manufacture of roughly 12 000, 650 V SiC MOSFETs devices from 7 wafers of 200 mm 4H-SiC, shows that QUAD-mapping is a valid alternative, and complement, to PL-mapping. The model used to calculate KR and YI shows a higher probability for QUAD to find dies that cause I_{DSS}, I_{GSS} and V_{TH}, the more common failures at EWS. As supported by the KR calculations, the accuracy of QUAD-mapping is also better than the PL-mapping. QUAD is also able to improve on the prediction of yield-impact. The capture rate of these combined methods shows that each respective technique uniquely predicts failures of dies that the other one missed. This information can be used to not only to improve the capture rate for both methods, but most important to progress the overall accuracy of KR and YI of defects and depletion voltage leakage sites.

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