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Challenges in Investigating UIS Material-Based Failures & Yield Prediction in the Absence of Robust 4H-SiC Epiwafer Quality Standards

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Abstract. Due to the lack of internationally accredited quality standards for silicon carbide (SiC) epiwafers, vendors provide defect maps using different metrology techniques and naming conventions, making it difficult to draw correlations between defect types and unclamped inductive switching (UIS) behavior. This study tested 1700 V rated Junction Barrier Schottky Diodes (JBS) using materials from five 4H-SiC epiwafer suppliers and concluded that, without maps having industry-standardized defect names and showing precise locations, sizes, and shapes, device manufacturers cannot effectively predict UIS yield and reliability.

Introduction

The correlation between epitaxial (epi) material defects and 4H-SiC diode UIS failures has not yet been clearly demonstrated. Historically, studies have focused on understanding general defect failure mechanisms of SiC MOSFETs [1,2,3], SiC device failure correlations [4,5], and studies of SiC diode design ruggedness [6,7,8,9,10,11,12,13]. This study was unable to establish a direct epi defect UIS failure correlation because epiwafer vendors do not provide sufficiently detailed defect maps for analysis, and results herein strongly point toward epi material as a contributor to UIS JBS diode failures. For SiC to become pervasive in power electronics, epiwafer quality standards that are comprehensive and internationally recognized are essential. After all, epiwafers are literally the foundation upon which devices are built as well as constituting a large portion of device cost. To deliver the reliability, price, and quantities that end users require to transition from silicon to SiC, device manufacturers must be able to apply statistical methods to establish correlations between epiwafer quality, specific defect types, and performance (including long-term reliability) of finished devices.

Today's manufacturers of SiC power devices rely on crystal defect maps for such predictions; these defect maps are provided by epiwafer vendors. Unfortunately, the SiC community does not yet have quality standards to which epiwafer vendors must comply. Device manufacturers must reconcile different defect terminology reported by various mapping tools, often leaving defective device performance (or failure) a mystery. Some epiwafer defects go entirely unrecognized due to insufficient detectivity of production-scale metrology techniques. Capabilities exist to address these issues, but standards are needed. Using the unclamped inductive switching (UIS) test, this paper illustrates an example where existing capabilities should be used to elucidate defect-performance relationships so that standards may be established.

Experimental

The UIS test is standard industry practice for production verification of the avalanche energy rating of power devices [14]. The relevance of UIS testing is three-fold: First, designers rely on this metric to select devices that can survive avalanche breakdown given the operating conditions of their systems. Second, due to the high energy levels the device may see during avalanche, epiwafer defects that may be benign under normal conditions could precipitate critical failures during UIS testing.

Third, UIS testing to failure has proven valuable for appraising epiwafer quality due to its timeliness and low use of resources, as compared to extended lifetime stresses which can take months to complete.

In this work, five different turn-key epiwafer vendors (A, B, C, D, E) were used to fabricate 1700 V JBS diodes using Microchip's production fabrication process for Microchip part number MSC050SDA170B. Figure 1 shows portions of epiwafer defect maps provided by each of the five vendors; the reader can see how each supplier uses a different classification system. To objectively evaluate the epiwafer quality of each vendor, control wafers from Vendor A were processed with each run. Wafers were probed and sawn, and passing devices were assembled into TO-247 packages for characterization.

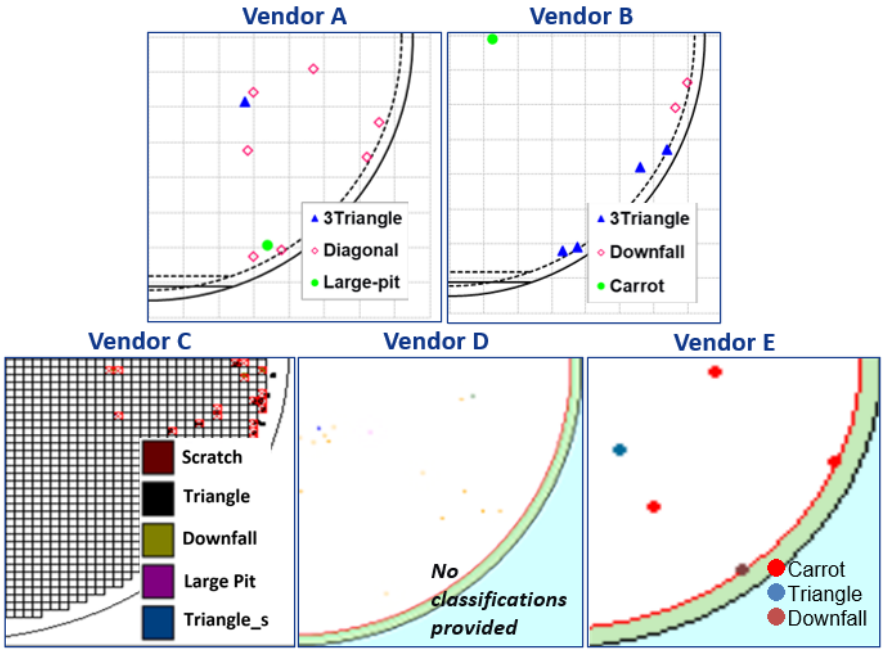

Fig. 1. Excerpts of epiwafer epi defect maps provided by five different vendors. Vendors A, B & E designate defects, but don't report the same defects. Vendors C & D are not clearly defined.

The UIS test circuit is shown in Figure 2. Measurements were taken using the ITC 55100C system with the ITC 55HVD1 high voltage diode adapter box [15] represented by the dotted square, which uses a MOSFET with higher breakdown voltage than the device under test (DUT) to channel the UIS energy into the DUT. The test voltage V_{DD} is set to 150 V to speed up the inductor charging time and reduce DUT heating.

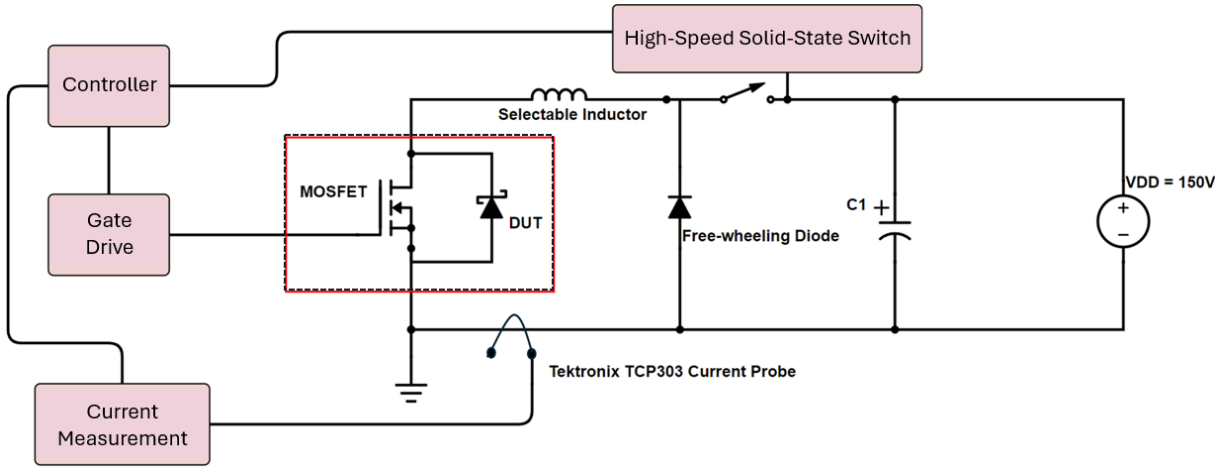

Fig. 2. Circuit diagram of single-pulse UIS test bed.

Figure 3 shows typical UIS waveforms from the study. To begin, the MOSFET is in the ON state to charge the inductor to an energy level, E_{AS}, then the MOSFET is abruptly switched to the OFF state. Because the MOSFET in the ITC diode adapter box has a much higher blocking voltage rating than the JBS diode DUT, the DUT is forced into avalanche breakdown; this leads to a rise in junction temperature until the DUT undergoes catastrophic and permanent failure, as seen by the collapse of the DUT's cathode-anode voltage. The ITC tester contains an array of inductors ("selectable inductor" in Fig. 2) that allows a ramp of E_{AS} in even steps. To gather a multitude of failure data points, E_{AS} was incremented by 500 mJ until the part passes at 3 J; beyond this value, increments are reduced to 100 mJ to the 3-4 J range, where failure is expected. The waveforms in Figure 3 show a device failing at 4 J, the critical value at which the device can no longer dissipate the E_{AS} delivered from the inductor; a failed DUT measures an electric short from anode to cathode.

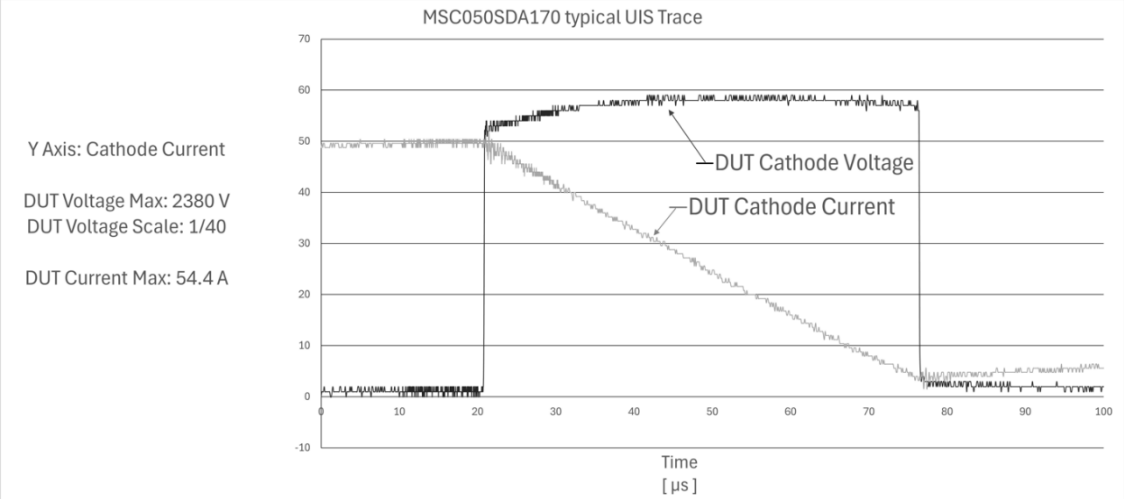

Fig. 3. Typical UIS waveforms of this study, showing expected failure in the range of 4 J.

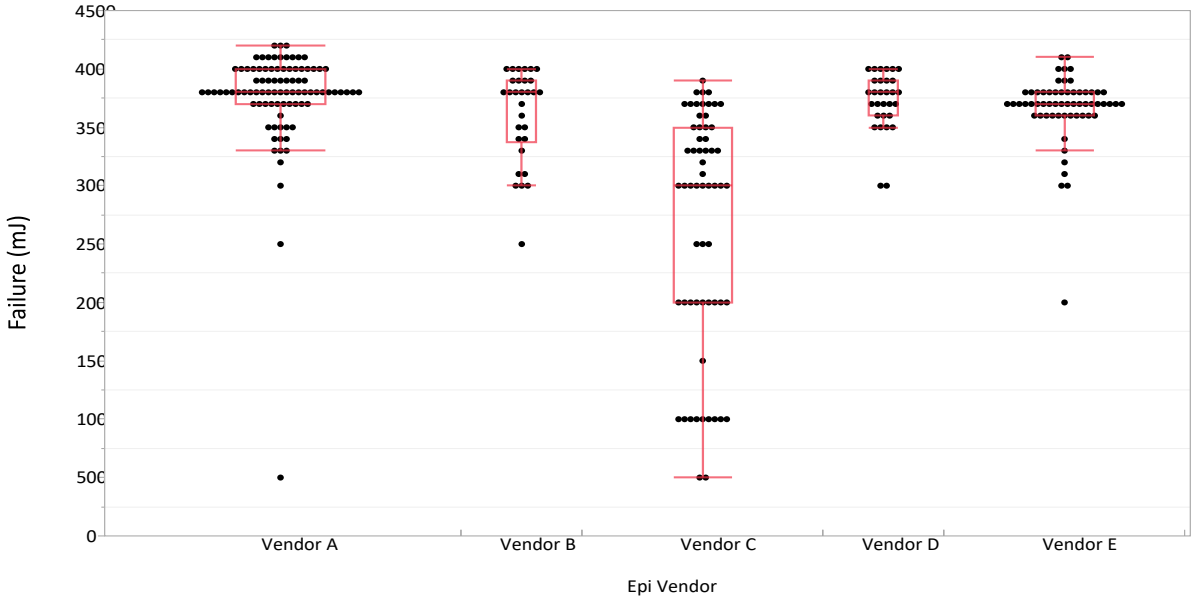

Fig. 4. UIS failure distribution of tested devices across five epiwafer vendors. Black dots represent a single failure; box plot shows E_{AS} quartile distributions for each vendor. Numerical values are given in Table 1. Excerpts of defect maps provided by each vendor are shown in Fig. 1.

Table 1. Numerical values of failure energy, E_{AS}, in Joules, corresponding to the box plot of Fig. 4.

Vendor	Min	10%	25%	Med	75%	90%	Max
A	0.5	3.4	3.7	3.8	4.0	4.1	4.2
B	2.5	3.0	3.4	3.8	3.9	4.0	4.0
C	0.5	1.0	2.0	3.0	3.5	3.7	3.9
D	3.0	3.5	3.6	3.8	3.9	4.0	4.0
E	2.0	3.3	3.6	3.7	3.8	3.9	4.1

Discussion

Observing Figure 4 and the numerical data of Table 1 leads one to speculate there is a material quality issue that brings the average failure energy for Vendor C well below that for the other four vendors—especially if the one outlier data point for Vendor A is ignored. In any case, speculation is the best one can do when using non-standardized defect maps provided by vendors. For high volume manufacturing, additional characterization is required to identify the defect type and precise position on the wafer. Historically, ultraviolet photoluminescence (UVPL) analysis has proven to offer high resolution and detectability and has clearly documented significant progress in improving 4H-SiC materials [16] but is not easily deployed into a high volume manufacturing environment.

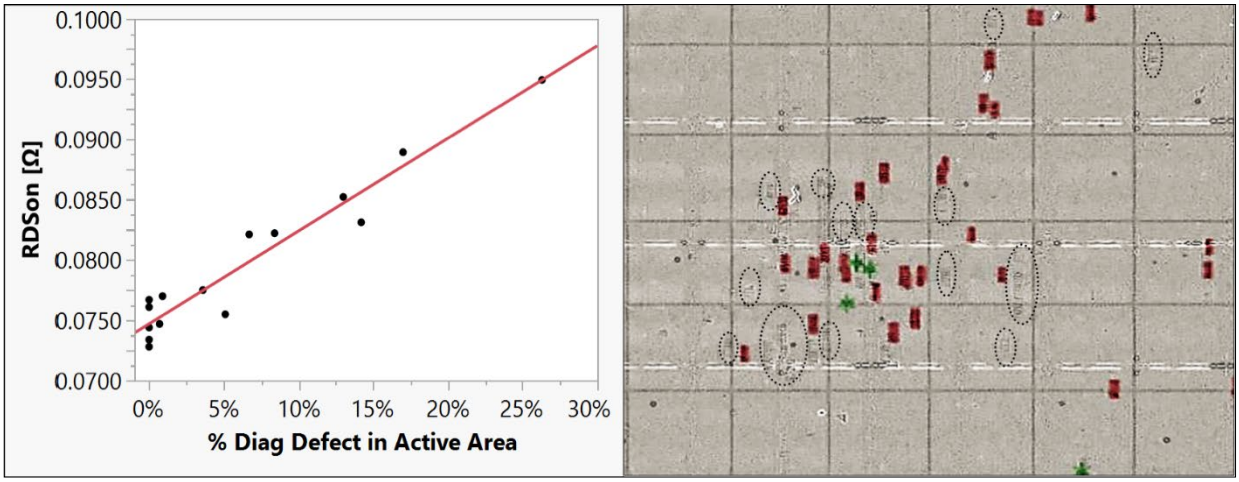

Fig. 5. *Left* – On-state resistance vs percent of MOSFET active area with trapezoidal defects. *Right* – Defect data points, as reported by epiwafer supplier, overlaid onto a high-detectability UVPL image to highlight defects not reported by the vendor. *Legend* – Rectangle = trapezoidal, Star = large pit, Dashed circles = defects not reported in the provided map.

Systematic studies where crystal defects are structurally identified followed by a rigorous analysis of short- and long-term electrical performance is necessary to establish quality standards and defect classifications to which all epiwafer vendors and device manufacturers can subscribe. Previous work by device manufacturers to correlate epiwafer defects with device outcomes have warranted changes in SiC defect classifications. One such example is the impact of the "trapezoidal" defect, also called a "bar stacking fault" or "diagonal." Trapezoidal defects were long considered to have little or no impact on SiC MOSFETs and were classified as "non-killer." Figure 5 tells a different story, however, as there is a linear relationship between the percent of MOSFET active area spanned by trapezoidal defects and the MOSFET's on-state resistance [17], a finding also reported in [18]. By overlaying industry-generated epi defect maps onto high-detectability UVPL images (Fig. 5, right), Microchip identified a correlation between trapezoidal densities and increased on-state resistance. These results demonstrate that epiwafer defect maps can be used to effectively screen devices that pose a performance risk despite passing wafer-level electrical testing.

Epiwafer quality issues are further compounded when comparing total useable area (TUA) across epiwafer vendors, as there is no common baseline used in determining TUA with data provided in defect maps (see Fig. 1). The only existing standard related to TUA determination is found in SEMI M92-0423 [19], which states that TUA is "determined by a method agreed upon between the supplier and the customer." This may be perceived as a negotiation between two parties rather than an industry standard intended to establish a minimum bar for SiC product quality. Looking at the data, Vendor A recognizes "3Triangle" and "Large-pit" defects as killer defects, and TUA is calculated by excluding any area containing them. For the remaining four epiwafer vendors, it is unknown which defect types are excluded from TUA; indeed, the same crystal defect may be called a different name. Finally, the precise position, shape, and size of defects in vendor-provided defect maps are inadequate for predicting wafer-level yield.

Summary

While capabilities exist to identify SiC epiwafer crystal defects and correlate them to device performance and reliability, industry-wide material quality standards are needed to further the successful commercialization of SiC power devices. As an example, this work analyzes UIS performance of 1700 V SiC JBS diodes made on epiwafers from five different vendors. Non-standardized defect maps offer incomplete information on the type of defect, precise location, size, or shape. This leaves device manufacturers with unknown root cause and no direction toward a solution. The establishment of material standards will allow device manufacturers to have greater control over performance and reliability; to ensure a level, competitive playing field among material suppliers; and to drive continuous improvement in epiwafer quality and cost, ultimately benefiting end users and the SiC market.

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