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Non-Contact Full Wafer Imaging of Electrically Active Defects in 4H-SiC Epi with Comparison to End of Line Electrical Device Data

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Abstract. In this work we present the results of a comparison between the non-contact corona-based QUAD (Quality, Uniformity and Defects) technique for inline mapping of electrically active defects in SiC epi and final wafer level electrical device data on merged PiN Schottky diodes. A new defect analysis method for the QUAD mapping is introduced that involves the creation of a die yield bin map using the in-die values of depletion voltage that facilitates the comparison to the wafer level final electrical device data. Excellent correlation of the QUAD wafer bin map results to the final wafer level electrical device data was observed, illustrating that QUAD mapping of defects in SiC epi can provide a powerful and convenient inline complement to UVPL measurements for determining which defects are electrically active and will impact device performance.

Introduction

There is a strong need in the rapidly growing SiC epi industry for detection of defects and corresponding device yield diagnostics. Optical and UVPL mapping are currently used for inline defect detection however it can be difficult to determine with these techniques which defects will be electrically active and actually detrimental to devices. To address this need Semilab SDI introduced the Quality, Uniformity, and Defect mapping (QUAD) mode in their CnCV (Corona noncontact Capacitance-Voltage) line of tools. In the QUAD technique, the surface voltage is mapped after corona charging the whole wafer surface into deep depletion. Electrically active defects are detected as spots or clustered regions compared with the area surrounding the defect. QUAD demonstrated the electrical activity of defects such as triangular, downfall and carrot type defects and the QUAD detected defects were then compared with UVPL measurements [1]. A considerable fraction of the UVPL defects were found to be not electrically active and thus the QUAD detected electrically active defects provide a powerful compliment to UVPL and optical mapping measurements [2].

To facilitate comparison to final electrical device data, a new QUAD defect analysis is introduced in this work. It converts the map into a die grid of user selected size and creates a die bin map using the in-die values of depletion voltage. In such a parametric analysis, the die will be considered failed if the depletion voltage falls below or the reverse bias leakage current is above a certain defined threshold value. This provides an analogy to die failures in final electrical tests on Schottky diodes when the breakdown (BD) voltage falls below or if the reverse bias leakage (I_R) is above a defined threshold. In this way the QUAD wafer bin map results can be directly compared to final electrical device test results. The goal of the approach is to use QUAD as an early, after epi growth indication of electrical parameter-based die yield.

Experimental

The QUAD technique is a full wafer defect mapping mode in the CnCV metrology which is an adaptation of the corona-Kelvin noncontact electrical metrology extensively used in Si IC fabrication [3]. A description of the principles, apparatus and applications for wide bandgap semiconductors, including SiC, is given in a 2017 CnCV review paper [4]. The initial inline QUAD measurements were performed on n-type epitaxial 4H-SiC on n^+ substrates from two different vendors. Macro and micro scale QUAD measurements were also made on those same samples after wafer level final 1.5mm x 1.5mm 650V Merged PiN Schottky diodes were fabricated.

The CnCV apparatus used in this work included whole wafer wire type corona charging for QUAD mapping. The negative corona charging used involves the deposition of negative (CO_3^-) ions to bias the n-type SiC epi samples into depletion [3].

The Kelvin probe used in the QUAD mapping measures the contact potential difference, V_{CPD}, between the wafer and the vibrating reference electrode [4]. A probe pre-calibration is used to subtract the contribution due to the electrode work function. After such a correction, the V_{CPD} is referred to as the surface voltage, V, and in the case of measurement on bare SiC epi this measured surface voltage is equivalent to the depletion voltage. For macro scale QUAD mapping a 2mm diameter Kelvin probe was used. Whole wafer mapping was performed in about 8min for a 150mm SiC wafer.

For the micro scale QUAD (mQUAD) maps used to examine depletion voltage values within individual device dies, a 8mm diameter Kelvin Force Microscopy (KFM) probe was used. Further details regarding mQUAD measurements using KFM are described in references [5,6].

Electrical wafer level test data of breakdown voltage and reverse bias leakage were measured on 1.5mm x 1.5mm 650V Merged PiN Schottky diodes fabricated on the same SiC epi wafers initially measured with full wafer QUAD mapping. Ultraviolet photoluminescence (UVPL) results presented in this work were measured with a Lasertec SICA 88 tool.

Results and Discussion

As an illustration of this new QUAD die bin map analysis, we present two examples of 4H-SiC epi grown in the same reactor run on 150mm substrates from two different vendors giving different device yield. QUAD map results after epi growth are compared to electrical wafer level test data of breakdown voltage and leakage on 1.5mm x 1.5mm 650V Merged PiN Schottky diodes. In Fig 1a and 1b, the initial QUAD defect maps on the as grown SiC epi give a quick overall indication of defective regions on the Vendor A and B SiC epi samples. A smaller number of defective regions (low depletion voltage in red) are seen for the Vendor A sample while the Vendor B sample shows a large defective area covering most of the center of the sample. In both cases, there are some discrete defect locations that are detected by the original QUAD analysis based on contrast, however there are also larger clustered defect regions (red) near the wafer edge with defects not adequately resolved. The new QUAD die bin maps with a 1.5 x 1.5mm die size of the same surface voltage maps are given in Fig. 2a and 2b together with final electrical device results. The new analysis not only identifies the localized defects as electrically active defective dies but the clustered regions near the wafer edge for both samples are also identified as defective dies. In Fig. 2a and 2b, overlay die bin maps are shown of both QUAD failed defective dies (blue squares) identified by a depletion voltage threshold and wafer level test failed defective dies (open triangles) identified by falling below a BD voltage threshold or if reverse bias leakage is above a defined threshold. In each case there are regions of strong spatial correlation between the QUAD failed dies and the electrical device failed dies. This indicates the usefulness of the QUAD die bin map analysis in prognostics of device failures early in the process flow. One may also point out the presence of a certain number of device failed dies not observed in QUAD. Such dies may be indicative of process induced (or enhanced) defects not present in the as grown epi. UVPL defect maps were also measured on these samples in the present study in order to address correlation to the QUAD and electrical device failed die bin maps.

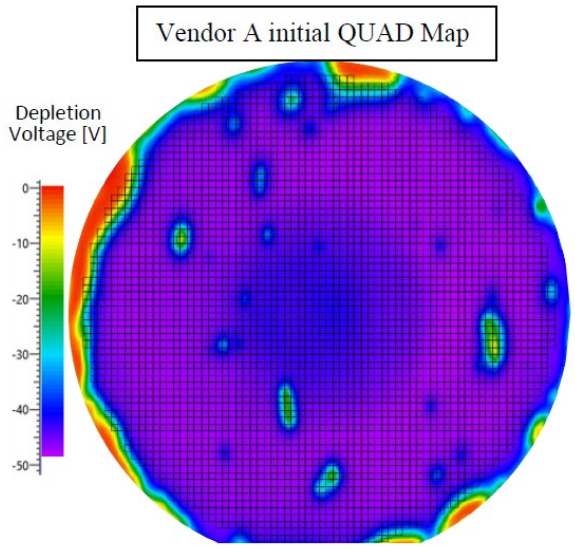

Fig. 1a. Vendor A initial QUAD map on the bare SiC epi showing localized defective regions with low depletion voltage along with larger clustered defective regions of low depletion voltage near the wafer edge.

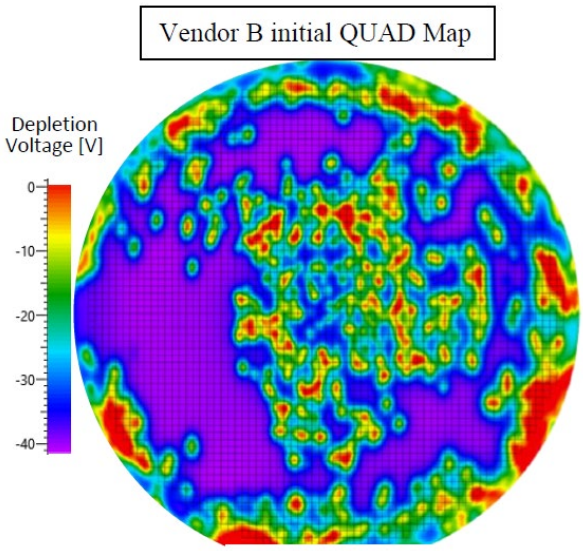

Fig. 1b. Vendor B initial QUAD map on the bare SiC epi showing a high density of defective regions with low depletion voltage in the center and edge regions of the wafer.

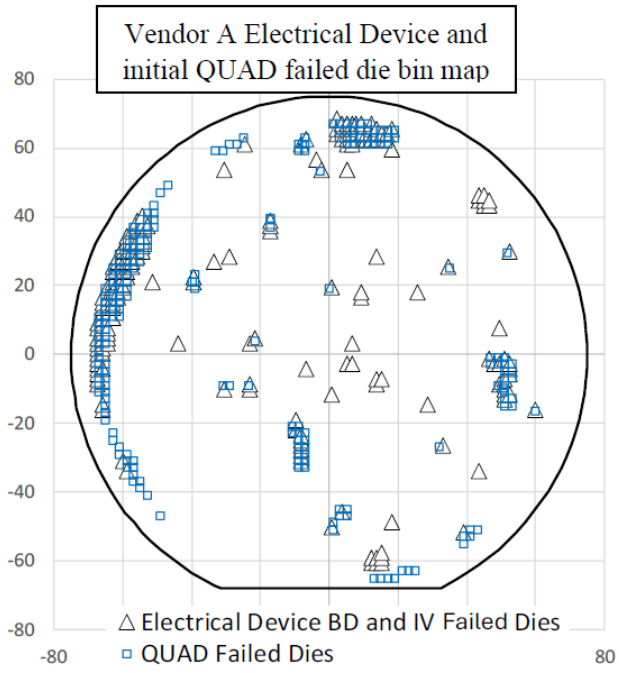

Fig. 2a. An overlay of the Vendor A initial QUAD failed die and the wafer level test device failed die bin maps based on a die size of 1.5mm x 1.5mm.

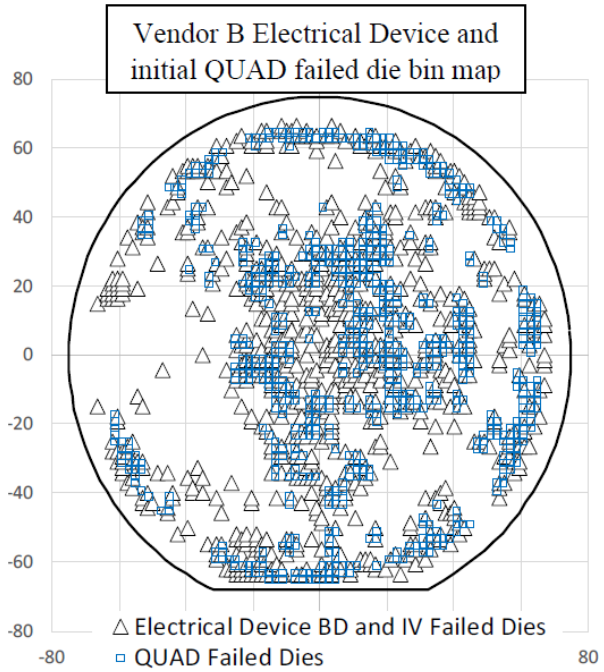

Fig. 2b. An overlay of the Vendor B initial QUAD failed die and the wafer level test device failed die bin maps based on a die size of 1.5mm x 1.5mm.

The initial Vendor A QUAD map in Fig. 2a gives a QUAD die yield of 96.8% while the final electrical device die bin map based on breakdown voltage and reverse bias leakage thresholds gives a die yield of 95.5%. The Vendor B QUAD map in Fig. 2b gives a QUAD die yield of 88.1% and the final electrical device die bin map based on breakdown voltage and leakage thresholds gives an electrical device die yield of 87.1%. Additional failed dies in the final electrical device results lowering the die yield can be attributed to process induced defects during the fabrication of the merged PiN Schottky diodes.

After the wafer level fabrication of the merged PiN Schottky diode devices, QUAD mapping was performed again on the samples. This is possible because the individual diodes are electrically isolated and the deposited corona charge will distribute across the metalized surface of each individual diode. This allows for a very interesting analysis of the evolution of process induced defects during the diode fabrication process. The Vendor A QUAD map after the device fabrication is shown in Fig. 3a. The QUAD map is converted to a failed die bin map and once again compared to the electrical test failed die bin map in Fig. 3b. Additional failed dies in the QUAD bin map now appear (shown as red squares) and correlate well with failed electrical test dies that were not detected in the initial QUAD map on the as grown SiC epi. These additional failed dies are most likely due to process induced defects enhanced or created during the device fabrication process.

For the Vendor A sample, macro QUAD mapping identified 194 out of 205 defective dies, giving a capture rate of 94.1%. Future work will employ UVPL and optical imaging to analyze the nature of the defects contributing to die failures and to investigate the small fraction of failed dies undetected by QUAD. Potential factors include the need for further optimization of QUAD depletion voltage threshold criteria and depletion region probing depth. Refinements of these factors will be explored in a subsequent study.

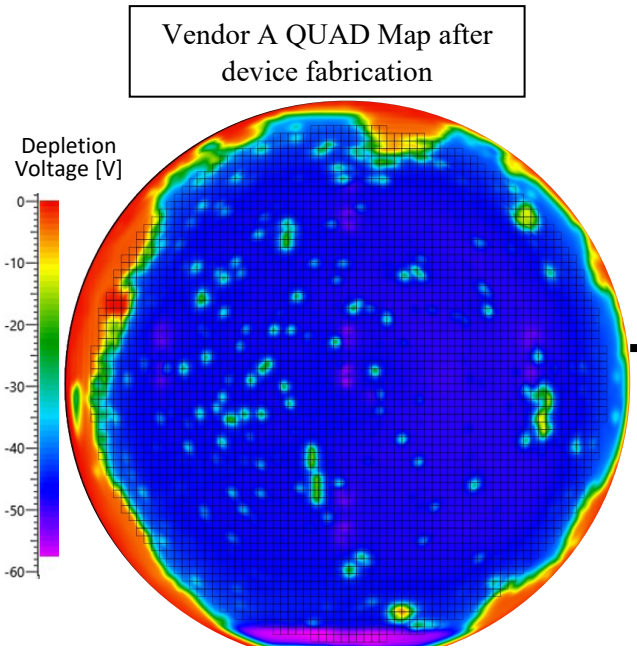

Fig. 3a. Vendor A QUAD map after wafer level device fabrication showing a device grid overlay to define the individual dies. Additional process induced failed dies are visible compared to the initial QUAD map on the bare SiC epi.

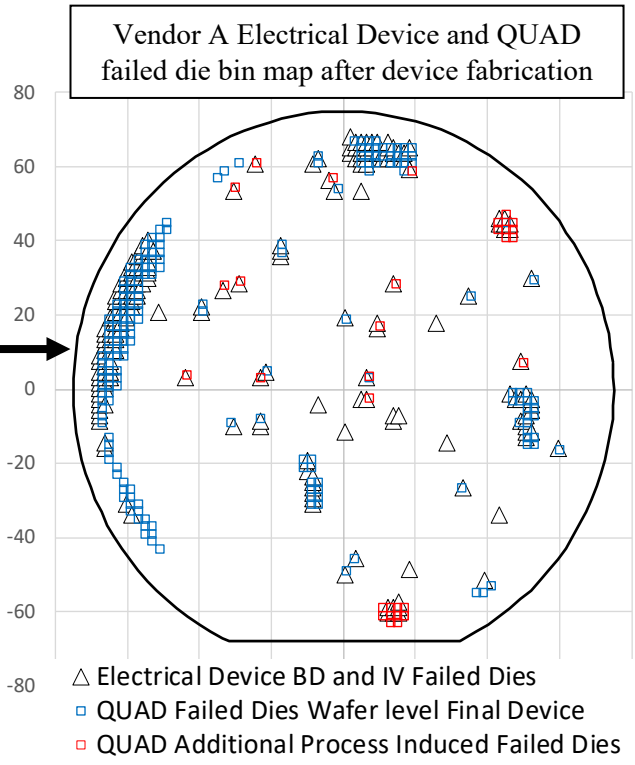

Fig. 3b. An overlay of the test device failed die bin map and the Vendor A QUAD failed die bin map after wafer level device fabrication showing additional QUAD failed dies due to process induced defects as red squares.

The isolated diodes on the final device wafer also allow for another very compelling investigation of the in-die depletion voltage retained on individual diodes using micro-scale QUAD (mQUAD) mapping with a Kelvin Force Microscopy (KFM) probe. With the mQUAD mapping the depletion voltage retained on each individual diode can be resolved. This allows for a unique and powerful analysis of the QUAD failed dies directly compared to the electrical test failed dies on a die by die basis. Such an example of this analysis is shown in Fig. 4 for the Vendor B sample. A full wafer macro QUAD failed die bin map after wafer level device fabrication along with the final electrical test failed die bin map is shown on the left hand side of Fig 4. As an example of mQUAD mapping,

a 35x30mm region in the center of the wafer was mapped with a KFM probe after corona charging, shown in the upper right corner of Fig. 4. Each individual QUAD failed die, based on a retained depletion voltage threshold of -20V, can then be compared to the electrical test failed dies, shown in the bottom right corner of Fig. 4. In this region 145 of the 154 electrical test failed dies were detected by the mQUAD mapping giving a 94% capture rate in this region. Considering the promising nature of these results, future studies will aim to collect more comprehensive statistics of the mQUAD measurements across a larger number of wafers. mQUAD mapping on the wafer level merged PiN diode samples also opens the door to investigation of the electrical nature of both failed and good individual diodes by analyzing high resolution voltage distributions across the diodes in addition to depletion voltage decay transients that can help elucidate the relative electrical activity of particular defects such as triangular, stacking faults, etc. that result in a failed die.

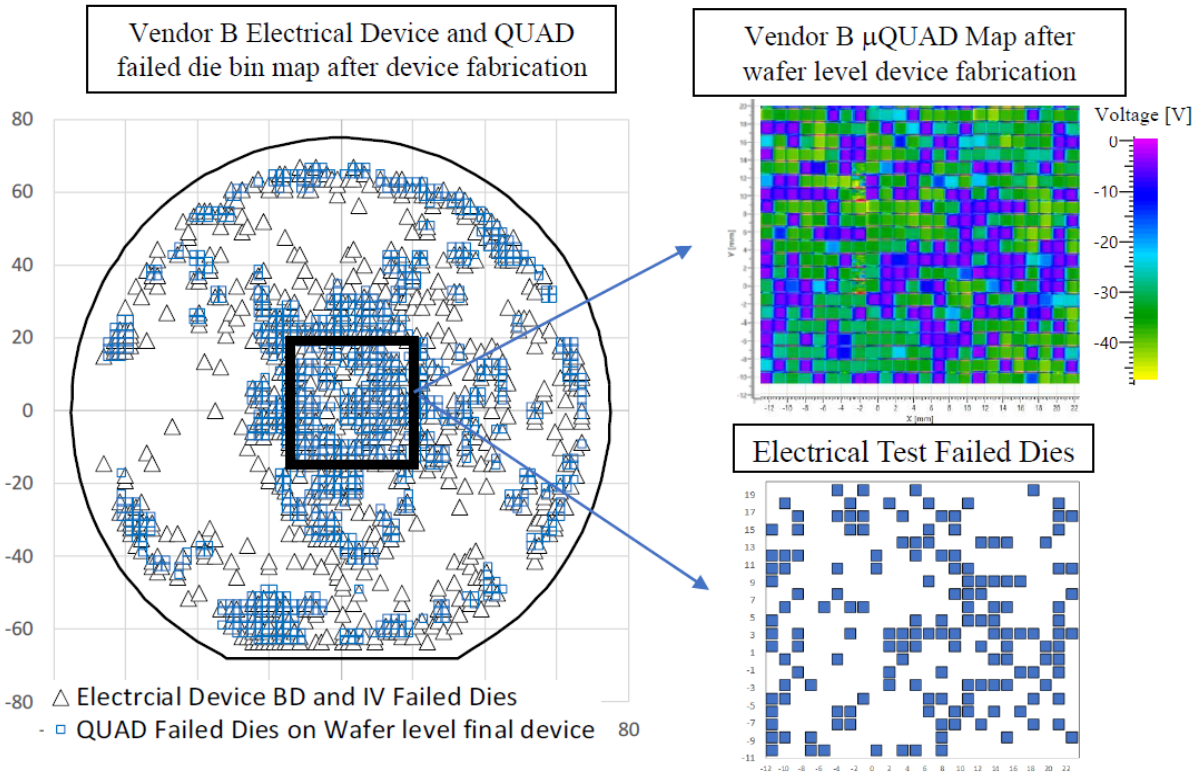

Fig. 4. An overlay of the test device failed die bin map and the Vendor B QUAD failed die bin map after wafer level device fabrication. A 35x30mm region in the center was measured with mQUAD which clearly shows well defined low depletion voltage in the failed dies due to the electrically isolated merged PiN Schottky diode devices. The mQUAD map shows excellent correlation to the electrical test failed dies based on BD voltage and I_R criteria.

The QUAD failed die bin results can also be compared to UVPL results. An example of this is shown in Fig.5 for the Vendor A sample. There is a strong correlation of clustered stacking fault defects near the wafer edge to both QUAD failed dies and electrical test failed dies. However there are a large percentage of stacking fault defects in the remainder of the sample that do not cause electrical die failures. Diode devices are much less sensitive to stacking faults compared to MOSFET devices and typically a higher density of stacking faults within a die is necessary to cause diode failures [7]. QUAD mapping can be a strong complement to UVPL to help differentiate which of these defects will result in electrical device failure. Another advantage of the QUAD mapping is that it can effectively measure depletion voltage all the way to the wafer edge as demonstrated in Fig 5.

Using UVPL, QUAD failed die and electrical test failed die results the kill-ratio (KR) and yield impact for various defect types can be calculated using a method proposed by M. Ono et al. [8] and D. Baierhofer et al. [9]. This yield impact and kill ratio analysis, which can give an indication of how detrimental certain defect types are to the efficacy of a particular type of device, will be performed in future work on this project.

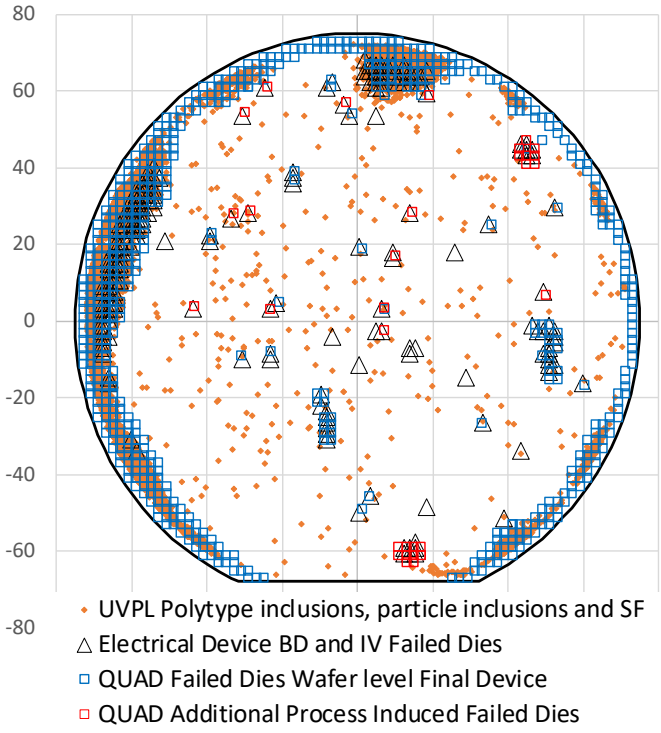

Fig. 5. An overlay of the test device failed die bin map, Vendor A QUAD failed die bin map after wafer level device fabrication and a UVPL map of polytype inclusions (triangles, downfall, carrot defects), particle inclusions and stacking faults (SF).

Conclusion

This work presents a comparison between the non-contact corona-based QUAD technique for inline mapping of electrically active defects in SiC epi and final wafer level electrical device data on merged PiN Schottky diodes. Excellent correlation between QUAD wafer bin maps and final device data was observed, demonstrating effectiveness of QUAD as an inline complement to UVPL measurements for identifying electrically active defects. mQUAD mapping with a KFM probe provides a detailed analysis of individual diodes, allowing direct comparison of QUAD and electrical test failures on a die-by-die basis.

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