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Ultra-Thick (~200µm) Epitaxy on 150mm 4H-SiC Wafers Using Single Wafer CVD Reactor

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Abstract. Thick epitaxy with different buffer and drift layer growth rates are studied. Epilayer with higher growth rates demonstrates lower basal plane dislocaiton (BPD) but higher stacking faults. We use the optimum growth rate found from the aforesaid experiments to achieve 100um and 200um epilayers. BPD pileup was observed, especifally at the edges of the epilayer rendering an exclusion area upto 15mm from the edge. Hence, we argue that it is essential to consider higher exclusion region for thicker epilayers. Large, pits and bumps are observed for thicker epitaxy, upto a diameter of 48µm for 200µm epilayers. Finally, we polish the epilayers and demonstrated 98% and 95% total usable area (TUA) for 100µm and 200µm epitalayers respectively.

Introduction

Silicon carbide is an important material for high voltage applications due to its various exceptional electrical and mechanical properties [1]. Currently SiC crystal is widely used in electric vehicle (EV) related electronic applications. Typically, operational voltages of these power devices are in the range of 0.6-1.5kV, where typically 6µm-15µm epitaxial layers are used. However, to block high voltage (>5kV), much thicker epitaxy (>50µm) is required. Thick SiC epitaxy is extremely challenging due to severe surface degradation by formation of larger morphological and extended defects, as well as various complex dislocations (half loop array or HLA, BPD pileup, etc.). Thick epitaxy in the range of 50-100µm is demonstrated in earlier literature [2]. In this research, we study epitaxy in the range of 60-200µm on 150 mm 4H-SiC wafers for surface, defectivity, wafer shape, etc.

Experimental

A commercial, single wafer epi reactor is used to grow epilayers with various thicknesses. We compare the results with various growth rates. We increase growth rates for buffer and drift layers (3 times (3x) and 2 times (2x) respectively) by increasing precursor gases. We adjust growth time to achieve the target thicknesses (60µm, 100µm and 200µm), whereas adjust nitrogen flow rate to achieve a doping target of ~1e15 cm^{-3}. We select wafers from adjacent slices in a boule to minimize the wafer-to-wafer variations. Wafer shapes are measured using Tropel Ultrasort and defects are characterized by a SiCA88 tool. Chemo-mechanical polishing (CMP) was performed on these epilayers with a removal of ~1µm to improve roughness of the surface, associated with the thick epitaxy.

Results

Higher growth rate is needed for thicker epitaxies to minimize the growth time. To study the effect of higher growth rates on defects, first, we increase growth rate by increasing precursor gas flow rates.

We find that higher growth rates reduce basal plane dislocations (BPD) in the epilayer, however increases stacking faults (SF) (Fig. 1). We further optimize the process for the higher growth rates to reduce SF by optimizing process conditions.

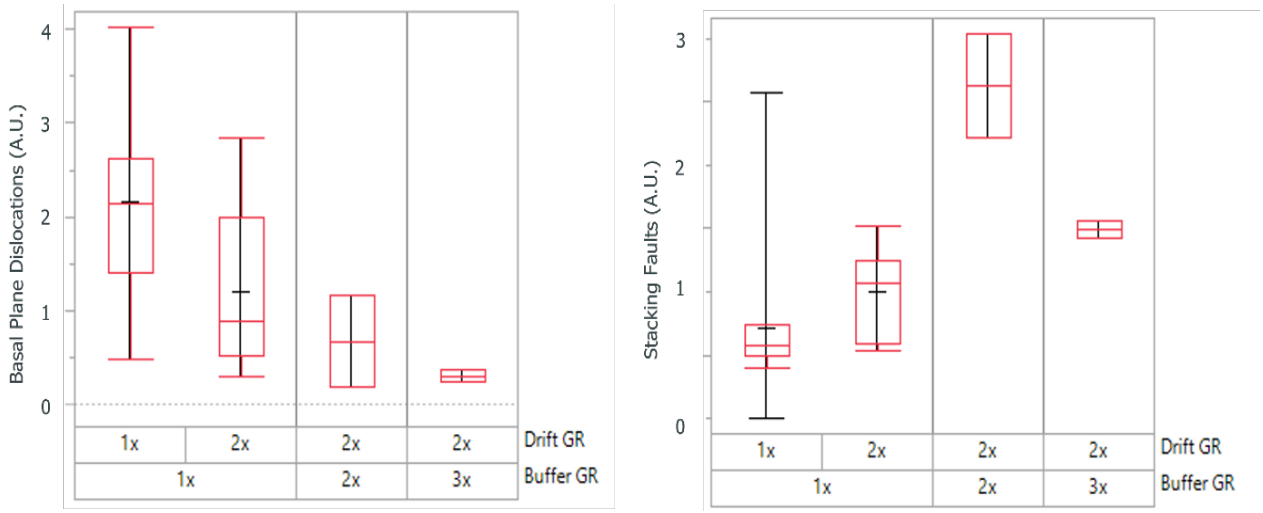

Fig. 1. Optimization of the buffer and drift layer growth rates (GR) are performed. a) BPD is reduced with higher growth rate and b) stacking faults are increased with higher growth rates.

We study surface defects on the epitaxy grown at different thicknesses using Sica88. We find that surface degrades with increased roughness with thicker epitaxies, visible from the surface images with pits and bumps. Threading screw/edge dislocations (TSD/TED) in the substrates can introduce pits in the epilayers [3]. These pits grow significantly larger for the thicker epitaxies (60µm, 100µm, 200µm). We observe that for thicker epitaxies, these pits also create bump and wave-like features from the pit center, towards $11\bar{2}0$ direction (Fig.2).

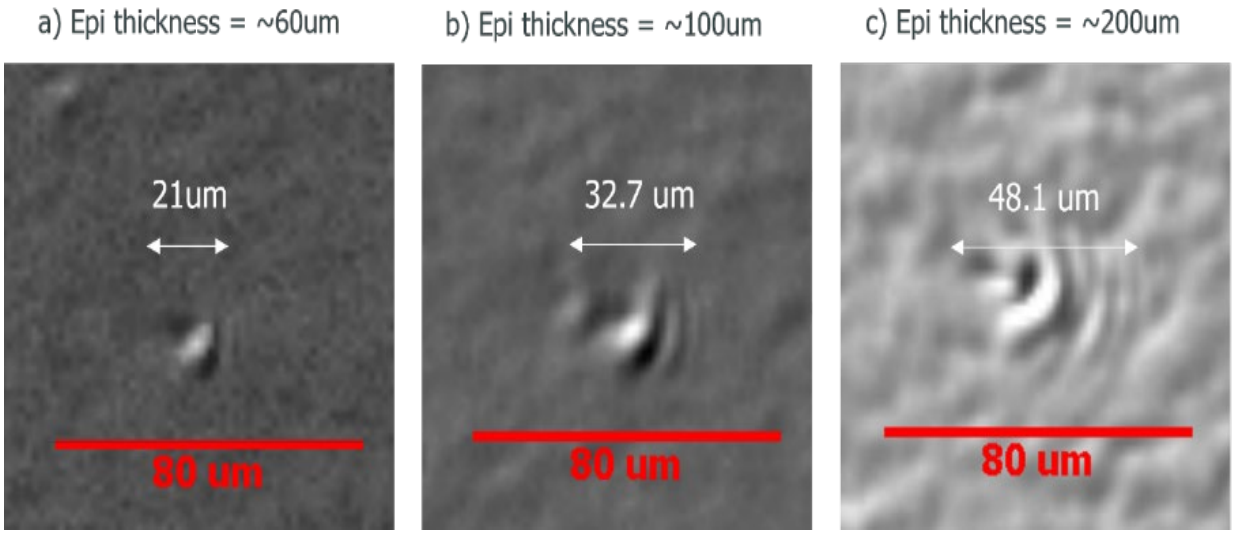

Fig. 2. Examples of pits in the epi at different thicknesses. a) smaller (21µm) size epi pits are seen for ~60µm epilayer, with waviness on the right side of the pit towards $11\bar{2}0$ direction. These pits and the consequent wave shapes becomes larger for thicker epitaxy (b and c).

On the other hand, intricate shapes of basal plane dislocations (BPD) as pileups are seen in the PL images as described in [4]. We find that these BPD pileups are mainly seen at the edge of the wafers (Fig. 3), or around any obstructions on the step flow (e.g. particle, triangular defects etc.).

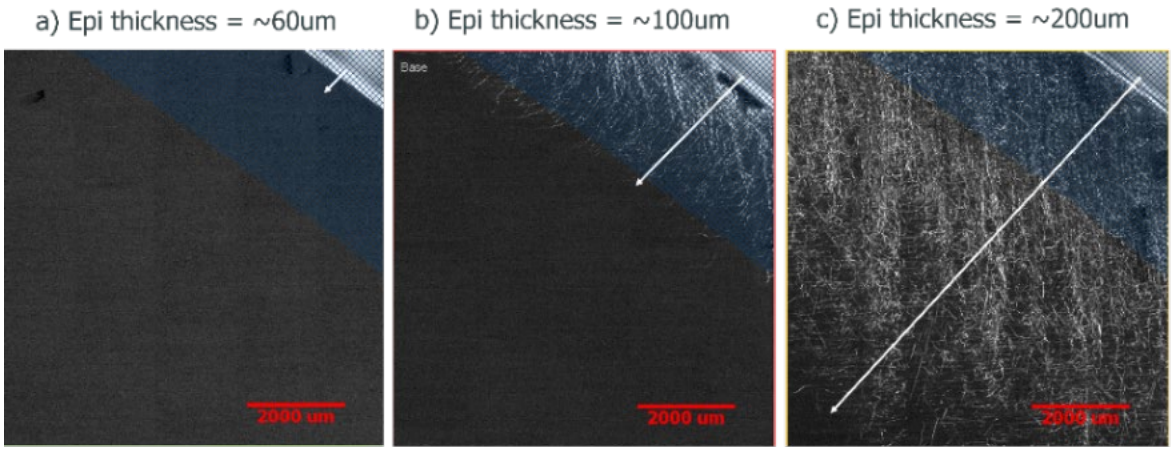

Fig. 3. PL images are shown for the epilayers grown with different thicknesses. Intricate lines of PL BPDs are seen for the thicker epi (100µm, 200µm). The width of the impact increases for thicker epi, extending upto 15µm from the edge. Shaded region shown as typical edge exclusion (3µm).

Initially, we study on the effect of polishing for 60µm epilayers to smooth out the pits and high step bunching associated with the thick epitaxy. We find that a surface removal of ~0.5um by polishing effectively removes pits on the surface for 60µm epi (Fig. 4).

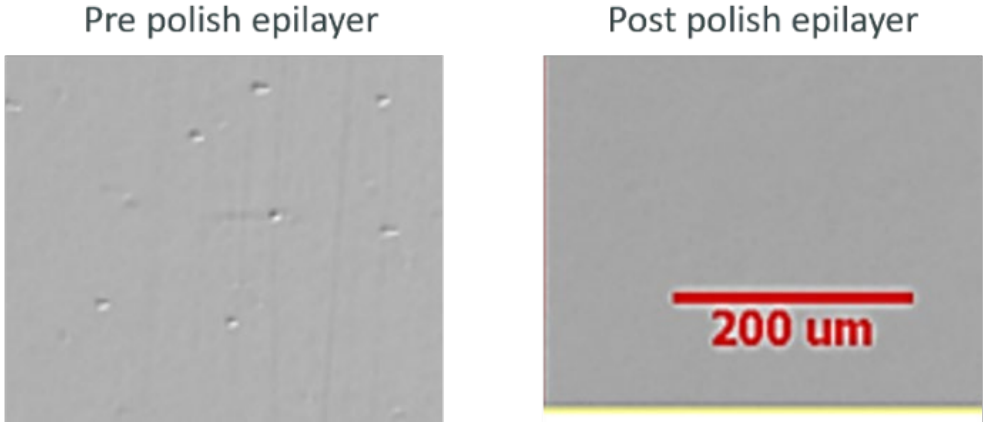

Fig. 4. Surface images are shown for a ~60µm epilayer. a) large pits and step bunching are seen for the epilayer b) These pits and step bunchings are removed by planarization technique (polishing).

We conduct similar polishing study for the 100µm and 200µm epitaxy with a ~1µm removal to have the similar effect to remove pits and bumps (Fig. 5).

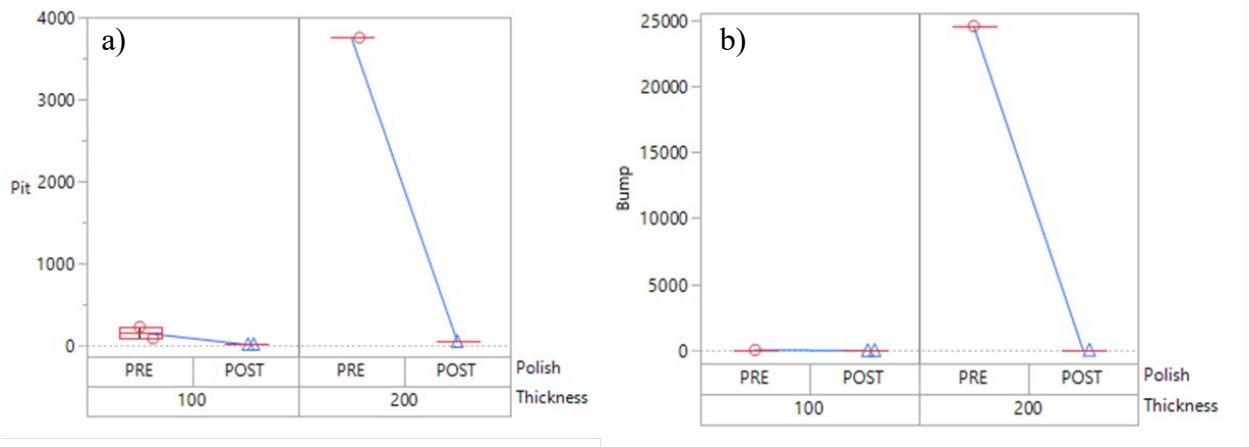

Fig. 5. a) Pits and b) bump reduction by polishing in 100µm and 200µm epilayer.

Larger sized pits and bumps in 200µm epilayers render total usable area (TUA) poorly (~2%). Hence, Si face polishing was essential to smooth out the surface. Si face polishing (1µm removal) significantly reduces pits and bumps in the epilayer (Fig. 5). With polishing, we demonstrate TUA of 98% for 100µm and 95% for the 200µm epilayer, respectively. Even though polishing removes pits and bumps from the surfaces, it cannot remove particle-induced [5], larger morphological defects, like carrot, triangles etc., especially which originate closer to substrate-epilayer interfaces (Fig. 6).

Finally, we study the effect of polishing on the wafer shape. We find that wafer bows are reduced after polishing (Fig. 7). This is due to stress reduction by removal of Si and C faces.

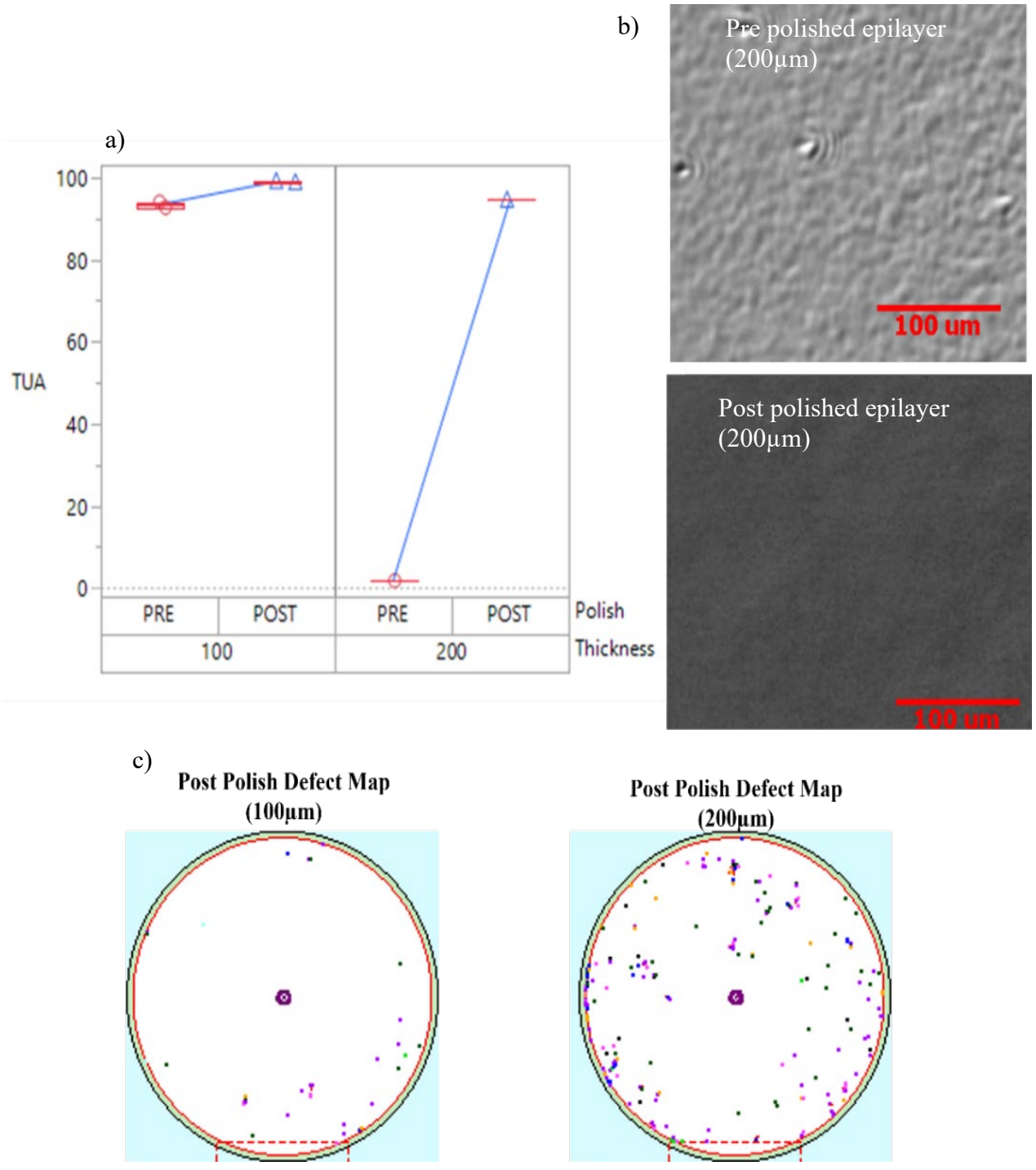

Fig. 6. a) Polishing steps increase total usable area (TUA) for thick epitaxy by eliminating pits and bumps in the epilayer (b, c).

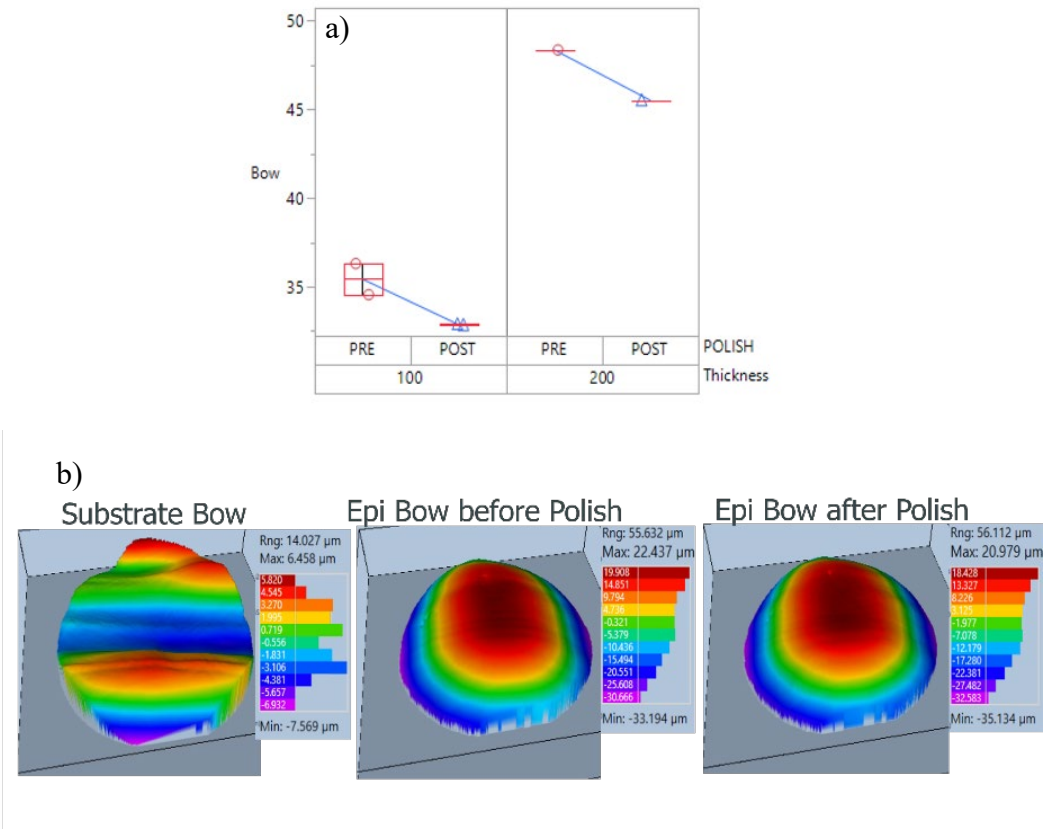

Fig. 7. a) Shape transformation is shown for substrate to epilayer after the polishing of 200µm epilayer b) Polishing reduces the bow for both 100µm and 200µm epitaxy.

Summary

Higher growth rate is found to be beneficial for BPD conversion but may have adverse effect on stacking fault generation. Pit and bump sizes increase with higher thickness and polishing is essential to smooth out the surface. BPD crowding or pileup at the edge increases for thicker epitaxy and may impact up-to 15mm from the edge for 200µm epitaxy. We demonstrate 95%-98% TUA after polishing for 100µm and 200µm epitaxy. Thick epitaxy is challenging due to higher morphological and extended defects, which critically impact TUA of the ultra-thick epitaxy. Further optimization is required to reduce particle related defects and improve surface quality (pit, bumps etc.) for ultra thick epitaxy.

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