Solid State Phenomena
ISSN: 1662-9779, Vol. 393, pp 59-64
doi:10.4028/p-NdIf3k

Submitted: 2025-09-23
Revised: 2026-02-04
Accepted: 2026-02-23
Online: 2026-05-18

Optimization of Seed Crystal Stability at the Initial Growth Stage Depending on Heating Ramp Rates and Gas Flow Channels of SiC Source Powder for Growth of 8-inch *n*-Type 4H-SiC Single Crystal

Chae-Young Lee[1,a*], Su-Ho Kim[1,b], Jung Woo Choi[1,c], Myung-Ok Kyun[1,d], Jung Gyu Kim[1,e], Kap-Ryeol Ku[1,f], Yeon-Suk Jang[1,g], Jung-Gon Kim[2,h], Won Jae Lee[2,i*]

[1]Senic, 17-15, 4sandan 7-ro, Jiksan-eup, Seobuk-gu, Cheonan-si, Chungcheongnam-do, Republic of Korea

[2]Dong-Eui University, 176, Eomgwang-ro, Busanjin-gu, Busan, Republic of Korea

[a]cylee@eincrystal.co.kr, [b]shkim@eincrystal.co.kr, [c]jwchoi@senic.co.kr, [d]bjk006@eincrystal.co.kr, [e]jgkim@senic.co.kr, [f]krku@senic.co.kr, [g]ysjang@senic.co.kr, [h]kimjg@deu.ac.kr, [i]leewj@deu.ac.kr

Keywords: 4H-SiC, 8-inch SiC growth, Physical vapor transport, Single crystal, Ramp rates, Gas flow, Source powder

Abstract. Seed crystal stabilization during the initial stage of 200-mm 4H-SiC crystal growth is critical for achieving high-quality wafers with large diameters. This study investigated the effects of heating ramp rates (0 - 6 °C/min) and SiC source powder porosity through both simulation and experimental approaches. Low ramp rates resulted in surface degradation of the seed crystal, whereas high ramp rates induced significant thermal stress, leading to cracking. Optimal ramp rates of 3 - 5 °C/min significantly minimized damage caused by seed crystal loss. Furthermore, high-porosity source powder facilitated adequate gas transport channels, thereby enhancing seed crystal stability. Crystals grown under these optimized conditions demonstrated improved edge morphology, absence of polycrystalline inclusions, and low dislocation densities, with threading screw dislocations (TSD) below 500 cm^{-2} and basal plane dislocations (BPD) below 1,000 cm^{-2}. These results demonstrate that precise control of thermal parameters and source powder porosity offers an effective strategy for stable seed attachment and reproducible growth of high-quality, large-diameter SiC single crystals.

Introduction

The next generation of wireless infrastructure will rely on wide bandgap semiconductors such as SiC and GaN due to their superior physical properties, including a large bandgap, high thermal conductivity, and high breakdown field. [1, 2] In the SiC wafer-based device industry, increasing the wafer diameter is critically needed to enhance economic viability and production efficiency. [3, 4] Current research is intensively aimed at producing high-quality 8-inch SiC crystal ingots, with a strong focus on preventing internal polycrystalline inclusions. Ensuring the stability of the seed crystal during the initial growth stage is essential for achieving reliable and consistent crystal growth. In this study, we investigated the effects of heating ramp rates and source powder porosity on the growth of 8-inch 4H-SiC crystals. These factors can influence damage to the seed crystal during the initial growth stage, as well as affect the quality of the final crystal. Prolonged thermal exposure at low ramp rates leads to surface degradation and seed crystal detachment at the initial growth stage. In contrast, a fast ramp rate can induce steep thermal gradients, increasing the thermal stress mismatch between the seed crystal and the graphite lid, which often leads to cracking and seed detachment. [5, 6] To address these issues, SiC powders with varying porosities were utilized to optimize gas transport channels under appropriate heating ramp rates, aiming to stabilize the flow of sublimated gas species during the initial growth stage.

Experiments

The growth of 200-mm 4H-SiC crystals was conducted at temperatures ranging from 2300 to 2400 °C under a growth pressure of 20 torr, using both N_2 and Ar atmospheres. 4° off-axis, c-face substrates were used as seed crystals. Simulations were conducted using Virtual Reactor software (STR Software) during the initial growth process with heating ramp rates ranging from 0 to 6 °C/min. Additionally, seed crystal damage tests were performed based on the porosity of the SiC source powder. The defect density near the top (facet region) and bottom (near seed region) of SiC crystals grown under high gas flow conditions was examined following KOH etching. The spatial distribution of defects, including micropipes, inclusions, and stacking faults, was analyzed using a Candela system (KLA-Tencor Corp.).

Result and Discussion

Figure 1 (a) presents a schematic diagram of the experimental setup. The left diagram shows the thermal field at higher ramp-up rate, while the right one depicts that at a lower ramp-up rate near the seed region. Simulations were performed in the initial process with heating ramp rates ranging from 0 to 6 °C/min. Figure1 (b) exhibited the relationship between the seed loss-induced damage width (mm) and the heating ramp rate (°C/min) during the initial stage of crystal growth. The damage width represents the actual measured length from the single crystal toward the crystal edge where degradation begins, as identified through optical microscopy of the grown ingot. It is clear that ramp rates of 3~5 °C/min can effectively decrease the damage width of seed crystal. Compared with the narrower thermal field at a lower ramp-up rate, a higher ramp-up rate broadens the thermal field, thereby reducing thermal etching in the seed region and consequently decreasing seed damage. The determination coefficient ($R^2 = 0.9433$) signifies that the trend line accounts for approximately 94.3% of the variation in damage width (mm) relative to ramp rate (°C/min), demonstrating a strong correlation between ramp rate adjustments and the extent of seed crystal damage reduction.

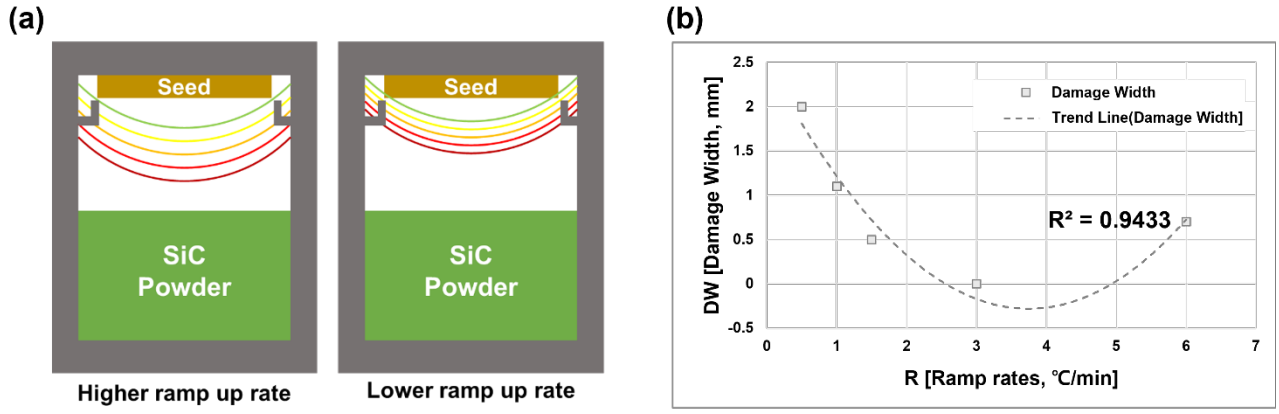

Fig. 1 Schematic diagram of the experimental setup configuration and (b) plot of seed loss-induced damage width (mm) as a function of heating ramp rates (°C/min) at the initial growth stage. R^2 shows the result of quadratic curve-fitting.

Figure 2 shows (a) a schematic illustration of gas flow channel distributions in the SiC source powder region under low and high porosity conditions, and (b) the variation of damage width (mm) as a function of the gas flow channel formed within the source powder. The damage width of the seed crystal was significantly reduced under conditions of high gas flow channels (high porosity) in the SiC source powder. The determination coefficient ($R^2 = 0.9611$) indicates that the trend line explains approximately 96.1% of the variation in damage width (mm) with respect to the powder porosity of the SiC source powder, highlighting a marked correlation between gas flow channel adjustments and the reduction of seed crystal damage. Based on the simulation results, crystal growth experiments were carried out by the PVT method using two configurations with different ramp rates and source powder porosities.

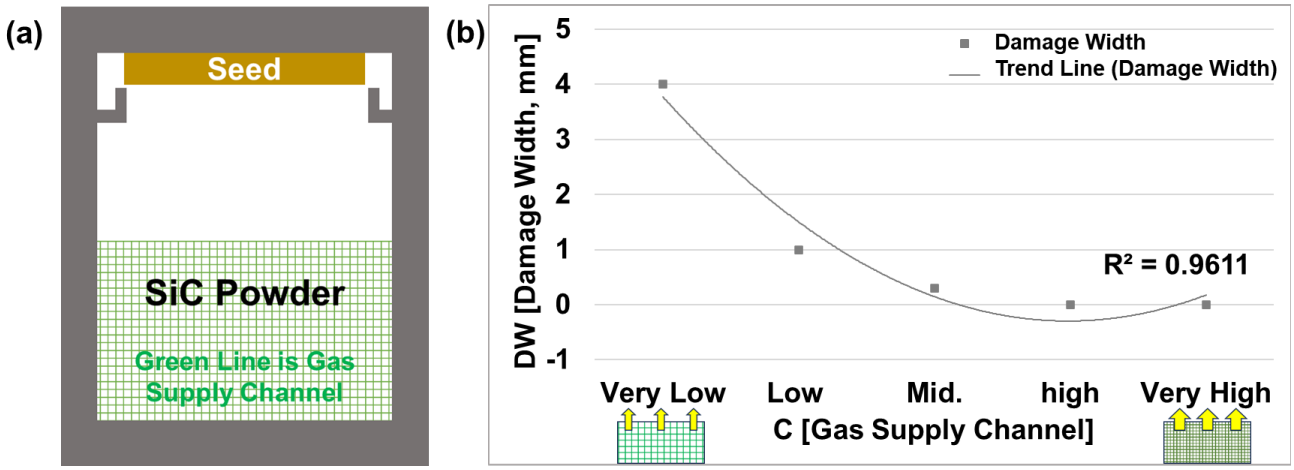

Fig. 2 (a) Schematic diagram of the channel distributions for gas flow at low and high porosity of SiC source powder and (b) plot of the damage width (mm) as a function of the gas flow channel of the SiC source powder. R^2 shows the result of quadratic curve-fitting.

Figure 3 presents the numerical simulation results illustrating the effect of source material porosity on the internal thermal distribution and the resulting mass transport characteristics driven by the temperature gradient between the source and the seed. Porosity determines the resistance to gas-phase transport through the source material. Higher porosity generally increases the permeability, allowing for more efficient mass transport. The six measurement points in the graphite crucible are defined as follows: P1, center of the crystal; P2, edge of the crystal; P3-P4, surface of the source material; and P5 - P6, bottom of source material. With increasing porosity (0.2 to 0.7,), an enhancement in vapor transport of SiC source species from the source is observed.

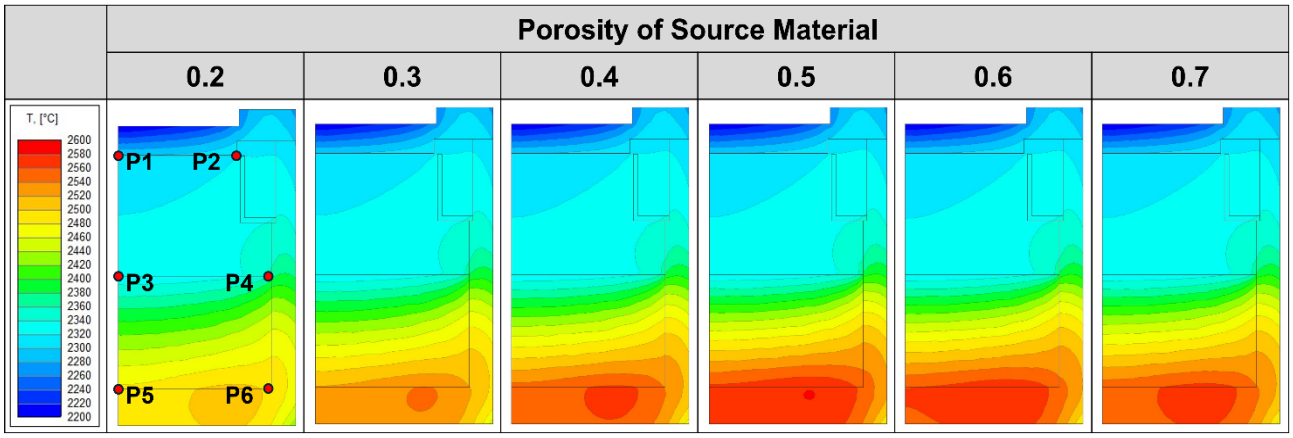

Fig. 3 Numerical simulation of the effect of source material porosity on internal thermal gradients and mass-transport characteristics. The six measurement points in the graphite crucible are defined as follows: P1, center of the crystal; P2, edge of the crystal; P3-P4, surface of the source material; and P5 - P6, bottom of source material.

Figure 4 presents the dependence of (a) mass source, (b) sublimation rate, (c) C/Si ratio, (d) SiC_2 ratio, (e) Si_2C ratio and (f) Si ratio on the porosity of the source material. These ratios (SiC_2, Si_2C, Si ratio, dimensionless quantity) represent the partial pressure share or mole fraction of each species within the total gas phase. Notably, at a porosity of 0.4, the C/Si ratio in the seed surface region reached a stabilized state. This stabilization is attributed to the simultaneous increase in carbon-carrying species SiC_2 and Si_2C and a corresponding decrease in the Si ratio, suggesting that a porosity of 0.4 provides an optimal balance between thermal distribution and gas-phase stoichiometry for high-quality SiC growth. Figure 5 shows optical images (left half) and UVF images (right half) of SiC ingots grown under (a) non-optimal porosity and (b) optimal porosity conditions of the source powder.

Due to the minimized seed crystal loss, the SiC ingot grown at a porosity of 0.4 exhibited superior edge quality and was free of polycrystalline regions compared with ingots grown under other porosity conditions.

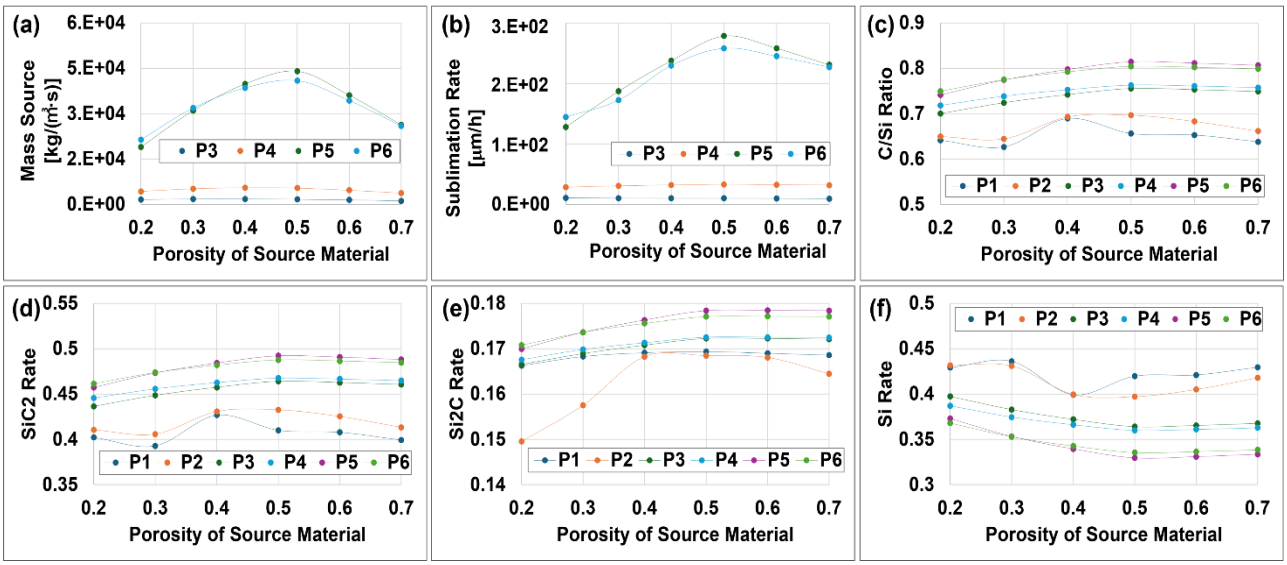

Fig. 4 Dependence of (a) mass source, (b) sublimation rate, (c) C/Si ratio, (d) SiC_2 ratio, (e) Si_2C ratio and (f) Si ratio on the porosity of the source material. SiC_2, Si_2C, and Si ratios are dimensionless quantities.

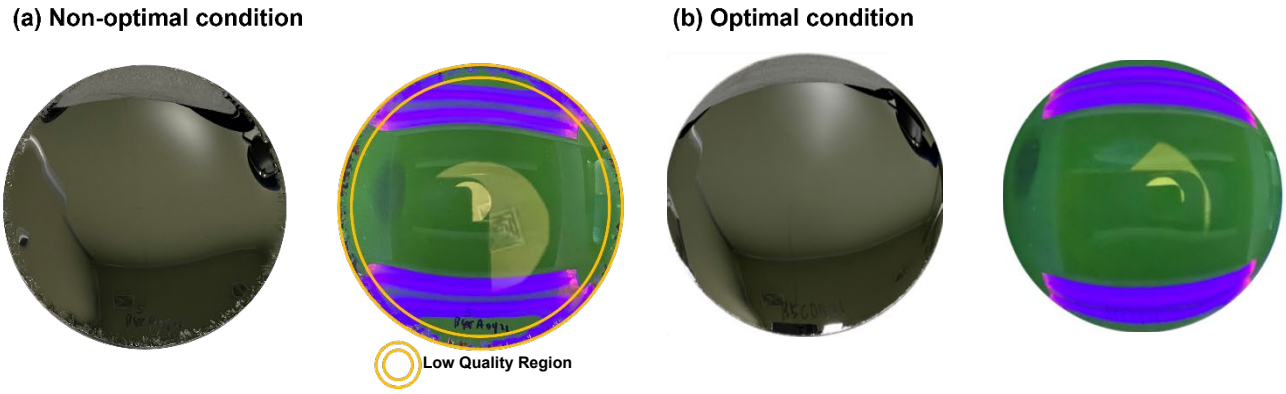

Fig. 5 Optical images (left half) and UVF images (right half) of SiC ingots grown under non-optimal porosity (a) and optimal porosity (b) conditions of the source powder. The bluish regions at the upper and lower ends of the ingots represent optical illusions caused by interference.

Defect densities at the top (near the surface region) and bottom (near the seed region) of the SiC crystal grown under optimal porosity conditions (porosity: 0.4) were investigated after KOH etching and are summarized in Table 1. Both threading screw dislocation (TSD) and basal plane dislocation (BPD) densities were found to be below 500 cm^{-2} and 1,000 cm^{-2}, respectively, indicating high crystalline quality. As shown in Fig. 6, growth under optimal porosity conditions resulted in low TSD and BPD densities, confirming the high crystal quality. Moreover, defect densities at the top and bottom of the wafer were comparable.

Table 1. Defect densities of the SiC crystal measured at the top (facet region) and bottom (near seed region) after KOH etching, under optimal porosity growth conditions.

Measurement positions	TSD (ea/cm^2)	BPD (ea/cm^2)	TED (ea/cm^2)	EPD (ea/cm^2)
Top	450	1,000	2,100	3,550
Bottom	480	920	2,300	3,700

*Threading Screw Dislocation (TSD), Basal Plane Dislocation (BPD), Threading Edge Dislocation (TED), Etch Pit Density (EPD)

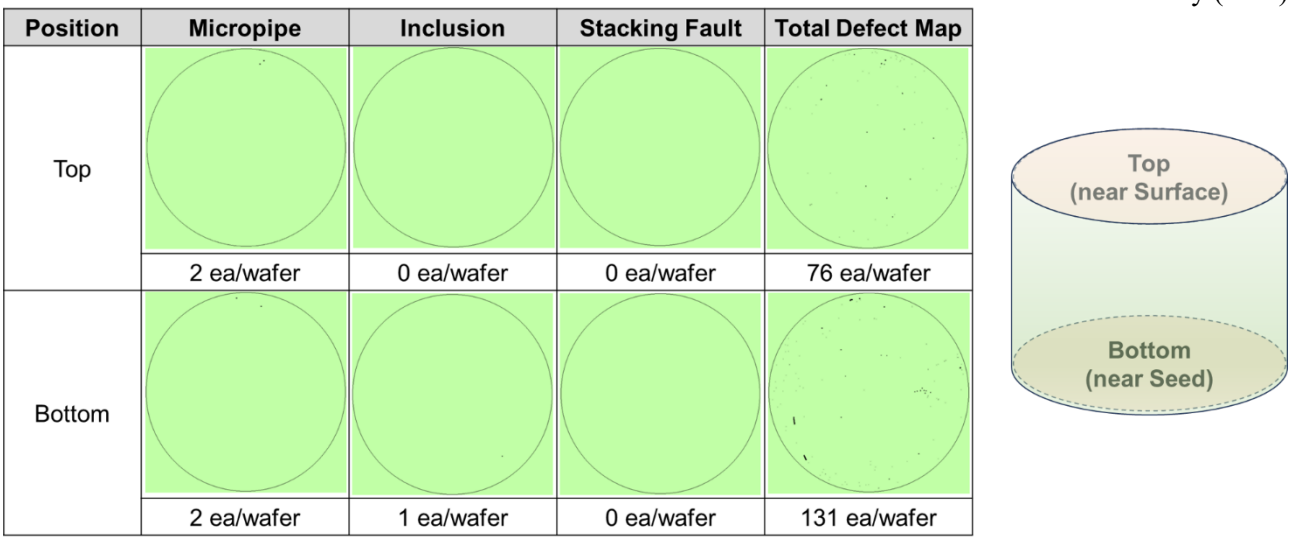

Fig. 6 Defect levels at the top (near surface) and bottom (near seed) of SiC crystals grown under optimal porosity conditions, measured using a Candela system (KLA-Tencor Corp.).

Summary

This study demonstrates that optimizing process parameters during the initial stage of SiC single crystal growth is crucial for minimizing damage caused by seed loss. Both simulations and experimental results confirm that heating ramp rates between 3 and 5 °C/min combined with higher porosity of the SiC source powder significantly reduce seed damage. SiC ingots grown under these optimized conditions exhibit superior edge quality, absence of polycrystalline regions, and low dislocation densities (TSD < 500 cm^{-2}, BPD < 1,000 cm^{-2}). These findings establish an effective process strategy for producing high-quality SiC single crystals and provide practical guidance for large-diameter crystal growth.

Acknowledgements

This work was supported by Technology Innovation Program (Project Number: 00402234, Project Name: Development of highly flat, highly clean large area polished SiC single crystal wafers by utilizing advanced process technology for power semiconductor application) funded by the Ministry of Trade, Industry and Energy.

References

[1] J. R. Jenny, D. P. Malta, St G. Müller, A. R. Powell, V. F. Tsvetkov, H. McD Hobgood, R. C. Glass, C. H. Carter Jr., Journal of Electronic Materials, 32, 432-436 (2003).

[2] M. V. S. Chandrashekhar, I. Chowdhury, P. Kaminski, R. Kozlowski, P. B. Klein and T. Sudarshan, Applied Physics express 5, 025502 (2012).

[3] I. Manning, K. Moeggenborg, A. Soukhojak, J. Searson, M. Gave, G. Chung, E. Sanchez, Materials Science Forum, 1062, 54-58 (2022).

[4] S. Zhang, G. Fu, H. Cai, J. Yang, G. Fan, Y. Chen, T. Li, L. Zhao, Materials, 16(2), 767 (2023).

[5] J. Steiner, P. J. Wellmann, Materials, 15(5), 1897 (2022).

[6] J. Pezoldt, V. Cimalla, Crystals, 10(6), 523 (2020).