

Table of Contents

Preface

Chapter 1: Substrate and Epitaxial Layer Manufacturing

Study on Homoepitaxy Performance of Engineered 150 mm and 200 mm SiC Substrates in a Multi-Wafer Batch Reactor P. Hens, K.M. Albrecht, B. Kallinger, R. Karhu and J. Erlekampf	3
A Study of Epitaxial Growth on 4H-SiC Substrates Treated by Plasma Polish Dry Etch (PPDE) Process T. Rana, K. Moeggenborg, L. Reyes, K.I. Stokeley, S. Johnson and E. Sanchez	12
Thick Semi-Insulating 4H-SiC Layer Exfoliation for Non-Epitaxial Engineered Substrates H. Jayaprakash, C. Csato, R. Koch, F. Krippendorf and M. Rueb	18
Lab-Based X-Ray Topography Characterization of Axial Samples from 4H-SiC Boules Grown by PVT Method Y. Liu, C. Bouch, P. Schunemann, R. Philpott, M. Safko, D. Hamann, M. Dupre and A. Goldberg	28
New Insights in Orientation and Growth of 150 mm GaN on SiC for HEMT C. Calabretta, N. Piluso, S. Boninelli, C. Iatosti, E. Roy, D. Calabriso, L. Lilja, A. Ellison, C. Riva, F. Iucolano and A. Severino	37
Process Gas Control for High-Resistance HPSI-SiC Growth S.J. Lee, S.H. Kim, C.Y. Lee, J.H. Park, J.W. Choi, J.G. Kim, K.R. Ku, G.U. Lee and W.J. Lee	42
High-Temperature Adhesive Bonding of 4H-SiC Substrates P. Parmar, M.K. Yadav, C. Zellner, G. Wedl, G. Pfusterschmied and U. Schmid	48
New Insights into the Occurrence of Prismatic Slip during PVT Growth of SiC Crystals S.S. Hu, B. Raghothamachar, Z.Y. Chen, K.W. Kayang, D. Gersappe, M. Dudley, V. Torres, D. Dukes, D. Lang, A. Martin, H. Briccetti, S. Griswold, T. Kegg and N. Griffin	56
SmartSiC™ 150 & 200mm Engineered Substrate: Enabling SiC Power Devices with Improved Performances and Reliability E. Guiot, G. Picun, F. Allibert, A. Drouin and W. Schwarzenbach	64
Development of a Novel Warpage Control Method for Epi-Ready 4H-SiC Wafers by Depositing Homoepitaxial Layers on both Si- and C-Faces D. Dojima, S. Jeong, K. Toda and T. Kaneko	74
Improvement of the Yield during Crystal Growth of SiC by PVT by Proper Selection and Design of Hot Zone Isolation Components S. Strüber, J. Ihle, J. Zöcklein, J. Steiner and P.J. Wellmann	81
Filling-Design Effect of Powder Source in the Crucible on SiC Single-Crystal Growth M.K. Kang, G.U. Lee, Y.J. Choi, G.J. Song, N.K. Kim, M.S. Park, K.H. Jung and W.J. Lee	91
Nitrogen Dopant Incorporation into Epitaxial 4H-SiC and the Influence of CVD Growth Parameters A. Schrader, N. Steller, D. Reimann and F. Faisal	98
Epitaxial SiC Development for High Nitrogen Incorporation B.L. VanMil, C.H. Burgess, H. Wen and F. Ayazi	106
The 4H-SiC Epitaxy Study of Ammonia Doping Y.B. Han, Z.Y. Li, Y.X. Niu, D. Li, H.L. Yan and J.X. Shi	112
Formation of Alternating Epilayers of 4H-SiC and 3C-SiC by Simultaneous Lateral Epitaxy H. Nagasawa, M. Abe, T. Tanno, M. Musya, M. Sakuraba, S. Sato, Y. Watanabe and M. Suemitsu	121
Predictive Doping and Thickness Analysis of a Multi-Wafer SiC Warm-Wall Epi Reactor for Improved Layer Cpk M.A. Johar, K. Singh and A.A. Burk Jr.	130
Recent Advancement in Noncontact Wafer Level Electrical Characterization for WBG Technologies M. Wilson, A. Savtchouk, L. Gutierrez, C. Almeida and J. Lagowski	135

Active Planarization Method from Rough Surface of 4°-off 4H-SiC (0001) Controlled by Step Bunching and Debunching Mechanism Using Dynamic AGE-ing® K. Toda, K. Kiritani, D. Dojima and T. Kaneko	143
The Application of Dynamical Thermal Annealing Processes after Mechanical Slicing as an Integrated Contactless SiC Wafering Method to Control Crystal Defects K. Toda, D. Dojima, Y. Nakajima, H. Mihara and T. Kaneko	149
Optimization of Heat Transfer Design for High Quality 4H-SiC Ingot Growth S.J. Lee, S.H. Kim, C.Y. Lee, J.H. Park, J.W. Choi, H.S. Lee, J.G. Kim, K.R. Ku, M.K. Kang and W.J. Lee	155
High-Quality SiC Crystal Growth by Cooldown Rate Control at Cooling Stage C.Y. Lee, S.H. Kim, S.J. Lee, J.H. Park, J.W. Choi, H.S. Lee, J.G. Kim, K.R. Ku, Y.J. Choi and W.J. Lee	160

Chapter 2: Structural Defects in Silicon Carbide

Deep-Ultraviolet Laser-Based Defect Inspection of Single-Crystal 4H-SiC and SmartSiC™ Engineered Substrates for High Volume Manufacturing E. Cela, W. Schwarzenbach, R. Shrestha, G. Bast, S. Shahidi and G. Simpson	167
Study of In-Grown Micropipes in 200 mm 4H-SiC (0001) Epitaxial Substrate A.M.A. Lee, X.Y. Li, Q.G.R. Voo, S. Kumar, E.S. Tok, U. Chand, L.K. Bera, H.L.R. Maddi, S. Chung, F. Hébert, N. Singh and Y.C. Yeo	173
Demonstration of Suppressing ISSF Expansion Using Energy Filtered Ion Implantation H. Jayaprakash, C. Csato, M. Kato, T. Li, F. Krippendorf and M. Rueb	178
Analysis of Trap Centers Generated by Hydrogen Implantation in 4H-SiC Bonded Substrates H. Uchida, M. Kobayashi, N. Hatta, S. Ishikawa, Y. Higashi, H. Sezaki, S. Harada and K. Kojima	186
Analysis of Lattice Damage in 4H-SiC Epiwafers Implanted with High Energy Al Ions with Silicon Energy-Filter for Ion Implantation Z.Y. Chen, Q.Y. Cheng, S.S. Hu, B. Raghothamachar, C. Carlson, D. Steski, T. Kubley, F. Krippendorf, M. Rüb, R. Koch, R. Ghandi, S. Kennerly and M. Dudley	193
Formation Mechanism and Complex Faulting Behavior of a BPD Loop in 180 µm Thick 4H-SiC Epitaxial Layer Z.Y. Chen, N.A. Mahadik, M. Dudley, B. Raghothamachar, D.A. Scheiman, R.E. Stahlbush, Y.S. Kim and M.W. Owen	199
Evaluation of 4HSiC Epitaxial CVD Process on Different 200 mm Substrates for Power Device Applications C. Nania, D. Raciti, C. Calabretta, F. Vento, R. Anzalone, E. Fontana and A. Severino	206
Characterization of Interface Trap and Mobility Degradation in SiC MOS Devices Using Gated Hall Measurements S. Das, D.J. Lichtenwalner, S.R. Stein and S.H. Ryu	211
Numerical Analysis of Correlation between UV Irradiation and Current Injection on Bipolar Degradation in PiN Diodes Y. Igarashi, K. Takano, Y. Matsushita and T. Morita	216
Investigation on Bipolar Degradation Caused by Micropipe in 3.3 kV SiC-MOSFET H. Niwa, T. Tanaka, K. Ishibashi, H. Amishiro, A. Imai, Y. Kagawa, K. Sugawara and T. Watahiki	223
Suppression and Analysis of Bipolar Degradation in 4H-SiC PiN Diodes through Proton Implantation A. Shimbori, R. Wada, N. Tokoro, T. Kuroi, H.Y. Wong and A.Q. Huang	229
Punching of Prismatic Dislocation Loops from Inclusions in 4H-SiC Wafers Q.Y. Cheng, K.W. Kayang, Z.Y. Chen, S.S. Hu, B. Raghothamachar, M. Dudley, D. Gersappe, A. Soukhovjak and S. Baek	236
Exploring the Influence of Implant Profile and Device Design on Basal Plane Dislocation Generation in 1.2kV 4H-SiC Power MOSFETs S.A. Mancini, S.Y. Jang, Z.Y. Chen, B. Raghothamachar, M. Dudley and W.J. Sung	245
Coherency between Epitaxial Defectivity, Surface Voltage, Photoluminescence Mapping and Electrical Wafer Sorting for 200mm SiC Wafers J. Thörnberg, G. Polisski, S. Giuffrida, V. de Luca, A. Catena, M. Wilson and B. Magnusson	253

Defect Density Reduction in 4H-SiC (0001) Epilayer via Growth-Interruption during Buffer Layer Growth	
S. Kumar, L.K. Bera, X.S. Nguyen, W.D. Song, A.M.A. Lee, X.Y. Li, E.S. Tok, M.S. Bharathi, C.D. Reddy, U. Chand, S. Chung, N. Singh and Y.C. Yeo	261
Dynamics of Stacking Fault Expansion in H⁺ Implanted SiC-MOSFETs	
K. Ishibashi, N. Shikama, H. Niwa, T. Tanaka, H. Amishiro, A. Imai, K. Sugawara, Y. Kagawa and A. Furukawa	266
Challenges in Investigating UIS Material-Based Failures & Yield Prediction in the Absence of Robust 4H-SiC Epiwafer Quality Standards	
J. Soto, B. Odekirk, S. Maximenko, B. Rodgers, M. Fisher and K. Speer	274
Polarization Superimposed Phase Contrast Microscope Inspection of Dislocations in SiC Epitaxial Layer	
R. Hattori, Y. Yao and Y. Ishikawa	280
High Temperature Evolution of Thin Films Confined between Two SiC Substrates	
M. Le Cunff, F. Rieutord, D. Landru, O. Kononchuk and N. Cherkashin	288
Non-Contact Full Wafer Imaging of Electrically Active Defects in 4H-SiC Epi with Comparison to End of Line Electrical Device Data	
F. Faisal, N. Steller, R. Karhu, B. Kallinger, G. Polisski, M. Wilson, A. Savtchouk, L. Gutierrez, C. Almeida, D. Marinskiy and J. Lagowski	296
How to Simulate Bipolar Degradation by UV Irradiation with High Accuracy	
Y. Igarashi, K. Takano, Y. Matsushita and T. Morita	303

Chapter 3: Processes and Technological Improvements in Devices Fabrication

Isolation Structure for Monolithic Integration of Planar CMOS and 1.7 kV Vertical Power MOSFET on 4H-SiC by High Energy Ion Implantation	
Y.J. Lin, C.H. Chen, M.H. Wang and B.Y. Tsui	313
Impact of Silicon Nitride Stress on Defects Generation in 4H-SiC and the Effect of Sacrificial Oxidation on Defects Reduction	
K.W. Hsu, H.L. Huang, C.L. Hung, Y.K. Hsiao and B.Y. Tsui	321
Impact of Interfacial SiO₂ Layer Thickness on the Electrical Performance of SiO₂/High-K Stacks on 4H-SiC	
S. Krause, A. Mikhaylov, U. Schroeder, T. Mikolajick and A. Wachowiak	328
Evolution of the Electrical and Microstructural Properties of Mo/4H-SiC Contact with the Annealing Temperature	
M. Vivona, P. Fiorenza, G. Greco, S. Di Franco, G. Bellocchi, P. Mancuso, S. Rascunà, A.M. Mio, G. Nicotra, F. Giannazzo and F. Roccaforte	337
Rapid Thermal Anneal with Conductive Heating for SiC Contact Formation	
X. Pages, S. van der Linde, J. Oterdoom, M. Steltenpool, V. Kuznetsov, J. Beijersbergen, M. Sanchez and S. Kerdilès	343
The Investigation of Effective Thermal Oxidation to SiC MOSFET Gate Oxide Quality Improvement	
Y.B. Im, I.K. Kim, J.Y. Yoon, J.G. Lee, G.H. Park, J.S. Lim, J.W. Son, J.H. Lee, Y.J. Jang and C.B. Jeong	351
A Simplified Method for Extracting Contact Resistivity Using the Circular Transmission Line Model	
J.H. Park, J.J.H. Kim, A. Kumar, J. Zacks, D. Flint, D.J. Lichtenwalner and S.H. Ryu	357
BCl₃ Plasma Treatment for Enhanced Ohmic Contact Performance to p-Type 4H-SiC	
A.H. Yeo, Q.G.R. Voo, L.K. Bera, U. Chand, N. Singh, S. Chung, X.S. Nguyen, Z.J. Quek, A. Ranjan, V.P.K. Reddy, S.J.G. Ho, S.K. Lim, M.O. Omar, J.W. Xie, Y.C. Yeo and X. Gong	362
Advantages of Backside Metal Contact Resistance on 4H-SiC Bonded Substrates for Power Devices	
M. Kobayashi, H. Uchida, N. Hatta, S. Ishikawa, Y. Higashi, H. Sezaki, S. Harada and K. Kojima	367
Investigation of Interface and Reliability of 3C- and 4H-SiC MOS Structures through Gate Dielectric Stacking and Post-Deposition Annealing	
M.A. Yildirim, V.A. Shah, M. Antoniou, A. Newton, S. Bolat, G. Colston, A. Graham, R. Jefferies, J.A. Gott, K. Perera, M.J. Powell, P.M. Gammon, P.A. Mawby, R. Gunn and A.B. Renz	374

Deep Implanted SiC Super-Junction Technology R. Ghandi, C. Hitchcock and S. Kennerly	382
Improved Angle Tolerance in 4H-SiC Trench Filling Epitaxy Using Chlorinated Chemistry R. Grover, K. Turner, G. Colston, A.B. Renz, M. Antoniou, P.M. Gammon, P.A. Mawby and V.A. Shah	387
Study of SiC Trench Etching Characteristics for Different Crystal Planes A. Ranjan, L.K. Bera, S. Kumar, H.M. Lin, U. Chand, N. Singh, S. Chung, A.H. Yeo, Q.G.R. Voo, A. Sundaram, L.Y. Liu and J.W.Y. Kam	393
Effects of Sulfurization on the Properties of 4H-SiC Schottky Contacts F. Roccaforte, M. Vivona, S.E. Panasci, S. di Franco, G. Greco, P. Fiorenza, A. Sulyok, A. Koos, B. Pécz and F. Giannazzo	398
C-Face Epitaxy for Enhanced SiC Device Performance: Insights from Schottky Barrier Diodes Q.G.R. Voo, A.H. Yeo, L.K. Bera, U. Chand, Y.C. Chien, X.S. Nguyen, W.D. Song, S. Kumar, H.M. Chua, N. Singh, S. Chung, S. Kam, M. Zielinski, L. Kabelaan, W. Schwarzenbach, I. Radu and L. Boudin	405
Indium-Tin-Oxide (ITO) Interlayer-Assisted Ohmic Contacts on n-Type 4H-SiC with Low Specific Contact Resistance A.H. Yeo, Q.G.R. Voo, L.K. Bera, U. Chand, N. Singh, X.S. Nguyen, S. Kumar, S. Chung, J.W. Xie, Y.C. Yeo and X. Gong	410
Trench Etch Processing for SiC Superjunction Schottky Diodes Q.Z. Cao, A.B. Renz, P.M. Gammon, N. Lophitis, K. Melnyk and M. Antoniou	416
Argon Plasma Treatment of 4H-SiC Surface before Nickel Ohmic Contacts Formation by UV Laser Annealing C. Berger, D. Alquier and J.F. Michaud	425
Analysis of Ohmic Contacts Simultaneously Formed on both n-Type and p-Type 4H-SiC A. Shimbori, R. Valecha and A.Q. Huang	431
Gate Oxide Performance and Reliability on SmartSiC™ Wafers and the Influence of RTA Processing on Gate Oxide Lifetime T. Becker, M. Rommel, H. Schlichting, L. Baier, E. Guiot and F. Allibert	438
Damage Evaluation and Elemental Analysis of SiC Wafers Processed by Water Jet Guided Laser S. Masui, S. Kadoya, S. Takahashi, M. Michihata, N. Ohtani, K. Abe, S. Hirano and S. Arimura	447
Formation of Structured Low-Ohmic p-Type Contacts on Al-Implanted 4H-SiC by Laser Annealing C. Hellinger, M. Thum and M. Rommel	452
Fabrication of the Planar SiC Gate-all-Around JFET with Channel Dose Modulation T. Amamiya, M. Yamamoto, H. Umezawa, K. Nakayama, T. Kuroiwa, S. Kuroki and Y. Tanaka	458
Investigation of Poly-Si Gated, Al₂O₃-Based High-k Dielectrics on 4H-SiC J. Ziegler, D. Scholten, H. Bartolf, A. Voznyi, P. Rabinzohn and J. Schulze	464
Effect of Inserting an Intervening Layer on Φ_b Reduction in TiN Schottky S. Takagi, H. Yoshihashi, K. Tanaka, T. Imamura and H. Kono	471
SiC Plasma Dicing for Future High Yield Die Singulation B. Jones, A. Croot, J. Mitchell, S. Kazemi, C. Bolton, H. Ashraf, M. Jennings and O.J. Guy	477

Chapter 4: Characteristics Evaluation and Device Design

Electrical Characterization of HV (10 Kv) Power 4H-SiC Bipolar Junction Transistor P. Brosselard, B. Fosso-Sob, D. Planson, P. Bevilacqua, C. Sonnevile, M. Lazar, B. Vergne, S. Scharnholtz and H. Morel	487
Investigation on Effect of Electrical Characteristics of Proton Implanted 4H-SiC MOSFET N. Shikama, K. Ishibashi, H. Niwa, T. Tanaka, H. Amishiro, A. Imai, K. Sugawara, Y. Kagawa and A. Furukawa	493
Evaluation of Switching Performances and Short Circuit Capability of a 1.2 kV SiC GAA MOSFET through TCAD Simulations L. Maresca, V. Terracciano, A. Borghese, M. Boccarossa, M. Riccio, G. Breglio, S. Wirths and A. Irace	502

Impact of Positive and Negative High Voltage Gate Stress on Channel Degradation in SiC MOSFETs	
A.S.R. Stein, S. Das, A.K. Biswas, D.J. Lichtenwalner and S.H. Ryu	509
Impact of Single-Step Deep P-Body Implant on 1.2 kV 4H-SiC MOSFET	
P. Vudumula, Y.C. Chien, A.H. Yeo, L.K. Bera, U. Chand, V.Q.G. Roth, S. Chung, N. Singh and Y.C. Yeo	518
Temperature Dependence of 1200V-10A SiC Power Diodes Impact of Design and Substrate on Electrical Performance	
A. Abbas, C. Le Royer, R. Laviéville, J. Biscarrat, G. Gelineau, F. Allibert, E. Bano and P. Godignon	523
Designs of 1.2 kV Rated Semi-Superjunction MOSFET on the 2D and 3D Planes for Practical Realization	
V. Kotagama, A.B. Renz, K. Melnyk, G.W.C. Baker, V.A. Shah, M. Antoniou and P.M. Gammon	533
Superior Characteristics of Body Diode in DMOSFET Fabricated on 4H-SiC Bonded Substrate	
Y. Higashi, S. Ishikawa, K. Oozono, H. Sezaki, M. Kobayashi, H. Uchida, M. Okamoto, S. Harada, K. Kojima, T. Kato and Y. Tanaka	541
1200 V 4H-SiC VDMOSFET Having > 2.5x On-Current Improvement	
Y. Widjaja, V. Nebesnyi, A. Asenov, N. Xeni, I. Topaloglu, D. Bensouiah, S. Rath, R. Young, L. Laborie, Y. Qi, M. Bell and D.T. Clark	550
Static Analysis of Temperature-Dependence of Paralleled High Voltage Vertical Silicon & SiC NPN BJTs	
C. Shen, S. Jahdi, M. Hosseinzadehlish, P. Mellor, K. Floros and I. Lüdtke	556
Economic Feasibility Analysis of Vertical High-Voltage 4H-SiC Superjunction MOSFETs Compared to Conventional Counterparts	
M. Torky and W. Sung	565
Design Parameters Impact on Electrical Characteristics of 4H-SiC Thyristors with Etched Junction Termination Extension	
K. Kotra, S. Scharnholtz, R. Hassdorf, M. Zuvic and K. Hoffmann	574
SiC MOSFETs C-V Capacitance Curves with Negative Biased Drain	
I. Maticena, L. Maresca, M. Riccio, A. Irace, G. Breglio and S. Daliento	582
TCAD Modelling of Anisotropic Channel Mobility in 4H-SiC MOSFETs	
H. Dixit, D.J. Lichtenwalner, A. Scholze and S.H. Ryu	588
On the Characterization of 4H-SiC PiN Diodes and JFETs for their Use in High-Voltage Bidirectional Power Devices	
A.B. Renz, Y. Jiang, P.M. Gammon, E. Bashar and J. Bu	593
The 3rd Quadrant Operation of 4th Generation SiC MOSFETs: Recovery Charge & Bipolar Degradation	
Y. Liu, S. Jahdi, M. Hosseinzadehlish, I. Laird, P. Mellor, K. Floros and I. Lüdtke	601
Optimizing 1.2 kV SiC Trench MOSFETs for Enhanced Performance and Manufacturing Efficiency	
S.Y. Jang, D.Y. Kim, D.C.Y.B.Y. Mudiyanse, H.J. Lee, C.K. Lee, J.G. Kim, D.K. Kim and W.J. Sung	609
Novel SiC MOSFET Edge-Termination Structure for Electric Field Relaxation Using an Oxide Film along the Trench Surface	
Y. Kimura, T. Tominaga, Y. Fukui, A. Iijima, K. Adachi, F. Yamamoto, Y. Kagawa and K. Kono	616
SiC Schottky-Barrier Diode without Ion-Implanted P-Type Regions	
J. Damcevska, S. Dimitrijevic, J.S. Han, D. Haasmann and P. Tanner	623
Three Level Pulses to Investigate Gate Switching Instability	
D. Scholten and J. Uschmann	632
DFT Calculations on the Termination of 4H-SiC Non-Polar Surfaces during Photoelectrochemical Pore Formation	
T.Q. Yang, M. Perazzi, C. Zellner, G. Pfusterschmied and U. Schmid	638
TCAD Model Parameter Calibration Strategy for 1200V SiC MOSFET	
J. Lee, J.M. Kim, S.H. Kim, H.B. Lee, Y.C. Kim and H.C. Nah	646
Lifetime Modeling of MOS Based SiC Vertical Power Devices under High Voltage Blocking Stress	
A.K. Biswas, D.J. Lichtenwalner, B. Hull, D.A. Gajewski and S. Ganguly	652

Matching Physical and Electrical Measurements (OBIC) to Simulation (FEM) on High Voltage Bipolar Diodes	
D. Planson, C. Sonnevile, P. Bevilacqua, P. Brosselard, M. Lazar, S. Scharnholz, B. Vergne and H. Morel	658
Cost-Effective Design and Optimization of a 3300-V Semi-Superjunction 4H-SiC MOSFET Device	
K. Melnyk, M. Boccarossa, A.B. Renz, Q. Cao, P.M. Gammon, V.A. Shah, L. Maresca, A. Irace and M. Antoniou	664
A Physics-Based SPICE Model for a SiC Vertical Power MOSFET	
J.H. Lim, A.U. Rashid, B. Brooks and S.H. Ryu	670
A Novel 'Ladder' Design for Improved Channel Density for 1.2kV 4H-SiC MOSFETs	
S. de Boer, D.C.Y.B.Y. Mudiyanse, S.Y. Jang, A. Morgan and W.J. Sung	678
Single-Event-Burnout in 1.2kV 4H-SiC Lateral RESURF Power MOSFET	
Z.W. He, W. Ji and T.P. Chow	685
Investigation of Advanced Hexagonal Layouts for 650 V SiC MOSFETs	
J.H. Park, S. Sundaresan, A. Agarwal, V. Mulpuri, S. Dail, Y. Dong and N. Walsh	694
A Novel Design of SiC High-Voltage Lateral PiN Diode for IC Application	
X. Ma, M. Ekström and C.M. Zetterling	702
Design and Simulation of Improved Future Generation 4H-SiC JFET-R Integrated Circuits for Prolonged 500 °C Operation	
P.G. Neudeck, C.M. Adams, M.J. Krasowski, D.J. Spry and N.F. Prokop	708
Optimizing Short Channel Designs in 1700 V 4H-SiC VDMOSFET	
S. Rath, L. Laborie, Y. Qi, A. Murphy, M. Bell, R. Young and D.T. Clark	714
Fast High Current Sensing SMD Resistor Network Layout for Low Inductance Insertion	
A. Arrizabalaga and J. Oliver	720

Chapter 5: Analysis of Device Reliability and Characteristic Stability

Dynamic Switching Energy Monitoring during Gate Switching Stress to Evaluate Performance Degradation in Hard Switching Electric Power Conversion Systems	
A. Piccioni, M.W. Feil and T. Aichinger	729
TDDb and HTGB Study of SiC MOSFET with Excessive Channel Leakage	
S.B. Hou, C. Lundgren, W. Kaplan and S. Reshanov	734
Optimization of Gate Oxide Screening Technology for Commercial SiC Discrete MOSFETs and Power Modules	
L.M. Shi, M. Jin, J.S. Qian, M. Bhattacharya, S. Houshmand, H.Y. Yu, A. Shimbori, M.H. White and A.K. Agarwal	739
D_{it} ($\sim 5 \times 10^{10} \text{ eV}^{-1} \text{ cm}^{-2}$), Competitive J_G ($\sim 5 \times 10^{-10} \text{ A cm}^{-2}$) Performance and Enhanced Post-Stress Flatband Voltage Stability Using Deposited Oxide	
U. Chand, Y.C. Chien, A.H. Yeo, Q.G.R. Voo, S. Kumar, A. Ranjan, B. Varghese, W.J. Wang, P. Vudumula, T. Fidler, P. Schmid, M. Saggio, M. Castorina, M. Camalleri, J. Xie, X. Gong, S. Chung, L.K. Bera, N. Singh and Y.C. Yeo	746
Investigation of Overcurrent Turn-Off Robustness of 1200 V SiC MOSFETs	
M.L. Mysore, D.K.P. Kumar, C.H. Wang, J. Lutz and T. Basler	752
Prospects and Challenges for SiC Power Devices in MMC-VSC-HVDC Applications	
O. Alatis, S. Jahdi, P.M. Gammon, J. Ortiz-Gonzalez, M. Hosseinzadehlis, K. Floros and I. Ludtke	761
Dynamic Characterization and Robustness of SiC MOSFETs Based on SmartSiC™ Engineered Substrates	
M. Alaluss, C. Böhm, M.L. Mysore, P. Heimler, T. Basler, A. Elsayed, K. Oberdieck and S. Goel	770
Device Performance and Reliability of SiC CMOS up to 400°C	
E.K. Ashik, S.B. Isukapati, H. Zhang, T.S. Liu, U. Gupta, A.J. Morgan, V. Misra, W.J. Sung, A. Fayed, A.K. Agarwal and B.M. Lee	778

Chapter 6: Quantum Applications, Sensors and Use in Space Engineering

SiC Avalanche Photodiodes - Crystal Orientation and Spatial Uniformity D.B. Habersat, A. Sampath, G. Garrett, M. Derenge, F. Nouketcha, B. VanMil, M. Wraback, J. Schuster, J. Smith, E. Bellotti, M. Zhu, R. Ghandi and M. Aghayan	789
Influence of Gold Nanoparticle Distribution on the Performance of Self-Powered Silicon Carbide Ultraviolet Photodetector K. Teker, M.A. Yildirim and T.U. Teker	795
Fabrication of 4H-SiC Low Gain Avalanche Detectors (LGADs) B.J. Sekely, Y. Satapathy, T. Yang, G. Allion, P. Barletta, S. Holland, S. Stucci, C. Haber, S. Pavlidis and J.F. Muth	800
All Electrical Near-Zero Field Magnetoresistance Magnetometry up to 500°C Using SiC Devices F. Sgrignuoli, I. Viti, Z.G. Yu, E. Allridge, P.M. Lenahan, S. Goswami, R. Ghandi, M. Aghayan and D.M. Shaddock	808
SiC in Space: Potential High-Power Application Survey A. Arrizabalaga	817
SiC Half-Bridge Modules to Improve Efficiency and Reduce Area of High-Power Motor Drives in Space A. Arrizabalaga	827
Latching Current Limiter for High-Power Distribution in Space Enabled by SiC N-MOSFET A. Arrizabalaga	835