

Table of Contents

Preface

Punching of Prismatic Dislocation Loops from Inclusions in 4H-SiC Wafers Q.Y. Cheng, K.W. Kayang, Z.Y. Chen, S.S. Hu, B. Raghothamachar, M. Dudley, D. Gersappe, A. Soukhojak and S. Baek	1
Exploring the Influence of Implant Profile and Device Design on Basal Plane Dislocation Generation in 1.2kV 4H-SiC Power MOSFETs S.A. Mancini, S.Y. Jang, Z.Y. Chen, B. Raghothamachar, M. Dudley and W.J. Sung	11
Coherency between Epitaxial Defectivity, Surface Voltage, Photoluminescence Mapping and Electrical Wafer Sorting for 200mm SiC Wafers J. Thörnberg, G. Polisski, S. Giuffrida, V. de Luca, A. Catena, M. Wilson and B. Magnusson	19
Defect Density Reduction in 4H-SiC (0001) Epilayer via Growth-Interruption during Buffer Layer Growth S. Kumar, L.K. Bera, X.S. Nguyen, W.D. Song, A.M.A. Lee, X.Y. Li, E.S. Tok, M.S. Bharathi, C.D. Reddy, U. Chand, S. Chung, N. Singh and Y.C. Yeo	27
Dynamics of Stacking Fault Expansion in H⁺ Implanted SiC-MOSFETs K. Ishibashi, N. Shikama, H. Niwa, T. Tanaka, H. Amishiro, A. Imai, K. Sugawara, Y. Kagawa and A. Furukawa	33
Challenges in Investigating UIS Material-Based Failures & Yield Prediction in the Absence of Robust 4H-SiC Epiwafer Quality Standards J. Soto, B. Odekirk, S. Maximenko, B. Rodgers, M. Fisher and K. Speer	41
Polarization Superimposed Phase Contrast Microscope Inspection of Dislocations in SiC Epitaxial Layer R. Hattori, Y. Yao and Y. Ishikawa	47
High Temperature Evolution of Thin Films Confined between Two SiC Substrates M. Le Cunff, F. Rieutord, D. Landru, O. Kononchuk and N. Cherkashin	55
Non-Contact Full Wafer Imaging of Electrically Active Defects in 4H-SiC Epi with Comparison to End of Line Electrical Device Data F. Faisal, N. Steller, R. Karhu, B. Kallinger, G. Polisski, M. Wilson, A. Savtchouk, L. Gutierrez, C. Almeida, D. Marinskiy and J. Lagowski	63
How to Simulate Bipolar Degradation by UV Irradiation with High Accuracy Y. Igarashi, K. Takano, Y. Matsushita and T. Morita	71