

Table of Contents

Preface

Investigation of Potential Impact of Nitridation Process on Single Event Gate Rupture Tolerance in SiC MOS Capacitors

M. Takahashi, E. Kagoshima, T. Makino, M. Iwata, N. Ohtani, N. Nemoto, S. Narita, T. Tawara, J. Senzaki, K. Kobayashi, T. Suematsu, S. Harada, A. Takeyama, T. Ohshima, J. Saito, H. Fujiwara and H. Shindou

1

Venus Surface Environmental Chamber Test of SiC JFET-R Multi-Chip Circuit Board

P.G. Neudeck, L.Y. Chen, L.C. Greer, D.J. Spry, N.F. Prokop, D. Lukco, M.J. Krasowski and G.W. Hunter

7

Coupled Non-Destructive Methods, Kelvin Force Probe Microscopy and μ -Raman to Characterize Doping in 4H-SiC Power Devices

E. Vuillermet, K.T. Wu, A. Sedilot, R. Deturche, N. Bercu, E. Usureau, J. Beal and M. Lazar

13

Concept and Technology for Full Monolithic MOSFET and JBS Vertical Integration in Multi-Terminal 4H-SiC Power Converters

R. Makhoul, N. Beydoun, A. Bourennane, L.V. Phung, F. Richardeau, M. Lazar, P. Godignon, D. Planson, H. Morel and D. Bourrier

23

Comparing 4H-SiC NPN Buffer Layers by Epitaxial Growth and Implantation for Neural Interface Isolation

S. Greenhorn, E. Bano, V. Stambouli and K. Zekentes

31

Modeling the Charging of Gate Oxide under High Electric Field

D. Scholten and J. Baringhaus

37

Complementary Two Dimensional Carrier Profiles of 4H-SiC MOSFETs by Scanning Spreading Resistance Microscopy and Scanning Capacitance Microscopy

P. Fiorenza, M. Zignale, E. Zanetti, M.S. Alessandrino, B. Carbone, A. Guarnera, M. Saggio, F. Giannazzo and F. Roccaforte

45

Temperature Dependence of 4H-SiC Gate Oxide Breakdown and C - V Properties from Room Temperature to 500 °C

A. May, L. Baier and M. Rommel

51

Detection of Very Fast Interface Traps at 4H-SiC/AlN and 4H-SiC/Al₂O₃ Interfaces

A.M. Vidarsson, A.R. Persson, J.T. Chen, D. Haasmann, J. Ul-Hassan, S. Dimitrijević, N. Rorsman, V. Darakchieva and E.Ö. Sveinbjörnsson

59

A Voltage Adjustable Diode Integrated SiC Trench MOSFET with Barrier Control Gate

S.J. Li, X.C. Deng, X. Li, X. Li and Y. Wen

65

Effects of High Gate Voltage Stress on Threshold Voltage Stability in Planar and Trench SiC Power MOSFETs

A.K. Biswas, D.J. Lichtenwalner, S. Das, C. Isaacson, S. Ganguly and D.A. Gajewski

71

Design of Al₂O₃/LaAlO₃/SiO₂ Gate Stack on Various Channel Planes for High-Performance 4H-SiC Trench Power MOSFETs

L.H. Huang, Y. Liu, X. Peng, T. Tsuji, Y. Onozawa, N. Fujishima and J.K.O. Sin

79

Channel Density Design Guidelines for the Transient Characteristics of SiC Trench Gate MOSFETs

S. Kimoto, R. Iijima and S. Harada

89

Analysis of On-State and Short-Circuit Capability in 3D Trench SiC MOSFET Designs

K. Melnyk, L.Y. Zhang, P.M. Gammon, A.B. Renz and M. Antoniou

97

Revised Channel Mobility Model for Predictive TCAD Simulations of 4H-SiC MOSFETs

H. Dixit, D.J. Lichtenwalner, A. Scholze, J. Kim, K.J. Han and S.H. Ryu

103

Improvement of Reflectance Spectroscopy for Oxide Layers on 4H-SiC

J. Koerfer, M. Rommel, A. Fuchs and O. Rusch

109

Doping and Temperature Dependence of Carrier Lifetime in 4H SiC Epitaxial Layers

L. Lilja and J.P. Bergman

115

Fail-to-Open Short Circuit Failure Mode of SiC Power MOSFETs: 2-D Thermo-Mechanical Modeling

I. Kovacevic-Badstuebner, S. Race, N. Luethi, M. Nagel and U. Grossner

121

Gate Resistance Integration in SiC MOSFETs: Performance Simulations under Different Implementation Methods

M. Pulvirenti, D. Cavallaro, A. Cascio, A. Raffa, L. Salvo, A. Sciacca, A. Guarnera, E. Zanetti and M. Saggio

127

Fast Estimation of the Lateral Fidelity of Ion Implantation in 4H-SiC through Calibration to JFET Transfer Characteristics in TCAD

K. Sakai, N. Boettcher, M. Szabo, S. Beuer and M. Rommel

133